Infineon Technologies - SAF-XC164D-32F20F BB Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164d-32f20f-bb

  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Four Programmable Chip-Select Signals
- Up to 79 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers,
  Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers,
  Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 100-Pin Green TQFP Package, 0.5 mm (19.7 mil) pitch (RoHS compliant)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164D please refer to your responsible sales representative or your local distributor.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the XC164D group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164D** throughout this document.

Table 1 XC164D Derivative Synopsis

Derivative[1]	Temp. Range	Program Memory	On-Chip RAM	Interfaces
Standard Devices[2]				
SAF-XC164D-32F40F SAF-XC164D-32F20F	-40 °C to 85 °C	256 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 6 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, CC6
ROM Devices				
SAF-XC164D-32R40F SAF-XC164D-32R20F	-40 °C to 85 °C	256 Kbytes ROM	2 Kbytes DPRAM, 4 Kbytes DSRAM, 6 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1, CAN0, CAN1, CC6

1) This Data Sheet is valid for devices starting with and including design step BB.

2) The Flash speed grading indicates the access time to the on-chip Flash module. According to this access time Flash waitstates must be selected (bitfield WSFLASH in register IMBCTRL) according to the intended operating frequency. For more details, please refer to **Section 4.3.2**.

2.2 Pin Configuration and Definition

The pins of the XC164D are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

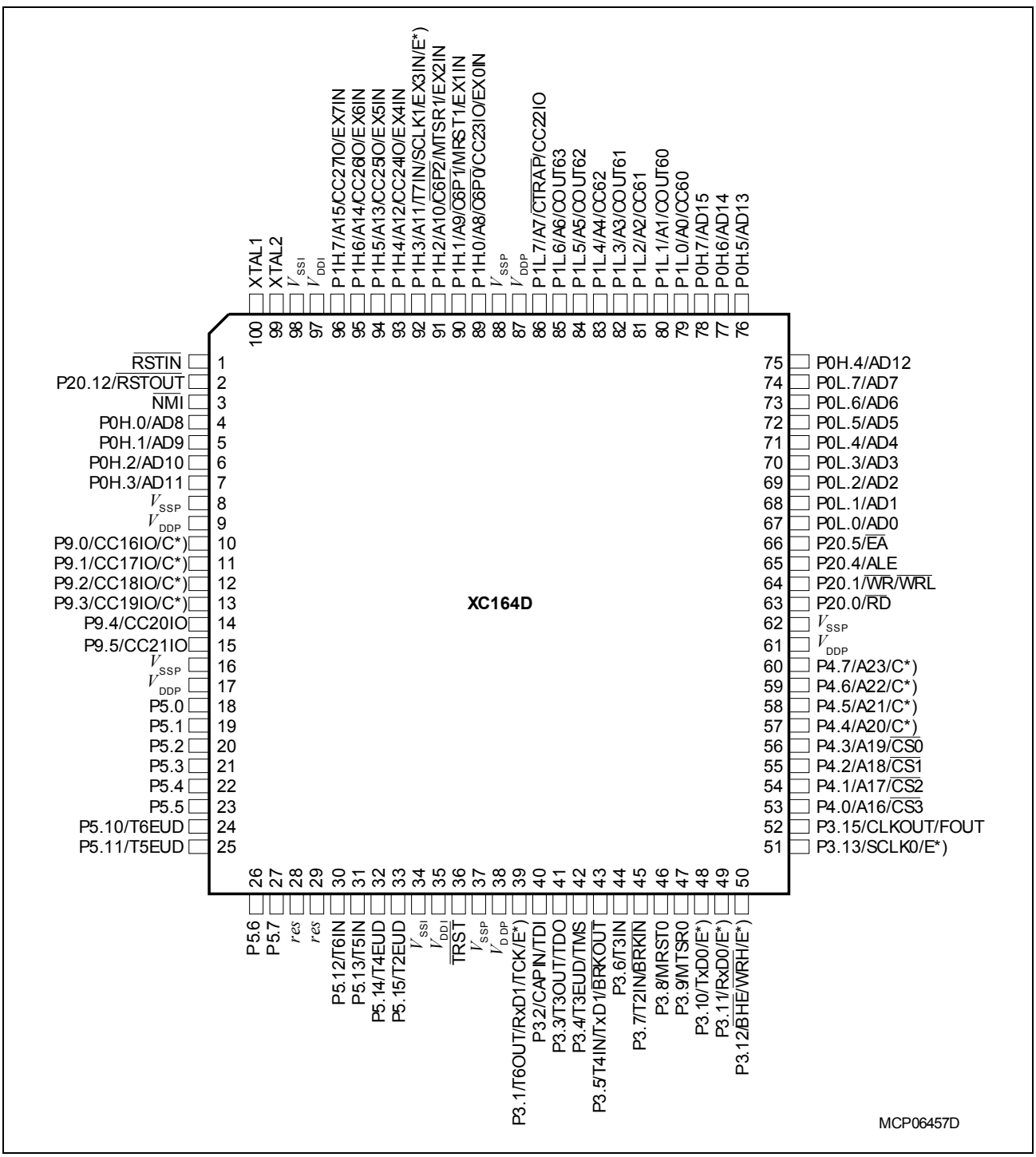

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	1	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164D. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
P20.12	2	IO	For details, please refer to the description of **P20**.
$\overline{\text{NMI}}$	3	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164D into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P0H.0-P0H.3	4…7	IO	For details, please refer to the description of **PORT0**.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{TRST}}$	36	I	Test-System Reset Input. For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{RSTIN}}$ activates the XC164CM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 14-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	39	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	40	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	41	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	42	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	43	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
		O	$\overline{\text{TxD1}}$	ASC0 Clock/Data Output (Async./Sync.),
		O	$\overline{\text{BRKOUT}}$	Debug System: Break Out
P3.6	44	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	45	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
		I	$\overline{\text{BRKIN}}$	Debug System: Break In
P3.8	46	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	47	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	48	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	49	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	$\overline{\text{EX2IN}}$	Fast External Interrupt 2 Input (alternate pin A)
P3.12	50	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	51	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	52	O	CLKOUT	System Clock Output (= CPU Clock),
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]
P4.0	53	O	$\overline{A16}$ Least Significant Segment Address Line,
		O	$\overline{CS3}$ Chip Select 3 Output
P4.1	54	O	$\overline{A17}$ Segment Address Line,
		O	$\overline{CS2}$ Chip Select 2 Output
P4.2	55	O	$\overline{A18}$ Segment Address Line,
		O	$\overline{CS1}$ Chip Select 1 Output
P4.3	56	O	$\overline{A19}$ Segment Address Line,
		O	$\overline{CS0}$ Chip Select 0 Output
P4.4	57	O	A20 Segment Address Line,
		I	CAN1_RxD CAN Node B Receive Data Input,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin B)
P4.5	58	O	A21 Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin B)
P4.6	59	O	A22 Segment Address Line,
		O	CAN0_TxD CAN Node A Transmit Data Output,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin A)
P4.7	60	O	A23 Most Significant Segment Address Line,
		I	CAN0_RxD CAN Node A Receive Data Input,
		O	CAN1_TxD CAN Node B Transmit Data Output,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P20		IO	Port 20 is a 5-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output. The input threshold of Port 20 is selectable (standard or special). The following Port 20 pins also serve for alternate functions:
P20.0	63	O	$\overline{RD}$ External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	64	O	$\overline{WR}$/$\overline{WRL}$ External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus.
P20.4	65	O	ALE Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	66	I	$\overline{EA}$ External Access Enable pin. **A low level** at this pin during and after Reset forces the XC164D to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the XC164D to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
P20.12	2	O	$\overline{RSTOUT}$ Internal Reset Indication Output. **Is activated** asynchronously with an external hardware reset. It may also be activated (selectable) synchronously with an internal software or watchdog reset. **Is deactivated** upon the execution of the EINIT instruction, optionally at the end of reset, or at any time (before EINIT) via user software.
			Note: Port 20 pins may input configuration values (see $\overline{EA}$).

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

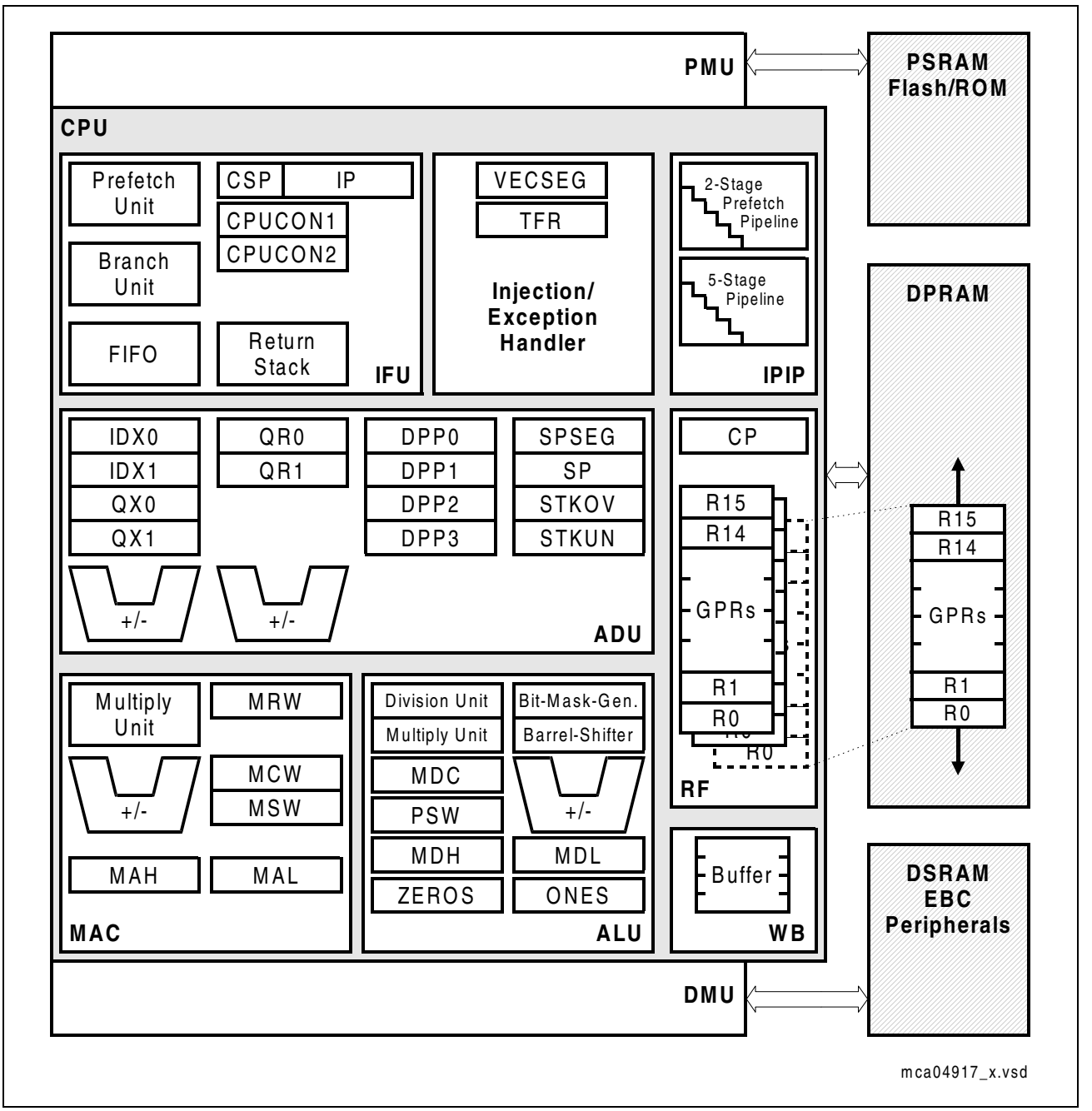

Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC164D's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164D is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164D supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164D has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC164D interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

The XC164D also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	$xx'0000_H$	00_H	III
• Software Reset		RESET	$xx'0000_H$	00_H	III
• Watchdog Timer Overflow		RESET	$xx'0000_H$	00_H	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	$xx'0008_H$	02_H	II
• Stack Overflow	STKOF	STOTRAP	$xx'0010_H$	04_H	II
• Stack Underflow	STKUF	STUTRAP	$xx'0018_H$	06_H	II
• Software Break	SOFTBRK	SBRKTRAP	$xx'0020_H$	08_H	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	$xx'0028_H$	$0A_H$	I
• PMI Access Error	PACER	BTRAP	$xx'0028_H$	$0A_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	$xx'0028_H$	$0A_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	$xx'0028_H$	$0A_H$	I
Reserved	–	–	$[2C_H - 3C_H]$	$[0B_H - 0F_H]$	–
Software Traps • TRAP Instruction	–	–	Any $[xx'0000_H - xx'01FC_H]$ in steps of 4_H	Any $[00_H - 7F_H]$	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

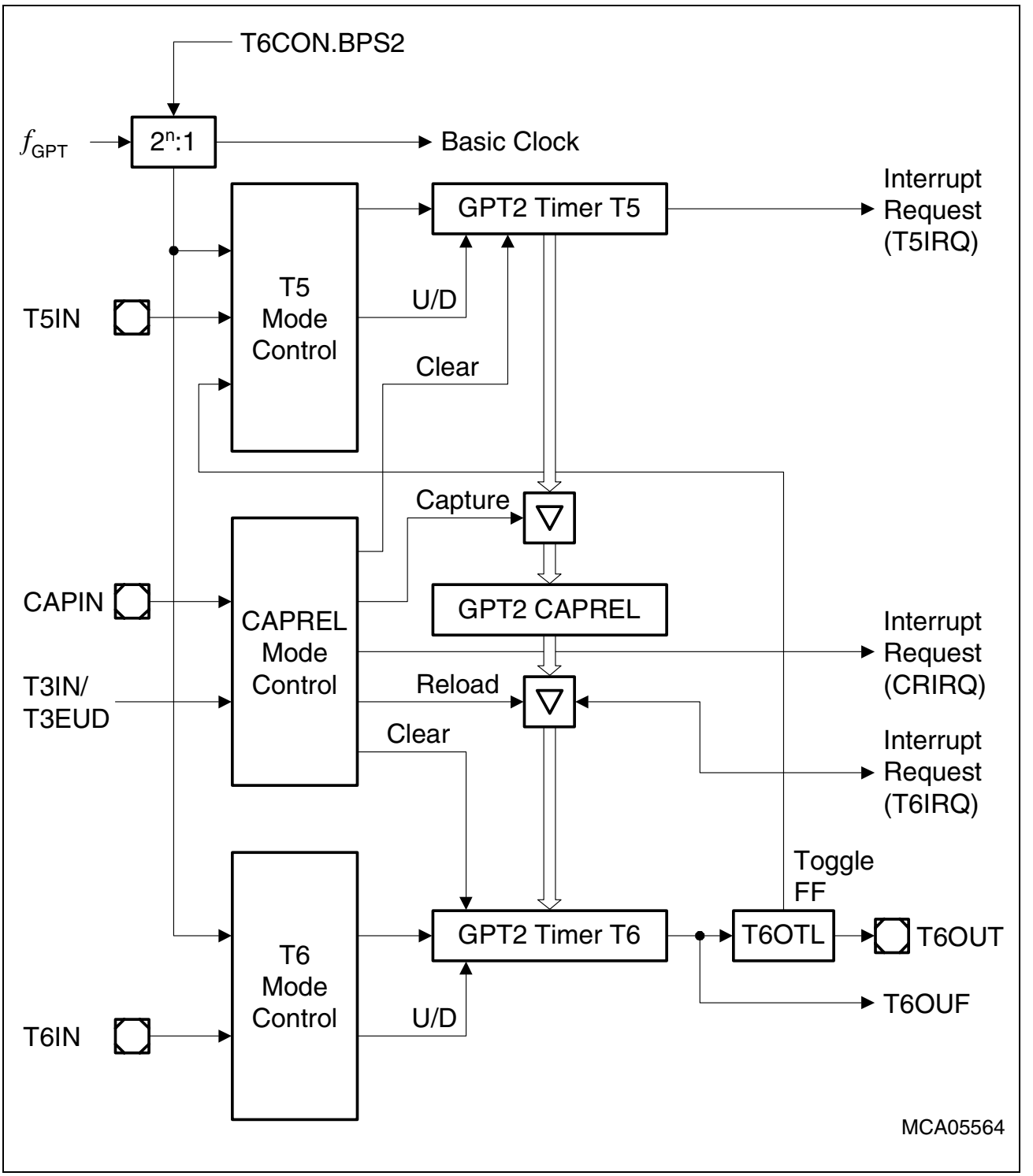

Figure 8 Block Diagram of GPT2

3.16 Power Management

The XC164D provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC164D into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC164D's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC164D by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP}$ - 0.1	V	–
Input low voltage XTAL1[2)]	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	[3)]
Input high voltage TTL (all except XTAL1)	V_{IH}	SR	$0.2 \times V_{DDP}$ + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1[2)]	V_{IHC}	SR	$0.7 \times V_{DDI}$	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP}$ - 0.2	V_{DDP} + 0.5	V	[3)]
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	–	V	V_{DDP} in [V], Series resistance = 0 Ω[3)]
Output low voltage	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[4)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[4)5)]
Output high voltage[6)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[4)]
			V_{DDP} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[4)5)]
Input leakage current (Port 5)[7)]	I_{OZ1}	CC	–	±300	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 125$ °C
				±200	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 85$ °C[14)]
Input leakage current (all other[8)])[7)]	I_{OZ2}	CC	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[9)]	I_{CPUH}[10)]		–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[11)]		-100	–	µA	$V_{IN} = V_{ILmax}$
Configuration pull-down current[12)]	I_{CPDL}[10)]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[11)]		120	–	µA	$V_{IN} = V_{IHmin}$

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Level inactive hold current[13]	I_{LHI}[10]		–	-10	µA	V_{OUT} = 0.5 × V_{DDP}
Level active hold current[13]	I_{LHA}[11]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[14] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) This parameter is tested for P3, P4, P9.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

9) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0

10) The maximum current may be drawn while the respective signal line remains inactive.

11) The minimum current must be drawn to drive the respective signal line active.

12) This specification is valid during Reset for configuration on ALE.

13) This specification is valid during Reset for pins P4.3-0, which can act as $\overline{CS}$ outputs, and for P3.12.

14) Not subject to production test - verified by design/characterization.

Table 12 Current Limits for Port Output Drivers

Port Output Driver Mode	Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)[1]	Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)
Strong driver	10 mA	2.5 mA
Medium driver	4.0 mA	1.0 mA
Weak driver	0.5 mA	0.1 mA

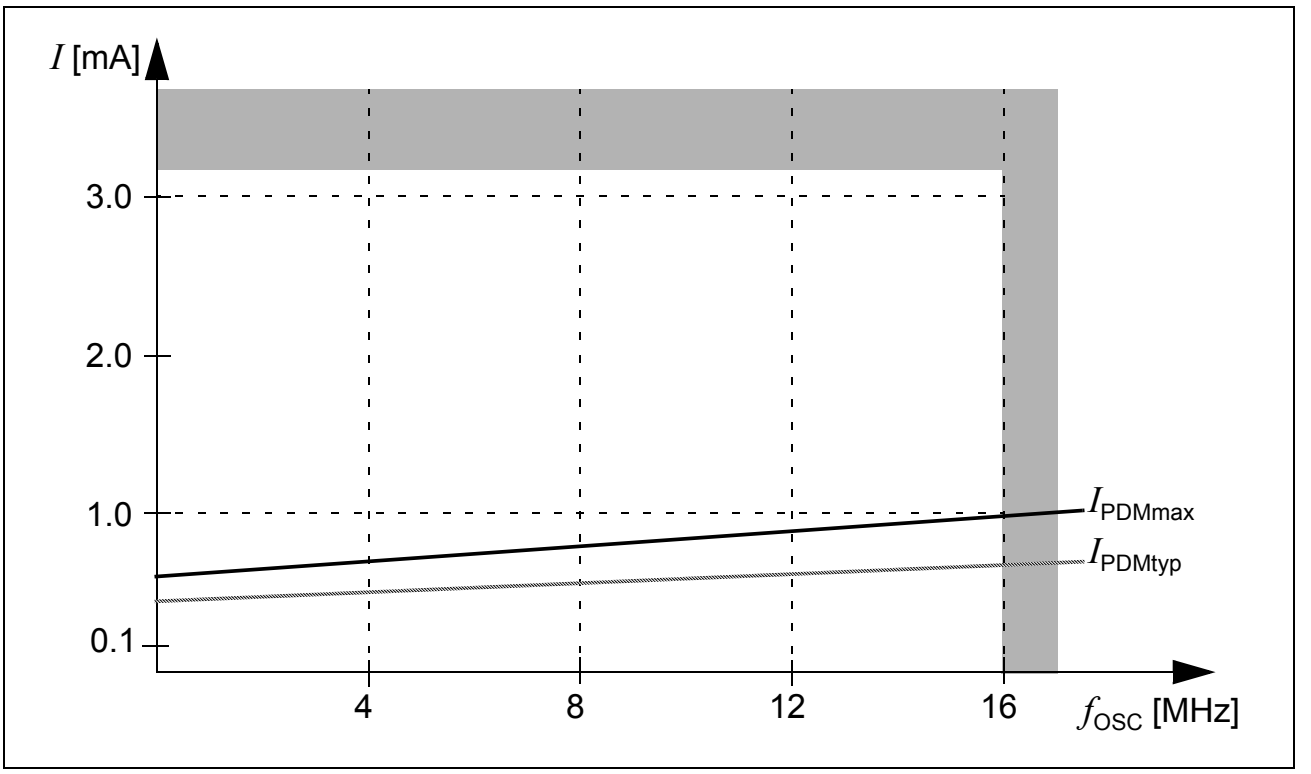

Figure 12 **Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency**

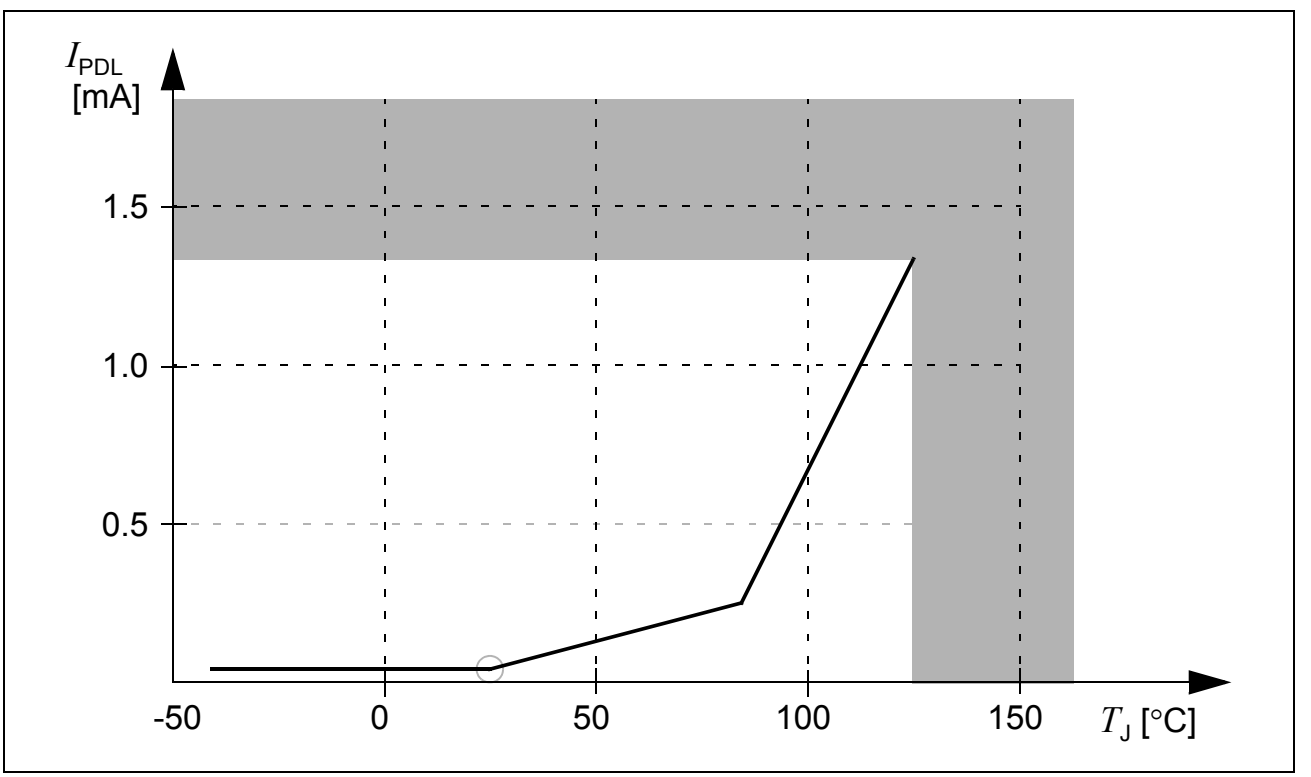

Figure 13 **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

4.3.5 External Bus Timing

Table 18 CLKOUT Reference Signal

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

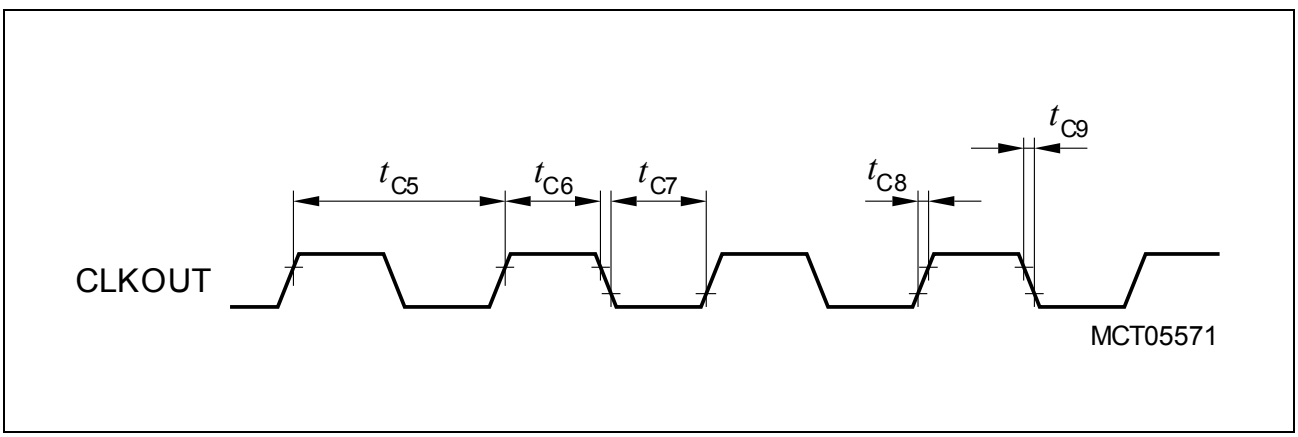

Figure 19 CLKOUT Signal Timing

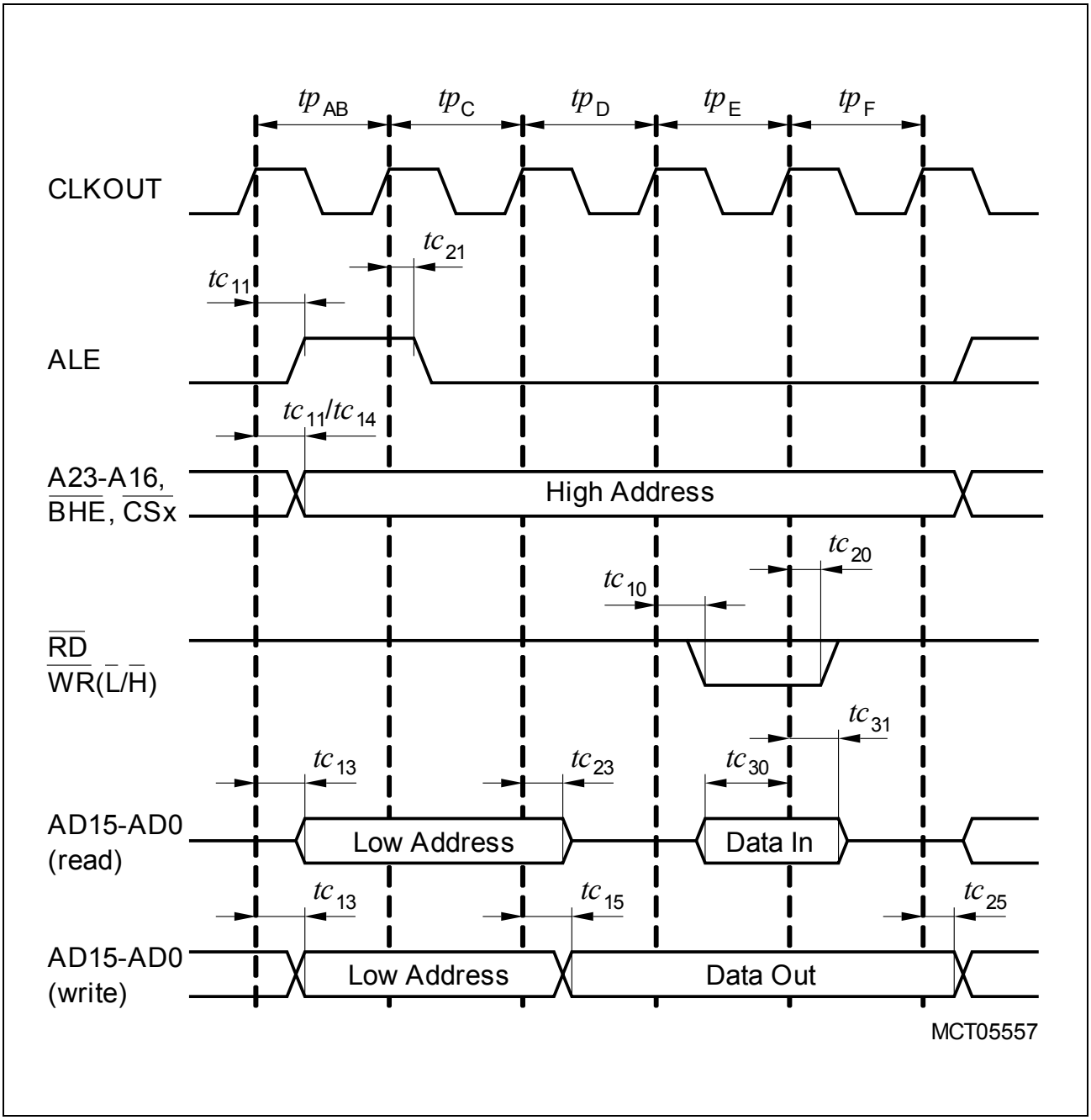

Figure 20 Multiplexed Bus Cycle

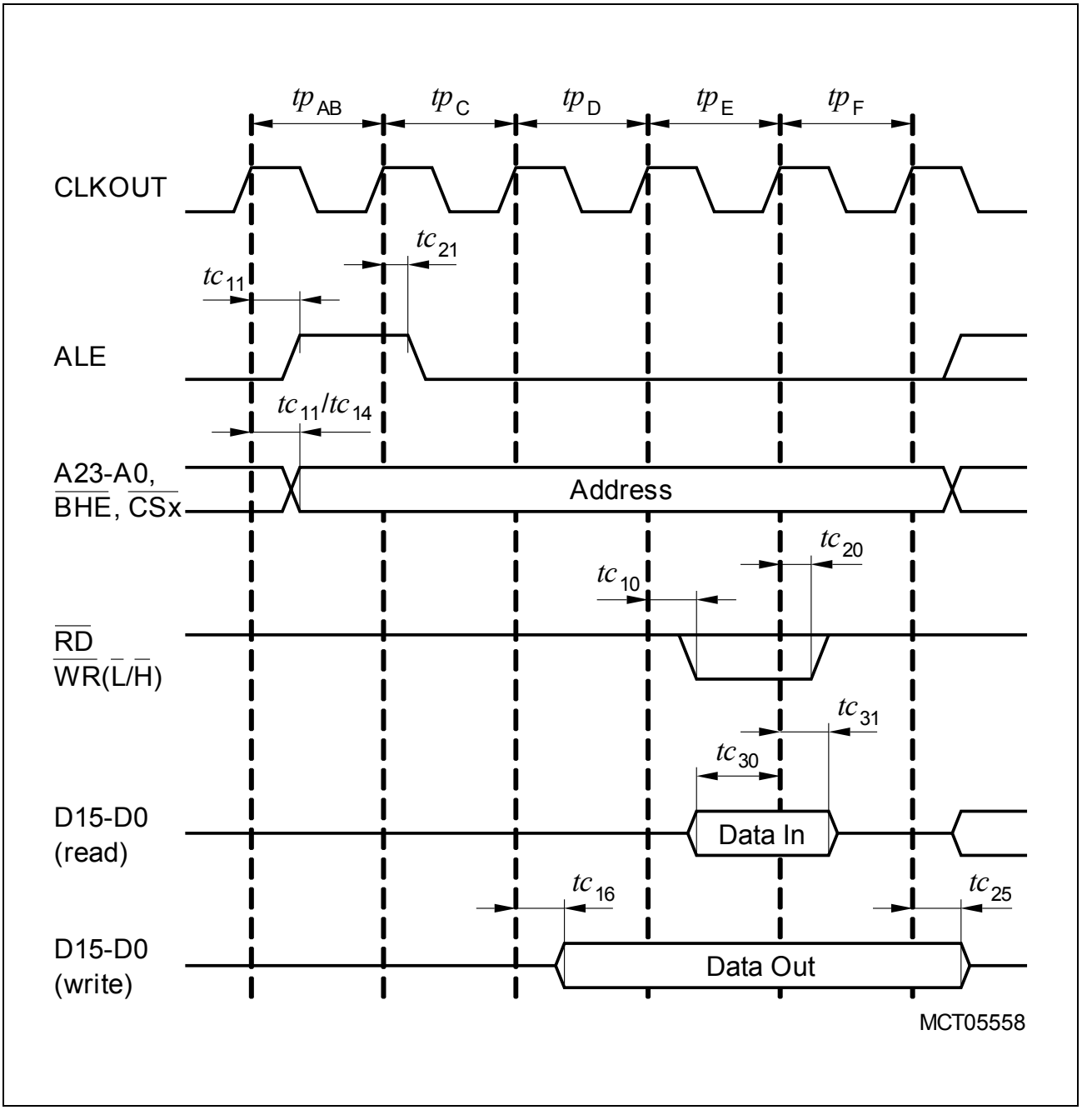

Figure 21 Demultiplexed Bus Cycle

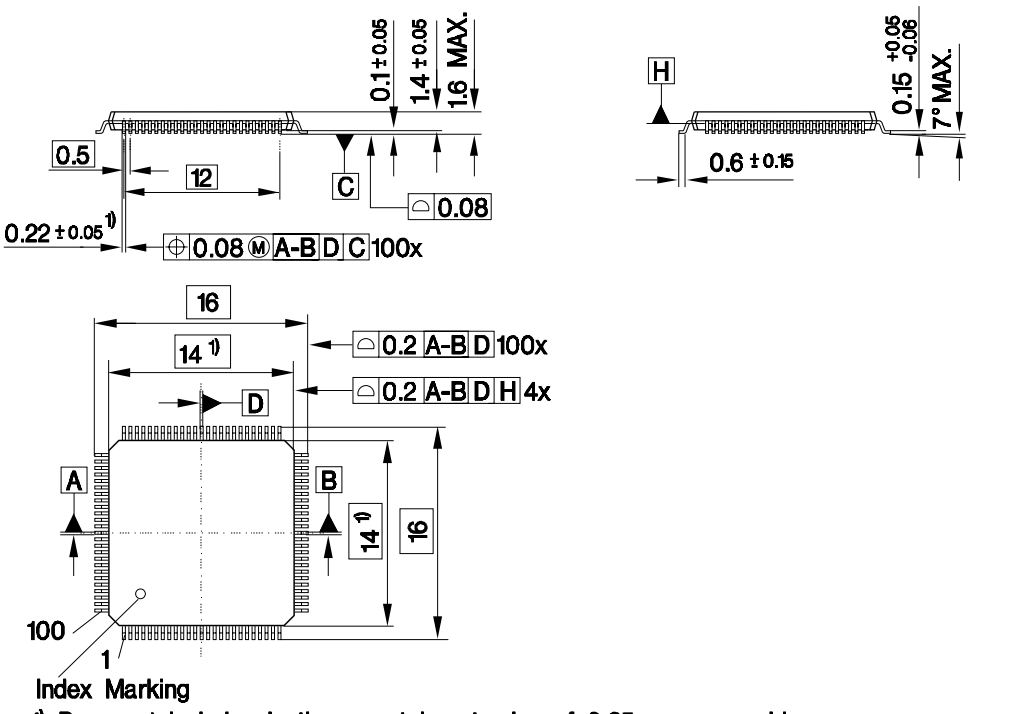

Figure 23 P-TQFP-100-16 (Plastic Thin Quad Flat Package)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**. Dimensions in mm