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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l162m8t6

IWDG: Independent watchdog
LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

3.1 Low-power modes

The high-density STM8L162x8 devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

3.3 Reset and supply management

3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage (V_{DD}). The external power supply pins must be connected as follows:

- V_{SS1}, V_{DD1}, V_{SS2}, V_{DD2}, V_{SS3}, V_{DD3}, V_{SS4}, V_{DD4}= 1.65 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through V_{DD} pins, the corresponding ground pin is V_{SS}. V_{SS1}/V_{SS2}/V_{SS3}/V_{SS4} and V_{DD1}/V_{DD2}/V_{DD3}/V_{DD4} must not be left unconnected.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external power supplies for analog peripherals (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC1 is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{REF+}, V_{REF-} (for ADC1): external reference voltage for ADC1. Must be provided externally through V_{REF+} and V_{REF-} pin.
- V_{REF+} (for DAC1/2): external voltage reference for DAC1 and DAC2 must be provided externally through V_{REF+}.

3.3.2 Power supply supervisor

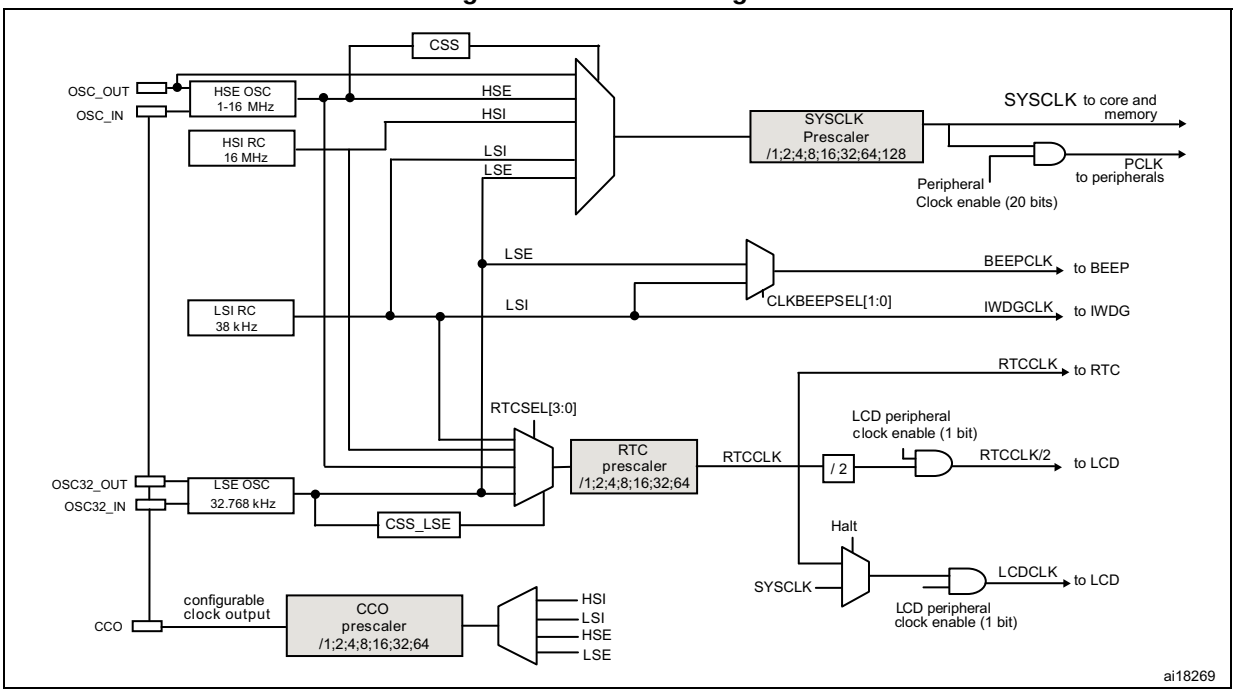
The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR). For the device sales types without the “D” option (see *Section 11: Ordering information scheme*), it is coupled with a brownout reset (BOR) circuitry. It that case the device operates between 1.8 and 3.6 V, BOR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the V_{DD} min. value at power-down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: For device sales types with the “D” option (see Section 11: Ordering information scheme) BOR is permanently disabled and the device operates between 1.65 and 3.6 V. In this case it is not possible to enable BOR through the option bytes.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Figure 2. Clock tree diagram



3.5 Low-power real-time clock

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field can also be read in binary format.

The calendar can be corrected from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5 ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from LSE period to every year

A clock security system detects a failure on LSE, and can provide an interrupt with wakeup capability. The RTC clock can automatically switch to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and can wakeup the MCU.

3.6 LCD (Liquid crystal display)

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. It can also be configured to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever V_{DD}.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

Note: Unnecessary segments and common pins can be used as general I/O pins.

3.7 Memories

The high-density STM8L162x8 devices have the following main features:

- 4 Kbytes of RAM
- The non-volatile memory is divided into three arrays:
  - 64 Kbytes of medium-density embedded Flash program memory
  - 2 Kbytes of Data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, AES, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage V_{REFINT}. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see *Section 3.13: Touch sensing*).

3.13 Touch sensing

The high-density STM8L162x8 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (for example glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In the high-density STM8L162x8 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solution can be quickly and easily implemented using the free STM8 touch sensing firmware library.

3.14 AES

The AES Hardware Accelerator can be used to encipher and decipher data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 892 clock cycles to encrypt/decrypt one 128-bit block

AES data flow can be served by the DMA1 controller.

3.15 Timers

The high-density STM8L162x8 devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

Table 2 compares the features of the advanced control, general-purpose and basic timers.

Table 4. STM8L162x8 pin description (continued)

Pin number		Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
80	-	PI3/TIM5_CH1/ *[SPI2_MISO]/[TIM3_CH2]*	I/O	FT (3)	**X**	X	X	HS	X	X	**Port I3**	TIM5 Channel 1 *[SPI2 master in- slave out] [TIM3 channel 2]*
-	39	PF0/ADC1_IN24/ DAC_OUT1 *[USART3_TX]*	I/O		**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]*
49	-	PF0/ADC1_IN24/ DAC_OUT1/*[USART3_TX] /[SPI1_MISO]*	I/O		**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit] [SPI1* master in- slave out*]*
50	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]*	I/O		**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive] [SPI1* master out- slave in*]*
-	40	PF1/ADC1_IN25/ DAC_OUT2/*[USART3_RX]*	I/O		**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]*
51	-	PF2/ADC1_IN26/ [SPI2_SCK]/ [USART3_SCK]	I/O		**X**	X	X	HS	X	X	**Port F2**	ADC1_IN26 *[SPI2 clock] [USART3 clock]*
52	-	PF3/ADC1_IN27/ [SPI1_NSS]	I/O		**X**	X	X	HS	X	X	**Port F3**	ADC1_IN26 *[SPI1 master/slave select]*
53	41	PF4/LCD_SEG36 /LCD_COM4(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F4**	LCD_SEG36/ LCD COM4(7)
54	42	PF5/LCD_SEG37/ LCD_COM5(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F5**	LCD_SEG37/ LCD COM5(7)
55	43	PF6/LCD_SEG38/ LCD_COM6(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F6**	LCD_SEG38/ LCD COM6(7)
56	44	PF7/LCD_SEG39/ LCD_COM7(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F7**	LCD_SEG39/ LCD COM7(7)
22	18	VLCD	S								LCD booster external capacitor	
15	11	V_{DD1}	S								Digital power supply	
14	10	V_{SS1}									I/O ground	
16	12	V_{DDA}	S								Analog supply voltage	
17	13	V_{REF+}/V_{REF+_DAC}	S								ADC1 and DAC1/2 positive voltage reference	

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 516A	RTC	RTC_CALRH	Calibration register high	0x00(1)
0x00 516B		RTC_CALRL	Calibration register low	0x00(1)
0x00 516C		RTC_TCR1	Tamper control register 1	0x00(1)
0x00 516D		RTC_TCR2	Tamper control register 2	0x00(1)
0x00 516E to 0x00 518A	Reserved area			
0x00 5190	CSSLSE	CSSLSE_CSR	CSS on LSE control and status register	0x00(1)
0x00 519A to 0x00 51FF	Reserved area			
0x00 5200	SPI1	SPI1_CR1	SPI1 control register 1	0x00
0x00 5201		SPI1_CR2	SPI1 control register 2	0x00
0x00 5202		SPI1_ICR	SPI1 interrupt control register	0x00
0x00 5203		SPI1_SR	SPI1 status register	0x02
0x00 5204		SPI1_DR	SPI1 data register	0x00
0x00 5205		SPI1_CRCPR	SPI1 CRC polynomial register	0x07
0x00 5206		SPI1_RXCRCR	SPI1 Rx CRC register	0x00
0x00 5207		SPI1_TXCRCR	SPI1 Tx CRC register	0x00
0x00 5208 to 0x00 520F	Reserved area (8 bytes)			
0x00 5210	I2C1	I2C1_CR1	I2C1 control register 1	0x00
0x00 5211		I2C1_CR2	I2C1 control register 2	0x00
0x00 5212		I2C1_FREQR	I2C1 frequency register	0x00
0x00 5213		I2C1_OARL	I2C1 own address register low	0x00
0x00 5214		I2C1_OARH	I2C1 own address register high	0x00
0x00 5215		I2C1_OARH	I2C1 own address register for dual mode	0x00
0x00 5216		I2C1_DR	I2C1 data register	0x00
0x00 5217		I2C1_SR1	I2C1 status register 1	0x00
0x00 5218		I2C1_SR2	I2C1 status register 2	0x00
0x00 5219		I2C1_SR3	I2C1 status register 3	0x0X
0x00 521A		I2C1_ITR	I2C1 interrupt control register	0x00
0x00 521B		I2C1_CCRL	I2C1 clock control register low	0x00
0x00 521C		I2C1_CCRH	I2C1 clock control register high	0x00
0x00 521D		I2C1_TRISER	I2C1 TRISE register	0x02
0x00 521E		I2C1_PECR	I2C1 packet error checking register	0x00

6 Interrupt vector mapping

Table 10. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)(1)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	TLI(2)	External Top level Interrupt	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(3)	0x00 800C
2	DMA1 0/1	DMA1 channels 0/1	-	-	Yes	Yes(3)	0x00 8010
3	DMA1 2/3	DMA1 channels 2/3	-	-	Yes	Yes(3)	0x00 8014
4	RTC/LSE_ CSS	RTC alarm interrupt/LSE CSS interrupt	Yes	Yes	Yes	Yes	0x00 8018
5	EXTI E/F/PVD(4)	PortE/F interrupt/PVD interrupt	Yes	Yes	Yes	Yes(3)	0x00 801C
6	EXTIB/G	External interrupt port B/G	Yes	Yes	Yes	Yes(3)	0x00 8020
7	EXTID/H	External interrupt port D/H	Yes	Yes	Yes	Yes(3)	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes(3)	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes(3)	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes(3)	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes(3)	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes(3)	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes(3)	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes(3)	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes(3)	0x00 8044
16	LCD/AES	LCD interrupt/AES interrupt	-	-	Yes	Yes	0x00 8048
17	CLK/ TIM1/ DAC	System clock switch/CSS interrupt/TIM1 break/DAC	-	-	Yes	Yes	0x00 804C
18	COMP1/ COMP2 ADC1	Comparator 1 and 2 interrupt/ADC1	Yes	Yes	Yes	Yes(3)	0x00 8050
19	TIM2/ USART2	TIM2 update /overflow/trigger/break/ USART2 transmission complete/transmit data register empty interrupt	-	-	Yes	Yes(3)	0x00 8054

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

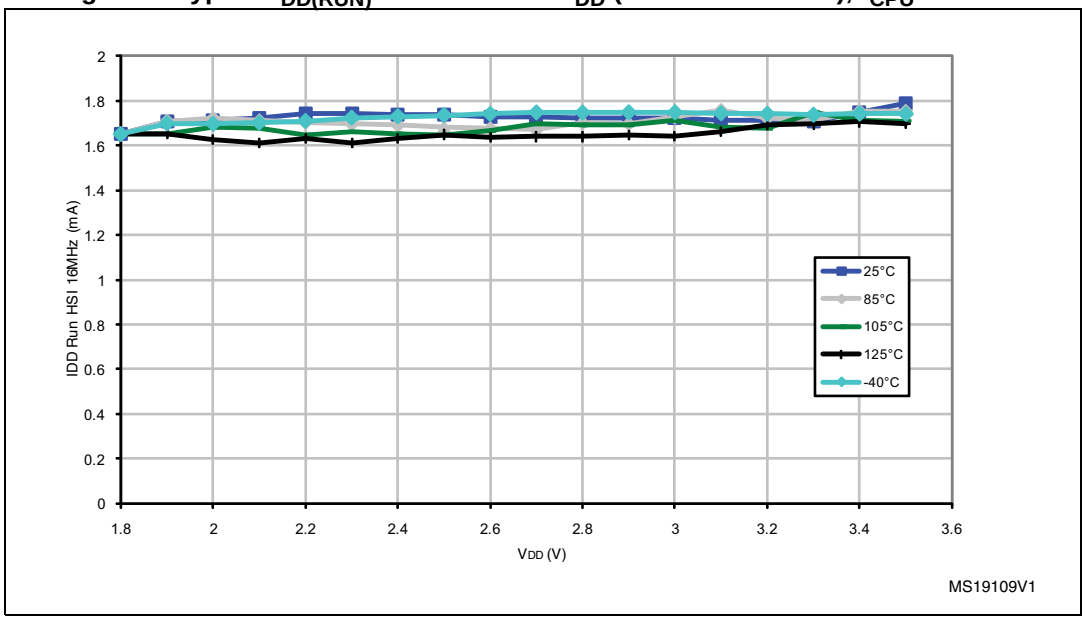
In the following table, data are based on characterization results, unless otherwise specified.

Subject to general operating conditions for V_{DD} and T_A.

Table 19. Total current consumption in Run mode

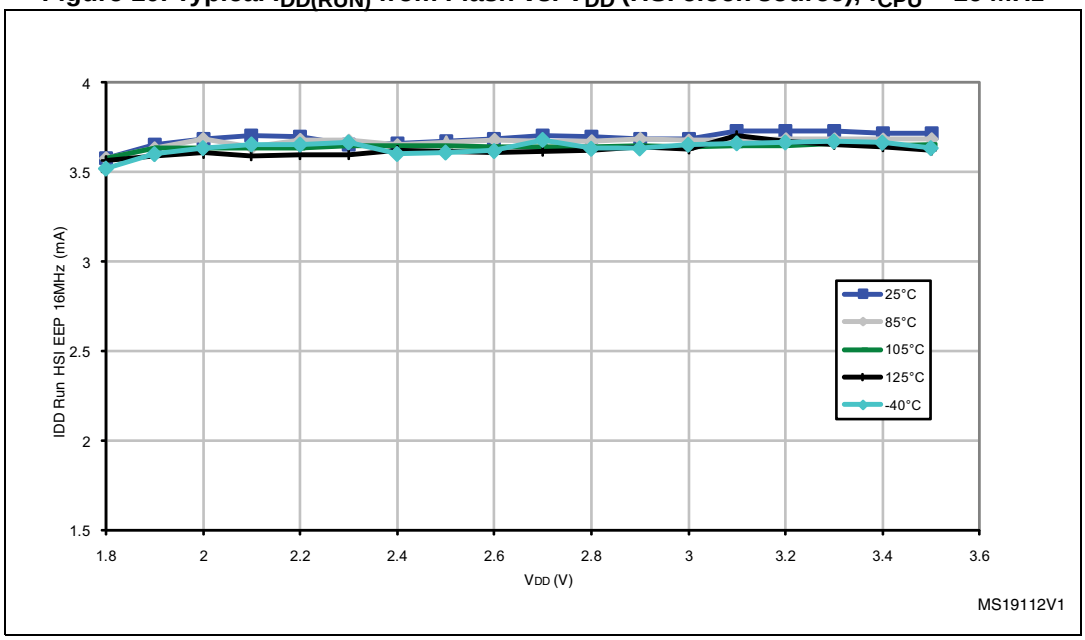
Symbol	Parameter	Conditions(1)			Typ.	Max.				Unit
						55°C	85 °C (2)	105 °C (3)	125 °C (4)	
$I_{DD(RUN)}$	Supply current in run mode (5)	All peripherals OFF, code executed from RAM, V_{DD} from 1.65 V to 3.6 V	HSI RC osc. (16 MHz)(6)	f_{CPU} = 125 kHz	0.22	0.28	0.39	0.47	0.51	mA
				f_{CPU} = 1 MHz	0.32	0.38	0.49	0.57	0.61	
				f_{CPU} = 4 MHz	0.59	0.65	0.76	0.84	0.88	
				f_{CPU} = 8 MHz	0.93	0.99	1.1	1.18	1.22	
				f_{CPU} = 16 MHz	1.62	1.68	1.79(7)	1.87(7)	1.91(7)	
			HSE external clock (f_{CPU}=f_{HSE}) (8)	f_{CPU} = 125 kHz	0.21	0.25	0.35	0.44	0.49	
				f_{CPU} = 1 MHz	0.3	0.34	0.44	0.53	0.58	
				f_{CPU} = 4 MHz	0.57	0.61	0.71	0.8	0.85	
				f_{CPU} = 8 MHz	0.95	0.99	1.09	1.18	1.23	
				f_{CPU} = 16 MHz	1.73	1.77	1.87(7)	1.96(7)	2.01(7)	
			LSI RC osc. (typ. 38 kHz)	f_{CPU} = f_{LSI}	0.029	0.035	0.039	0.044	0.055	
			LSE external clock (32.768 kHz)	f_{CPU} = f_{LSE}	0.028	0.034	0.038	0.042	0.054	

Figure 9. Typical $I_{DD(RUN)}$ from RAM vs. V_{DD} (HSI clock source), f_{CPU} =16 MHz



1. Typical current consumption measured with code executed from RAM.

Figure 10. Typical $I_{DD(RUN)}$ from Flash vs. V_{DD} (HSI clock source), f_{CPU} = 16 MHz



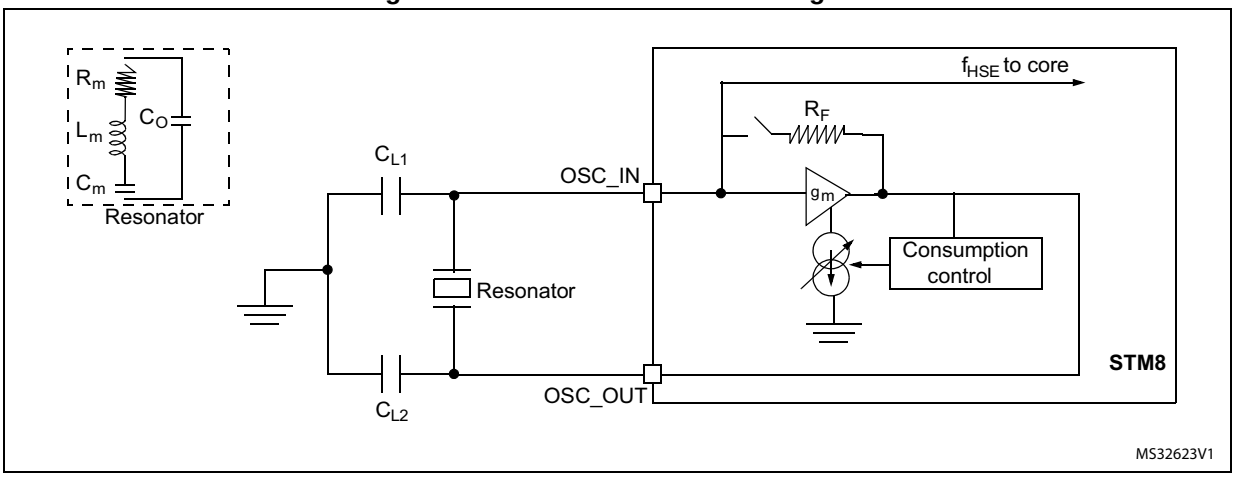
1. Typical current consumption measured with code executed from Flash.

Table 23. Total current consumption and timing in Active-halt mode at V_{DD} = 1.65 V to 3.6 V (continued)

Symbol	Parameter	Conditions[1]			Typ.	Max.	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSE external clock (32.768 kHz) (6)	LCD OFF[7]	T_A = -40 °C to 25 °C	0.54	1.35	µA
				T_A = 55 °C	0.61	1.44	
				T_A = 85 °C	0.91	2.27	
				T_A = 105 °C	2.24	5.42	
				T_A = 125 °C	5.03	12	
			LCD ON (static duty/ external V_{LCD}) [3]	T_A = -40 °C to 25 °C	0.91	2.13	
				T_A = 55 °C	1.05	2.55	
				T_A = 85 °C	1.42	3.65	
				T_A = 105 °C	2.63	6.35	
				T_A = 125 °C	5.24	13.15	
			LCD ON (1/4 duty/ external V_{LCD}) [4]	T_A = -40 °C to 25 °C	1.6	2.84	
				T_A = 55 °C	1.76	4.37	
				T_A = 85 °C	2.14	5.23	
				T_A = 105 °C	3.37	8.5	
				T_A = 125 °C	5.92	15.19	
			LCD ON (1/4 duty/ internal V_{LCD}) [5]	T_A = -40 °C to 25 °C	3.89	9.15	
				T_A = 55 °C	3.89	9.15	
				T_A = 85 °C	4.25	10.49	
				T_A = 105 °C	5.42	16.31	
				T_A = 125 °C	6.58	16.6	
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode (using HSI)	-	-	-	2.4	-	mA
$t_{WU\_HSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using HSI)	-	-	-	4.7	7	µs
$t_{WU\_LSI(AH)}$[8][9]	Wakeup time from Active-halt mode to Run mode (using LSI)	-	-	-	150	-	µs

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external V_{LCD} = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external V_{LCD}, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster V_{LCD} = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 31*

Figure 17. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

R_m: Motional resistance (see crystal specification), L_m: Motional inductance (see crystal specification),
C_m: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification),
C_{L1}=C_{L2}=C: Grounded external capacitance
$g_m >> g_{mcrit}$

LSE crystal/ceramic resonator oscillator

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 31. LSE oscillator characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSE}	Low speed external oscillator frequency			32.768		kHz
R_F	Feedback resistor	ΔV = 200 mV		1.2		MΩ
$C^{(1)(2)}$	Recommended load capacitance			8		pF
$I_{DD(LSE)}$	LSE oscillator power consumption	V_{DD} = 1.8 V		450		nA
		V_{DD} = 3 V		600		
		V_{DD} = 3.6 V		750		
g_m	Oscillator transconductance		3(3)			µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized		1		s

1. $C=C_{L1}=C_{L2}$ is approximately equivalent to 2 x crystal C_{LOAD}.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_m value. Refer to crystal manufacturer for more details.
3. Guaranteed by design. Not tested in production.
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

Table 36. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on true open-drain pins	-5	+0	mA
	Injected current on all 5 V tolerant (FT) pins	-5	+0	
	Injected current on any other pin	-5	+5	

9.3.7 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	-	0.3 x V_{DD}	V
		Input voltage on five-volt tolerant (FT) pins	V_{SS}-0.3	-	0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on five-volt tolerant (FT) pins with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 24*).

Figure 21. Typical V_{IL} and V_{IH} vs. V_{DD} (standard I/Os)

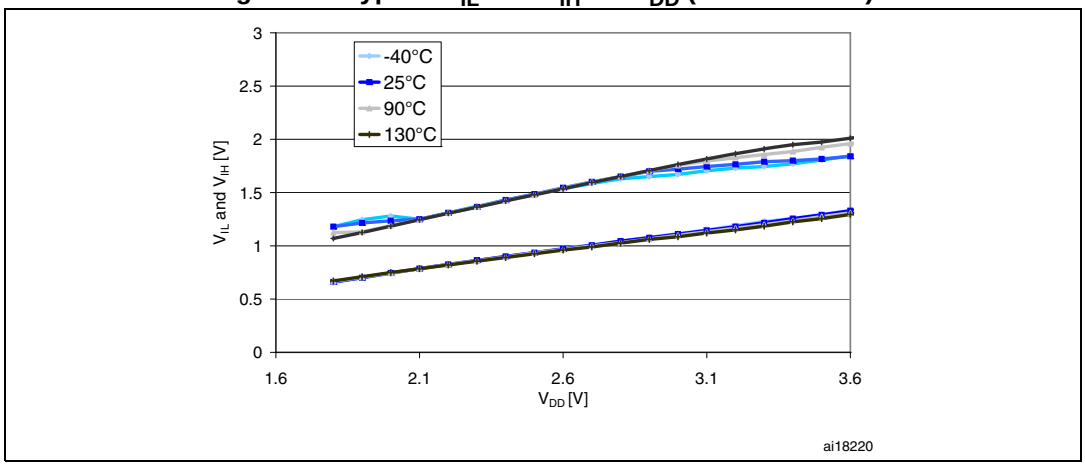


Figure 22. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

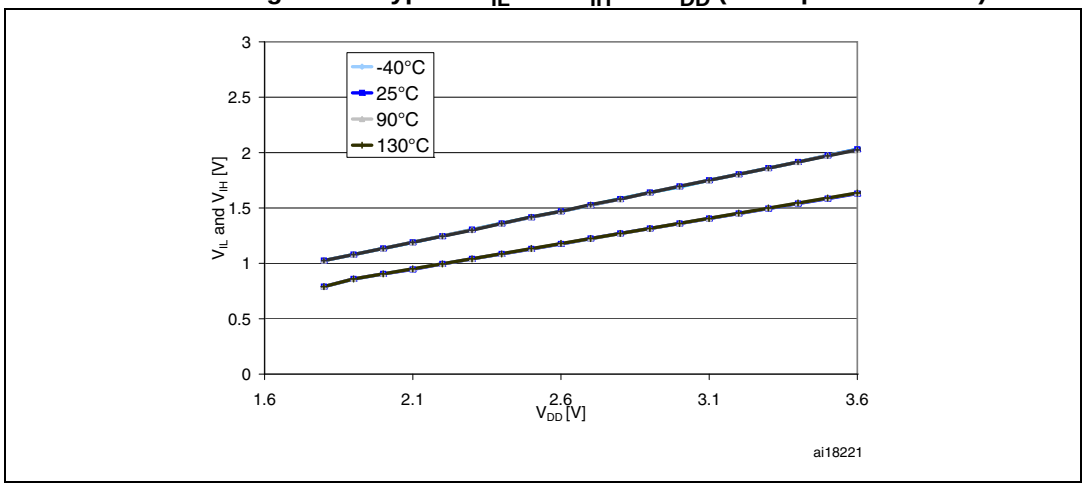
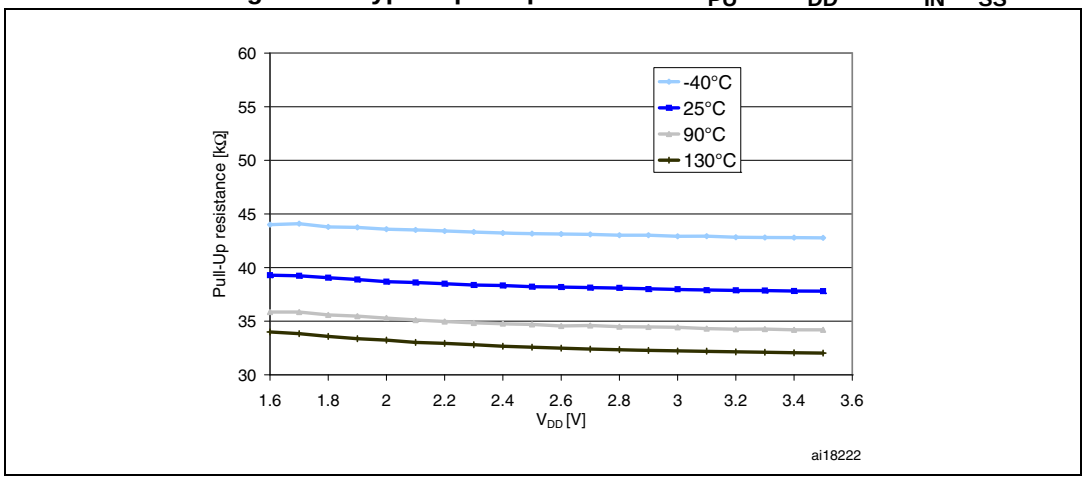


Figure 23. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



9.3.8 Communication interfaces

SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under ambient temperature, f_{SYSCLK} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI1 characteristics

Symbol	Parameter	Conditions(1)	Min.	Max.	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI1 clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI1 clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x $1/f_{SYSCLK}$	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x $1/f_{SYSCLK}$	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min. time is for the minimum time to drive the output and max. time is for the maximum time to validate the data.
4. Min. time is for the minimum time to invalidate the output and max. time is for the maximum time to put the data in Hi-Z.

9.3.11 Temperature sensor

In the following table, data are based on characterization results, not tested in production, unless otherwise specified.

Table 46. TS characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{90} (1)	Sensor reference voltage at 90°C ±5 °C,	0.580	0.597	0.614	V
T_L	V_{SENSOR} linearity with temperature	-	±1	±2	°C
Avg_slope(2)	Average slope	1.59	1.62	1.65	mV/°C
$IDD_{(TEMP)}$(2)	Consumption	-	3.4	6	µA
T_{START}(2)(3)	Temperature sensor startup time	-	-	10	µs
T_{S_TEMP}(2)	ADC sampling time when reading the temperature sensor	-	5	10	µs

1. Tested in production at V_{DD} = 3 V ±10 mV. The 8 LSB of the V_{90} ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Guaranteed by design, not tested in production.
3. Defined for ADC output reaching its final value ±1/2LSB.

9.3.12 Comparator characteristics

In the following tables, data are guaranteed by design, not tested in production.

Table 47. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage		1.65	-	3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Based on characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

Table 52. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(3)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 45*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ..
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

11 Ordering information scheme

Table 63. Ordering information scheme

Example: STM8 L 162 M 8 T 6 D

Device family

STM8 microcontroller

Product type

L = Low-power

Device subfamily

162: STM8L162 device family

Pin count

R = 64 pins

M = 80 pins

Program memory size

8 = 64 Kbytes of Flash memory

Package

T = LQFP

Temperature range

3 = Industrial temperature range, –40 to 125 °C

6 = Industrial temperature range, –40 to 85 °C

Option

Blank = V_{DD} range from 1.8 to 3.6 V and BOR enabled

D = V_{DD} range from 1.65 to 3.6 V and BOR disabled

For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.