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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, IR, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l162r8t6

3.3.3 Voltage regulator

The high-density STM8L162x8 devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low-power voltage regulator mode (LPVR) for Halt, Active-halt, Low-power run and Low-power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE)
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

Table 4. STM8L162x8 pin description (continued)

Pin number		Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
32	28	PD3/ TIM1_ETR/ LCD_SEG9/ADC1_IN19/ COMP1_INP	I/O	FT (3)	**X**	X	X	HS	X	X	**Port D3**	Timer 1 - trigger / LCD segment 9 / ADC1_IN19/Comparator 1 positive input
57	45	PD4/TIM1_CH2/ LCD_SEG18/ADC1_IN10/ COMP1_INP	I/O	FT (3)	**X**	X	X	HS	X	X	**Port D4**	Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/Comparator 1 positive input
58	46	PD5/TIM1_CH3/ LCD_SEG19/ADC1_IN9/ COMP1_INP	I/O	FT (3)	**X**	X	X	HS	X	X	**Port D5**	Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/Comparator 1 positive input
59	47	PD6/TIM1_BKIN/ LCD_SEG20/ADC1_IN8/ RTC_CALIB/COMP1_INP/ VREFINT	I/O	FT (3)	**X**	X	X	HS	X	X	**Port D6**	Timer 1 - break input /LCD segment 20/ADC1_IN8 / RTC calibration/Comparator 1 positive input/Internal reference voltage output
60	48	PD7/TIM1_CH1N/ LCD_SEG21/ADC1_IN7/RTC_ALARM/COMP1_INP/ VREFINT	I/O	FT (3)	**X**	X	X	HS	X	X	**Port D7**	Timer 1 - inverted channel 1/ LCD segment 21/ADC1_IN7/ RTC alarm/Comparator 1 positive input/Internal reference voltage output
61	49	PG4/LCD_SEG32/ SPI2_NSS	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G4**	LCD segment 32 / SPI2 master/slave select
62	50	PG5/LCD_SEG33/ SPI2_SCK	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G5**	LCD segment 33 / SPI2 clock
63	51	PG6/LCD_SEG34/ SPI2_MOSI	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G6**	LCD segment 34 / SPI2 master out- slave in
64	52	PG7/LCD_SEG35/ SPI2_MISO	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G7**	LCD segment 35 / SPI2 master in- slave out
23	-	PE0/LCD_SEG1/ TIM5_CH2	I/O	FT (3)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2
-	19	PE0/LCD_SEG1/ TIM5_CH2/RTC_TAMP1	I/O	FT (3)	**X**	X	X	HS	X	X	**Port E0**	LCD segment 1 /Timer 5 channel 2 / RTC tamper 1
24	-	PE1/TIM1_CH2N/ LCD_SEG2	I/O	FT (3)	**X**	X	X	HS	X	X	**Port E1**	Timer 1 - inverted channel 2 / LCD segment 2

Table 4. STM8L162x8 pin description (continued)

Pin number		Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
80	-	PI3/TIM5_CH1/ *[SPI2_MISO]/[TIM3_CH2]*	I/O	FT (3)	**X**	X	X	HS	X	X	**Port I3**	TIM5 Channel 1 *[SPI2 master in- slave out] [TIM3 channel 2]*
-	39	PF0/ADC1_IN24/ DAC_OUT1 *[USART3_TX]*	I/O		**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit]*
49	-	PF0/ADC1_IN24/ DAC_OUT1/*[USART3_TX] /[SPI1_MISO]*	I/O		**X**	X	X	HS	X	X	**Port F0**	ADC1_IN24 / DAC 1 output/ *[USART3 transmit] [SPI1* master in- slave out*]*
50	-	PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]*	I/O		**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive] [SPI1* master out- slave in*]*
-	40	PF1/ADC1_IN25/ DAC_OUT2/*[USART3_RX]*	I/O		**X**	X	X	HS	X	X	**Port F1**	ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]*
51	-	PF2/ADC1_IN26/ [SPI2_SCK]/ [USART3_SCK]	I/O		**X**	X	X	HS	X	X	**Port F2**	ADC1_IN26 *[SPI2 clock] [USART3 clock]*
52	-	PF3/ADC1_IN27/ [SPI1_NSS]	I/O		**X**	X	X	HS	X	X	**Port F3**	ADC1_IN26 *[SPI1 master/slave select]*
53	41	PF4/LCD_SEG36 /LCD_COM4(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F4**	LCD_SEG36/ LCD COM4(7)
54	42	PF5/LCD_SEG37/ LCD_COM5(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F5**	LCD_SEG37/ LCD COM5(7)
55	43	PF6/LCD_SEG38/ LCD_COM6(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F6**	LCD_SEG38/ LCD COM6(7)
56	44	PF7/LCD_SEG39/ LCD_COM7(7)	I/O	FT (3)	**X**	X	X	HS	X	X	**Port F7**	LCD_SEG39/ LCD COM7(7)
22	18	VLCD	S								LCD booster external capacitor	
15	11	V_{DD1}	S								Digital power supply	
14	10	V_{SS1}									I/O ground	
16	12	V_{DDA}	S								Analog supply voltage	
17	13	V_{REF+}/V_{REF+_DAC}	S								ADC1 and DAC1/2 positive voltage reference	

Table 4. STM8L162x8 pin description (continued)

Pin number		Pin name	Type	I/O level	Input			Output			Main function (after reset)	Default alternate function
LQFP80	LQFP64				floating	wpu	Ext. interrupt	High sink/source	OD	PP		
18	14	PG0/LCD SEG28/ USART3_RX/*[TIM2_BKIN]*	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G0**	LCD segment 28/ USART3 receive / *[Timer 2 - break input]*
19	15	PG1/LCD SEG29/ USART3_TX/*[TIM3_BKIN]*	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G1**	LCD segment 29/ USART3 transmit / *[Timer 3 -break input]*
20	16	PG2/LCD_SEG 30/ USART3_CK	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G2**	LCD segment 30/ USART 3 synchronous clock
21	17	PG3/LCD SEG 31/ *[TIM3_ETR]*	I/O	FT (3)	**X**	X	X	HS	X	X	**Port G3**	LCD segment 31/ *[Timer 3 - trigger]*
33		PH4/USART2_RX	I/O	FT (3)	**X**	X	X	HS	X	X	**Port H4**	USART2 receive
34		PH5/USART2_TX	I/O	FT (3)	**X**	X	X	HS	X	X	**Port H5**	USART2 transmit
35		PH6/USART2_CK/ TIM5_CH1	I/O	FT (3)	**X**	X	X	HS	X	X	**Port H6**	USART2 synchronous clock/Timer 5 - channel 1
36		PH7/TIM5_CH2	I/O	FT (3)	**X**	X	X	HS	X	X	**Port H7**	Timer 5 - channel 2
13	9	V_{SSA}/V_{REF-}	S								Analog ground voltage / ADC1 negative voltage reference	
37	29	V_{DD3}	S								IOs supply voltage	
38	30	V_{SS3}	S								IOs ground voltage	
5	1	PA0(8)/*[USART1_CK]*(2)/ SWIM/BEEP/IR_TIM(9)	I/O		X	**X**	X	HS(9)	X	X	**Port A0**	*[USART1 synchronous clock]*(2) / SWIM input and output / Beep output / Infrared Timer output
68	56	V_{SS2}									IOs ground voltage	
67	55	V_{DD2}									IOs supply voltage	
48	-	V_{SS4}									IOs ground voltage	
47	-	V_{DD4}									IOs supply voltage	

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output open-drain or push-pull, not as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xx and STM8L16xx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. In the 5 V tolerant I/Os, the protection diode to V_{DD} is not implemented.

4. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
5. In the open-drain output column, ‘T’ defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
6. Not in 64-pin version.
7. SEG/COM multiplexing available on medium+ and high-density devices. SEG signals are available by default (see reference manual for details)"
8. The PA0 pin is in input pull-up during the reset phase and after reset release.
9. High Sink LED driver capability available on PA0.

Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

System configuration options

As shown in *Table 4: STM8L162x8 pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the “Routing interface (RI) and system configuration controller” section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	2 Kbytes	0x00 0000	0x00 07FF
	4 Kbytes	0x00 0000	0x00 0FFF
Flash program memory	32 Kbytes	0x00 8000	0x00 FFFF
	64 Kbytes	0x00 8000	0x01 7FFF

5.2 Register map

Table 6. Factory conversion registers

Address	Block	Register label	Register name	Reset status
0x00 4910	-	VREFINT_Factory_CONV(1)	Internal reference voltage factory conversion	0xXX
0x00 4911	-	TS_Factory_CONV_V90(2)	Temperature sensor output voltage	0xXX

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V90 byte represents the 8 LSB of the result of the V90 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

Table 7. I/O port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xXX
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x01
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xXX
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PB_IDR	Port C input pin value register	0xXX
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00

Table 7. I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xXX
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00
0x00 5014	Port E	PE_ODR	Port E data output latch register	0x00
0x00 5015		PE_IDR	Port E input pin value register	0xXX
0x00 5016		PE_DDR	Port E data direction register	0x00
0x00 5017		PE_CR1	Port E control register 1	0x00
0x00 5018		PE_CR2	Port E control register 2	0x00
0x00 5019	Port F	PF_ODR	Port F data output latch register	0x00
0x00 501A		PF_IDR	Port F input pin value register	0xXX
0x00 501B		PF_DDR	Port F data direction register	0x00
0x00 501C		PF_CR1	Port F control register 1	0x00
0x00 501D		PF_CR2	Port F control register 2	0x00
0x00 501E	Port G	PG_ODR	Port F data output latch register	0x00
0x00 501F		PG_IDR	Port G input pin value register	0xXX
0x00 5020		PG_DDR	Port G data direction register	0x00
0x00 5021		PG_CR1	Port G control register 1	0x00
0x00 5022		PG_CR2	Port G control register 2	0x00
0x00 5023	Port H	PH_ODR	Port H data output latch register	0x00
0x00 5024		PH_IDR	Port H input pin value register	0xXX
0x00 5025		PH_DDR	Port H data direction register	0x00
0x00 5026		PH_CR1	Port H control register 1	0x00
0x00 5027		PH_CR2	Port H control register 2	0x00
0x00 5028	Port I	PI_ODR	Port I data output latch register	0x00
0x00 5029		PI_IDR	Port I input pin value register	0xXX
0x00 502A		PI_DDR	Port I data direction register	0x00
0x00 502B		PI_CR1	Port I control register 1	0x00
0x00 502C		PI_CR2	Port I control register 2	0x00

Table 8. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5400	LCD	LCD_CR1	LCD control register 1	0x00
0x00 5401		LCD_CR2	LCD control register 2	0x00
0x00 5402		LCD_CR3	LCD control register 3	0x00
0x00 5403		LCD_FRQ	LCD frequency selection register	0x00
0x00 5404		LCD_PM0	LCD Port mask register 0	0x00
0x00 5405		LCD_PM1	LCD Port mask register 1	0x00
0x00 5406		LCD_PM2	LCD Port mask register 2	0x00
0x00 5407		LCD_PM3	LCD Port mask register 3	0x00
0x00 5408		LCD_PM4	LCD Port mask register 4	0x00
0x00 5409		LCD_PM5	LCD Port mask register 5	0x00
0x00 540A to 0x00 540B	Reserved area (2 bytes)			
0x00 540C	LCD	LCD_RAM0	LCD display memory 0	0x00
0x00 540D		LCD_RAM1	LCD display memory 1	0x00
0x00 540E		LCD_RAM2	LCD display memory 2	0x00
0x00 540F		LCD_RAM3	LCD display memory 3	0x00
0x00 5410		LCD_RAM4	LCD display memory 4	0x00
0x00 5411		LCD_RAM5	LCD display memory 5	0x00
0x00 5412		LCD_RAM6	LCD display memory 6	0x00
0x00 5413		LCD_RAM7	LCD display memory 7	0x00
0x00 5414		LCD_RAM8	LCD display memory 8	0x00
0x00 5415		LCD_RAM9	LCD display memory 9	0x00
0x00 5416		LCD_RAM10	LCD display memory 10	0x00
0x00 5417		LCD_RAM11	LCD display memory 11	0x00
0x00 5418		LCD_RAM12	LCD display memory 12	0x00
0x00 5419		LCD_RAM13	LCD display memory 13	0x00
0x00 541A		LCD_RAM14	LCD display memory 14	0x00
0x00 541B		LCD_RAM15	LCD display memory 15	0x00
0x00 541C		LCD_RAM16	LCD display memory 16	0x00
0x00 541D		LCD_RAM17	LCD display memory 17	0x00
0x00 541E		LCD_RAM18	LCD display memory 18	0x00
0x00 541F		LCD_RAM19	LCD display memory 19	0x00
0x00 5420		LCD_RAM20	LCD display memory 20	0x00
0x00 5421	LCD	LCD_RAM21	LCD display memory 21	0x00

Table 9. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F90	DM	DM_BK1RE	DM breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	DM breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	DM breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	DM breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	DM breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	DM breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	DM Debug module control register 1	0x00
0x00 7F97		DM_CR2	DM Debug module control register 2	0x00
0x00 7F98		DM_CSR1	DM Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	DM Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	DM enable function register	0xFF
0x00 7F9B to 0x00 7F9F	Reserved area (5 bytes)			

1. Accessible by debug module only

8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

Table 13. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4926	X co-ordinate on the wafer	U_ID[7:0]							
0x4927		U_ID[15:8]							
0x4928	Y co-ordinate on the wafer	U_ID[23:16]							
0x4929		U_ID[31:24]							
0x492A	Wafer number	U_ID[39:32]							
0x492B	Lot number	U_ID[47:40]							
0x492C		U_ID[55:48]							
0x492D		U_ID[63:56]							
0x492E		U_ID[71:64]							
0x492F		U_ID[79:72]							
0x4930		U_ID[87:80]							
0x4931		U_ID[95:88]							

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions

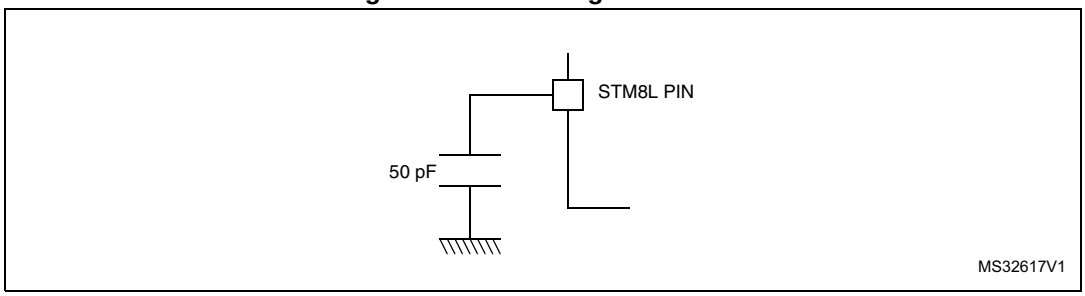
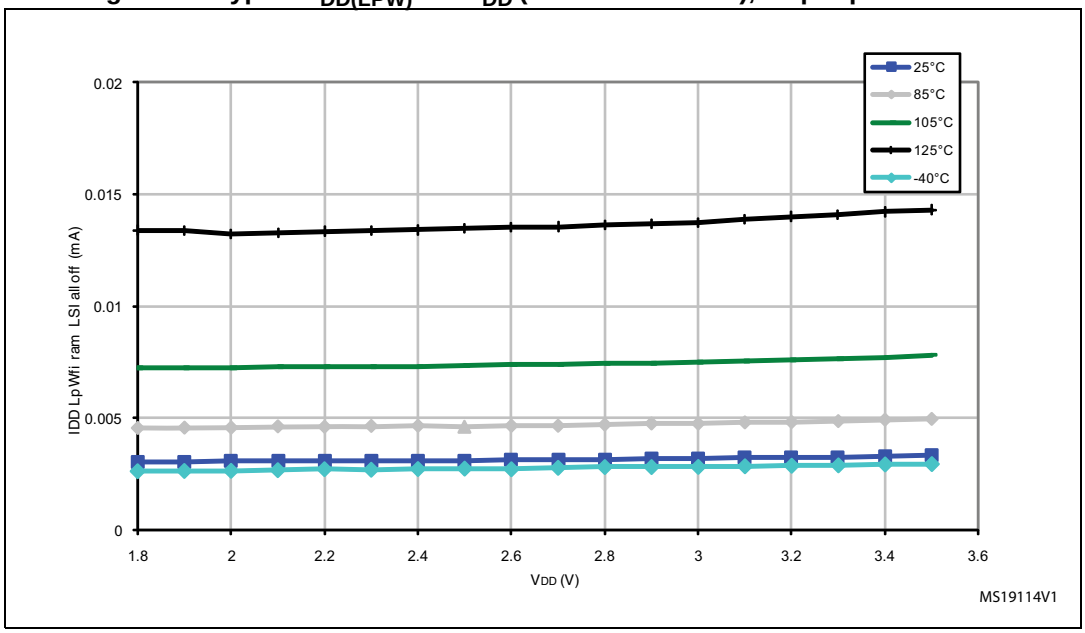


Figure 14. Typical $I_{DD(LPW)}$ vs. V_{DD} (LSI clock source), all peripherals OFF



1. Typical current consumption measured with code executed from RAM.

In the following table, data are based on characterization results, unless otherwise specified.

Table 25. Total current consumption and timing in Halt mode at V_{DD} = 1.65 to 3.6 V

Symbol	Parameter	Condition(1)	Typ.	Max.	Unit
$I_{DD(Halt)}$	Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register)	T_A = -40 °C to 25 °C	400	1600(2)	nA
		T_A = 55 °C	810	2400	
		T_A = 85 °C	1600	4500(2)	
		T_A = 105 °C	2900	7700(2)	
		T_A = 125 °C	5.6	18(2)	µA
$I_{DD(WUHalt)}$	Supply current during wakeup time from Halt mode (using HSI)		2.4		mA
$t_{WU\_HSI(Halt)}$(3)(4)	Wakeup time from Halt to Run mode (using HSI)		4.7	7	µs
$t_{WU\_LSI(Halt)}$ (3)(4)	Wakeup time from Halt mode to Run mode (using LSI)		150		µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after t_{WU}

Figure 16. Typical $I_{DD(Halt)}$ vs. V_{DD} (internal reference voltage OFF)

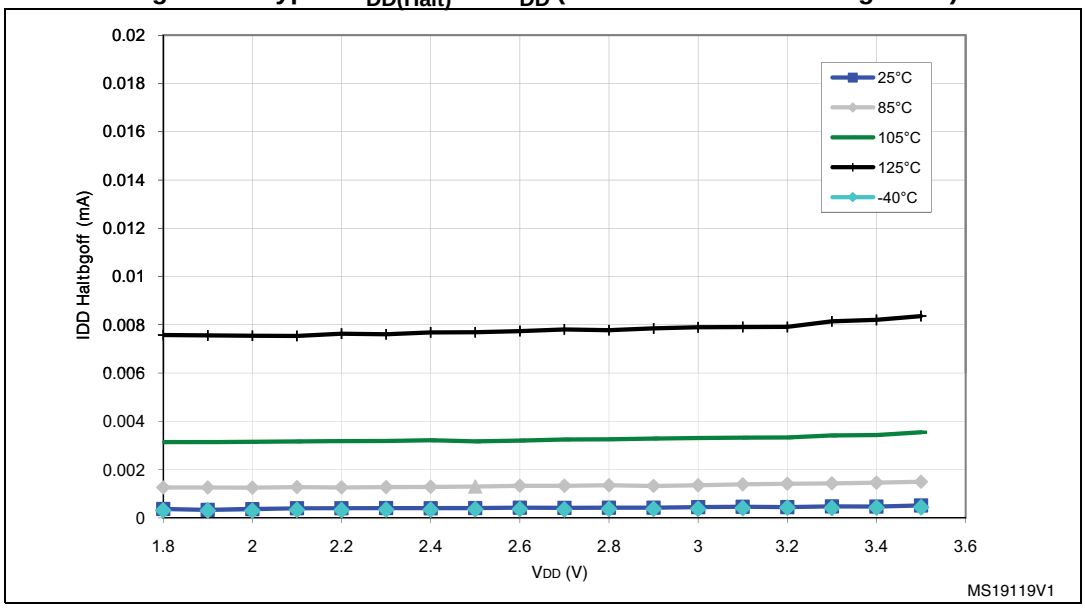
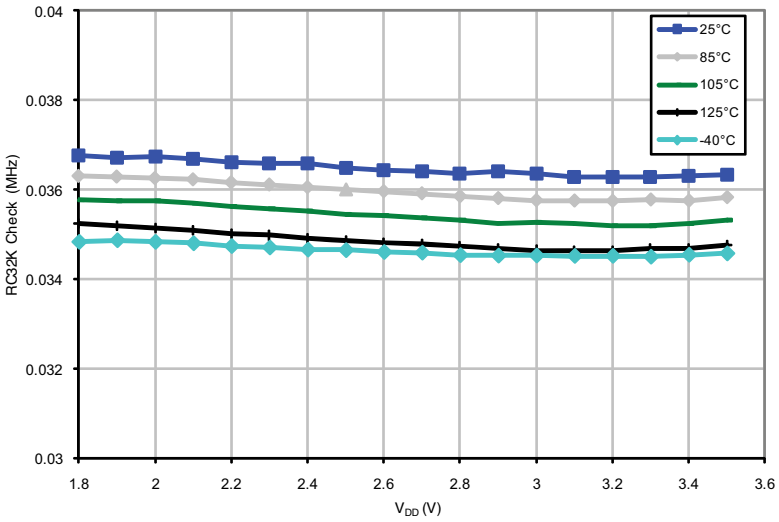


Figure 20. Typical LSI clock source frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 35. Flash program and data EEPROM memory

Symbol	Parameter	Conditions	Min.	Typ.	Max. (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{SYSCLK} = 16 MHz	1.65		3.6	V
t_{prog}	Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1 to 128 bytes (block) write cycles (on erased byte)	-	-	3	-	
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET} (2)	Data retention (program memory) after 10000 erase/write cycles at T_A=–40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	years
	Data retention (program memory) after 10000 erase/write cycles at T_A=–40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=–40 to +85 °C (6 suffix)	T_{RET}=+85 °C	30(1)	-	-	
	Data retention (data memory) after 300000 erase/write cycles at T_A=–40 to +125 °C (3 suffix)	T_{RET}=+125 °C	5(1)	-	-	
N_{RW} (3)	Erase/write cycles (program memory)	T_A=–40 to +85 °C (6 suffix), T_A=–40 to +105 °C (7 suffix) or T_A=–40 to +125 °C (3 suffix)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)		300(1) (4)	-	-	

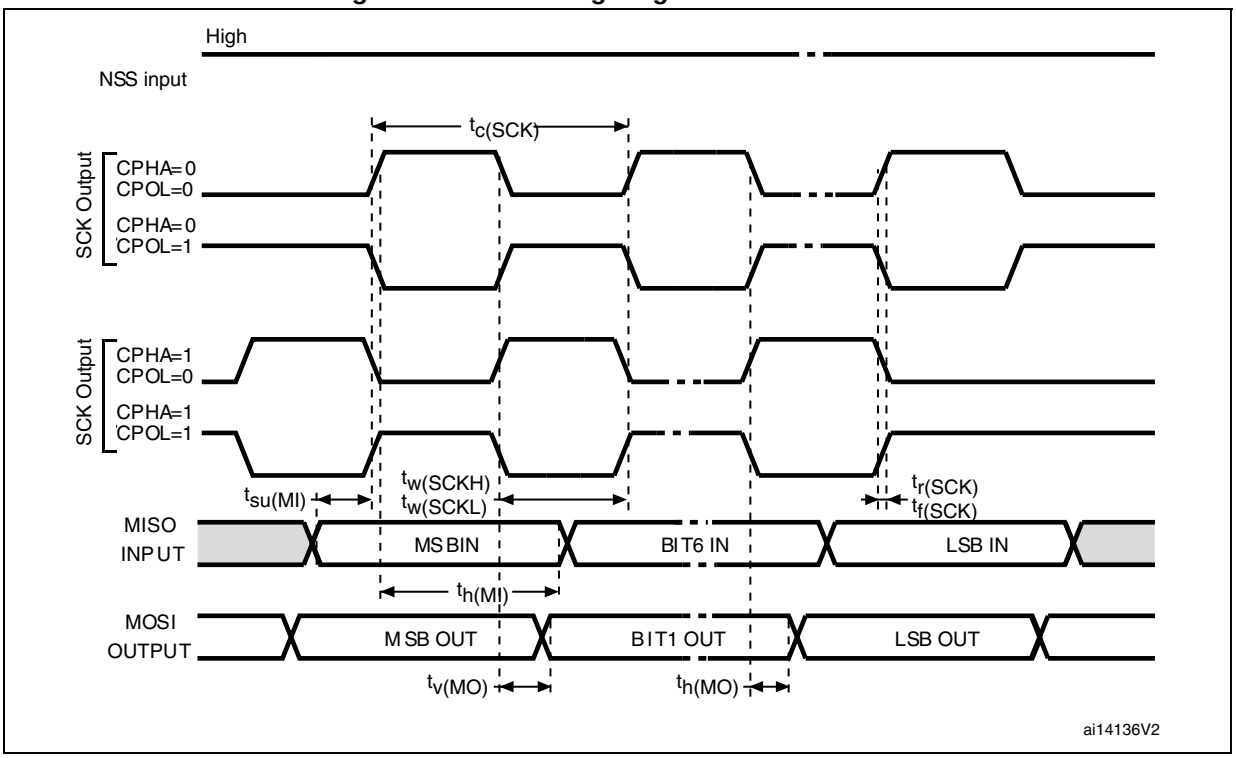
1. Data based on characterization results, not tested in production.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

Table 37. I/O static characteristics

Symbol	Parameter	Conditions(1)	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage(2)	Input voltage on true open-drain pins (PC0 and PC1)	V_{SS}-0.3	-	0.3 x V_{DD}	V
		Input voltage on five-volt tolerant (FT) pins	V_{SS}-0.3	-	0.3 x V_{DD}	
		Input voltage on any other pin	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Input voltage on true open-drain pins (PC0 and PC1) with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	V
		Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on five-volt tolerant (FT) pins with V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V		-	5.5	
		Input voltage on any other pin	0.70 x V_{DD}	-	V_{DD}+0.3	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	200	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(2)(6)	$V_{IN}=V_{SS}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 24*).

Figure 36. SPI1 timing diagram - master mode



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

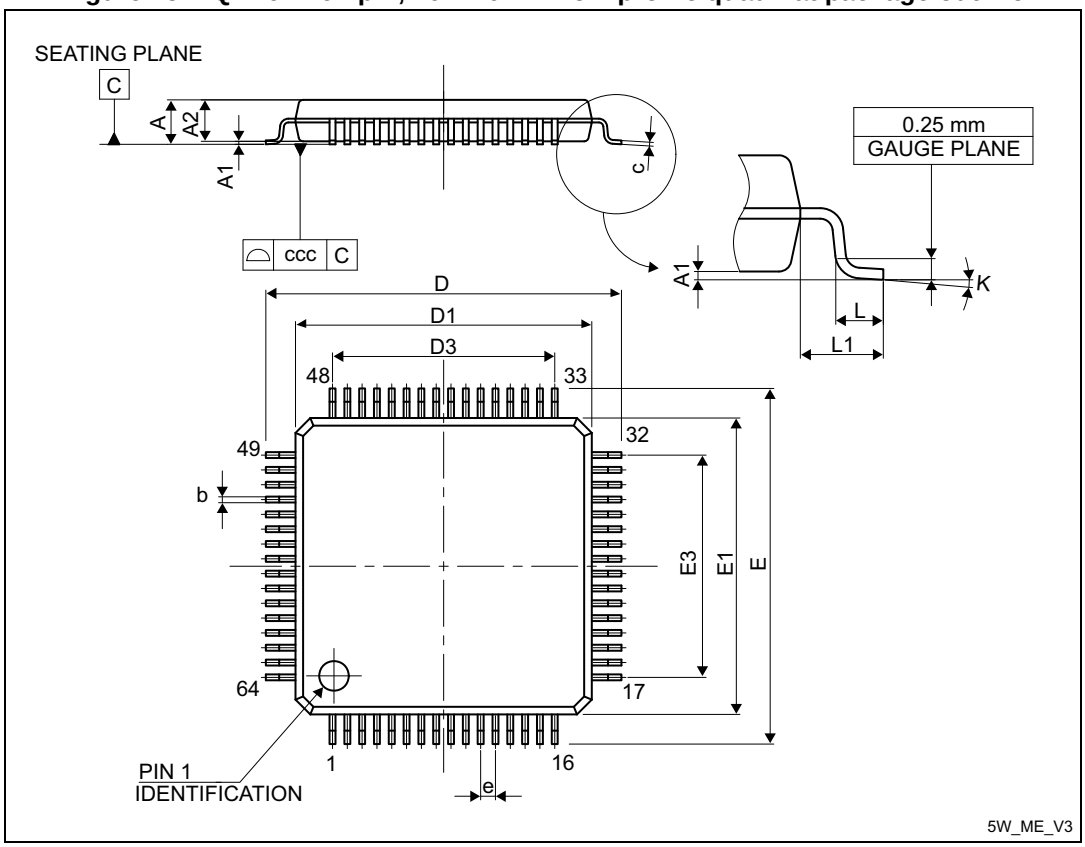
Table 52. ADC1 characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_S	Sampling time	V_{AIN} PF0/1/2/3 fast channels V_{DDA} < 2.4 V	0.43(3)(4)	-	-	µs
		V_{AIN} PF0/1/2/3 fast channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.22(3)(4)	-	-	
		V_{AIN} on slow channels V_{DDA} < 2.4 V	0.86(3)(4)	-	-	
		V_{AIN} on slow channels 2.4 V ≤ V_{DDA}≤ 3.6 V	0.41(3)(4)	-	-	
t_{conv}	12-bit conversion time	-	12 + t_S			$1/f_{ADC}$
		16 MHz	1(3)			µs
t_{WKUP}	Wakeup time from OFF state	-	-	-	3	µs
t_{IDLE}(5)	Time before a new conversion	-	-	-	∞	s
$t_{VREFINT}$	Internal reference voltage startup time	-	-	-	refer to *Table 45*	ms

1. The current consumption through V_{REF} is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. V_{REF-} must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum R_{AIN}= 0.5 kΩ..
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than t_{IDLE}.

10.2 LQFP64 package information

Figure 45. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 62. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

12 Revision history

Table 64. Document revision history

Date	Revision	Changes
14-Sep-2010	1	Initial release.
22-Mar-2011	2	*Table 4: STM8L162x8 pin description*: updated “standard port” changed to “high sink port”. *Figure 5: Memory map*: updated the address range of the AES registers. *Table 8: General hardware register map*: updated the address range of the AES registers. *Table 14: Voltage characteristics*: updated *Table 15: Current characteristics*: updated *Table 34: RAM and hardware registers*: updated VRM data min. retention. Added *Table 9.3.6: I/O current injection characteristics*. *Table 37: I/O static characteristics*: updated *Table 44: LCD characteristics*: updated