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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f276-ceg-p-tr

configured in order to send an acknowledge frame. The ST10F276E will not send this Message Object but the host can request it by sending a remote frame.

The acknowledge frame is the following for the ST10F276E:

- Standard identifier = E6h
- DLC = 3h
- Data0 = D5h, that is, generic acknowledge of the ST10 devices
- Data1 = IDCHIP least significant byte
- Data2 = IDCHIP most significant byte

For the ST10F276E, IDCHIP = 114Xh.

Note: Two behaviors can be distinguished in ST10 acknowledging to the host. If the host is behaving according to the CAN protocol, as at the beginning the ST10 CAN is not configured, the host is alone on the CAN network and does not receive an acknowledge. It automatically resends the zero frame. As soon as the ST10 CAN is configured, it acknowledges the zero frame. The "acknowledge frame" with identifier 0xE6 is configured, but the Transmit Request is not set. The host can request this frame to be sent and therefore obtains the IDCHIP by sending a remote frame.

Hint: As the IDCHIP is sent in the acknowledge frame, Flash programming software now can immediately identify the exact type of device to be programmed.

Table 32. BRP and PT0 values

BRP	PT0_min	PT0_max	Comments
0	464	1450	
1	1451	2900	
2	2901	4350	
3	4351	5800	
4	5801	7250	
5	7251	8700	
..	..	..	
43	20416	63800	
44	20880	65250	
45	21344	66700	Possible timer overflow
..	..	..	
63	X	X	

The error coming from the measurement of the 29 bit is:

$$e_1 = 6 / [PT0]$$

It is maximal for the smallest BRP value and the smallest number of ticks in PT0. Therefore:

$$e_{1\ Max} = 1.29\%$$

To improve precision, the aim is to have the smallest BRP so that the time quantum is the smallest possible. Thus, an error on the calculation of time quanta in a bit time is minimal.

In order to do so, the value of PT0 is divided into ranges of 1450 ticks. In the algorithm, PT0 is divided by 1451 and the result is BRP.

The calculated BRP value is then used to divide PT0 in order to have the value of *(1 + Tseg1 + Tseg2)*. A table is made to set the values for *Tseg1* and *Tseg2* according to the value of *(1 + Tseg1 + Tseg2)*. These values of *Tseg1* and *Tseg2* are chosen in order to reach a sample point between 70% and 80% of the bit time.

During the calculation of *(1 + Tseg1 + Tseg2)*, an error e_2 can be introduced by the division. This error is of 1 time quantum maximum.

To compensate for any possible error on bit rate, the (Re)Synchronization Jump Width is fixed to 2 time quanta.

12 Parallel ports

12.1 Introduction

The ST10F276E MCU provides up to 111 I/O lines with programmable features. These capabilities bring very flexible adaptation of this MCU to wide range of applications.

ST10F276E has nine groups of I/O lines gathered as follows:

- Port 0 is a two time 8-bit port named P0L (Low as less significant byte) and P0H (high as most significant byte)
- Port 1 is a two time 8-bit port named P1L and P1H
- Port 2 is a 16-bit port
- Port 3 is a 15-bit port (P3.14 line is not implemented)
- Port 4 is a 8-bit port
- Port 5 is a 16-bit port input only
- Port 6, Port 7 and Port 8 are 8-bit ports

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example, the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bit-wise) for push-pull or open drain operation using ODPx registers.

The input threshold levels are programmable (TTL/CMOS) for all the ports. The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with PICON and XPICON registers control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

Writing to a pin configured as an output (DPx.y='1') causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

12.2 I/O's special features

12.2.1 Open drain mode

Some of the I/O ports of ST10F276E support the open drain capability. This programmable feature may be used with an external pull-up resistor, in order to get an AND wired logical function.

This feature is implemented for ports P2, P3, P4, P6, P7 and P8 (see respective sections), and is controlled through the respective Open Drain Control Registers ODPx.

14 Serial channels

Serial communication with other microcontrollers, microprocessors, terminals or external peripheral components is provided by up to four serial interfaces: two asynchronous / synchronous serial channels (ASC0 and ASC1) and two high-speed synchronous serial channel (SSC0 and SSC1). Dedicated Baud rate generators set up all standard Baud rates without the requirement of oscillator tuning. For transmission, reception and erroneous reception, separate interrupt vectors are provided for ASC0 and SSC0 serial channel. A more complex mechanism of interrupt sources multiplexing is implemented for ASC1 and SSC1 (XBUS mapped).

14.1 Asynchronous / synchronous serial interfaces

The asynchronous / synchronous serial interfaces (ASC0 and ASC1) provides serial communication between the ST10F276E and other microcontrollers, microprocessors or external peripherals.

14.2 ASCx in asynchronous mode

In asynchronous mode, 8- or 9-bit data transfer, parity generation and the number of stop bits can be selected. Parity framing and overrun error detection is provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. Full-duplex communication up to 2M bauds (at 64 MHz of f_{CPU}) is supported in this mode.

Table 52. ASC asynchronous baud rates by reload value and deviation errors (f_{CPU} = 40 MHz)

S0BRS = '0', f_{CPU} = 40 MHz			S0BRS = '1', f_{CPU} = 40 MHz		
Baud rate (baud)	**Deviation error**	**Reload value (hex)**	**Baud rate (baud)**	**Deviation error**	**Reload value (hex)**
1 250 000	0.0% / 0.0%	0000 / 0000	833 333	0.0% / 0.0%	0000 / 0000
112 000	+1.5% / -7.0%	000A / 000B	112 000	+6.3% / -7.0%	0006 / 0007
56 000	+1.5% / -3.0%	0015 / 0016	56 000	+6.3% / -0.8%	000D / 000E
38 400	+1.7% / -1.4%	001F / 0020	38 400	+3.3% / -1.4%	0014 / 0015
19 200	+0.2% / -1.4%	0040 / 0041	19 200	+0.9% / -1.4%	002A / 002B
9 600	+0.2% / -0.6%	0081 / 0082	9 600	+0.9% / -0.2%	0055 / 0056
4 800	+0.2% / -0.2%	0103 / 0104	4 800	+0.4% / -0.2%	00AC / 00AD
2 400	+0.2% / 0.0%	0207 / 0208	2 400	+0.1% / -0.2%	015A / 015B
1 200	0.1% / 0.0%	0410 / 0411	1 200	+0.1% / -0.1%	02B5 / 02B6
600	0.0% / 0.0%	0822 / 0823	600	+0.1% / 0.0%	056B / 056C
300	0.0% / 0.0%	1045 / 1046	300	0.0% / 0.0%	0AD8 / 0AD9
153	0.0% / 0.0%	1FE8 / 1FE9	102	0.0% / 0.0%	1FE8 / 1FE9

Table 54. ASC synchronous baud rates by reload value and deviation errors (f_{CPU} = 40 MHz)

S0BRS = '0', f_{CPU} = 40 MHz			S0BRS = '1', f_{CPU} = 40 MHz		
Baud rate (baud)	Deviation error	Reload value (hex)	Baud rate (baud)	Deviation error	Reload value (hex)
900	0.0% / 0.0%	15B2 / 15B3	600	0.0% / 0.0%	15B2 / 15B3
612	0.0% / 0.0%	1FE8 / 1FE9	407	0.0% / 0.0%	1FFD / 1FFE

Table 55. ASC synchronous baud rates by reload value and deviation errors (f_{CPU} = 64 MHz)

S0BRS = '0', f_{CPU} = 64 MHz			S0BRS = '1', f_{CPU} = 64 MHz		
Baud rate (baud)	Deviation error	Reload value (hex)	Baud rate (baud)	Deviation error	Reload value (hex)
8 000 000	0.0% / 0.0%	0000 / 0000	5 333 333	0.0% / 0.0%	0000 / 0000
112 000	+0.6% / -0.8%	0046 / 0047	112 000	+1.3% / -0.8%	002E / 002F
56 000	+0.6% / -0.1%	008D / 008E	56 000	+0.3% / -0.8%	005E / 005F
38 400	+0.2% / -0.3%	00CF / 00D0	38 400	+0.6% / -0.1%	0089 / 008A
19 200	+0.2% / -0.1%	019F / 01A0	19 200	+0.3% / -0.1%	0114 / 0115
9 600	+0.0% / -0.1%	0340 / 0341	9 600	+0.1% / -0.1%	022A / 022B
4 800	0.0% / 0.0%	0681 / 0682	4 800	0.0% / -0.1%	0456 / 0457
2 400	0.0% / 0.0%	0D04 / 0D05	2 400	0.0% / 0.0%	08AD / 08AE
1 200	0.0% / 0.0%	1A09 / 1A0A	1 200	0.0% / 0.0%	115B / 115C
977	0.0% / 0.0%	1FFB / 1FFC	900	0.0% / 0.0%	1724 / 1725
			652	0.0% / 0.0%	1FF2 / 1FF3

Note: The deviation errors given in the Table 54 and Table 55 are rounded. To avoid deviation errors use a Baud rate crystal (providing a multiple of the ASC0 sampling frequency)

14.4 High speed synchronous serial interfaces

The High-Speed Synchronous Serial Interfaces (SSC0 and SSC1) provides flexible high-speed serial communication between the ST10F276E and other microcontrollers, microprocessors or external peripherals.

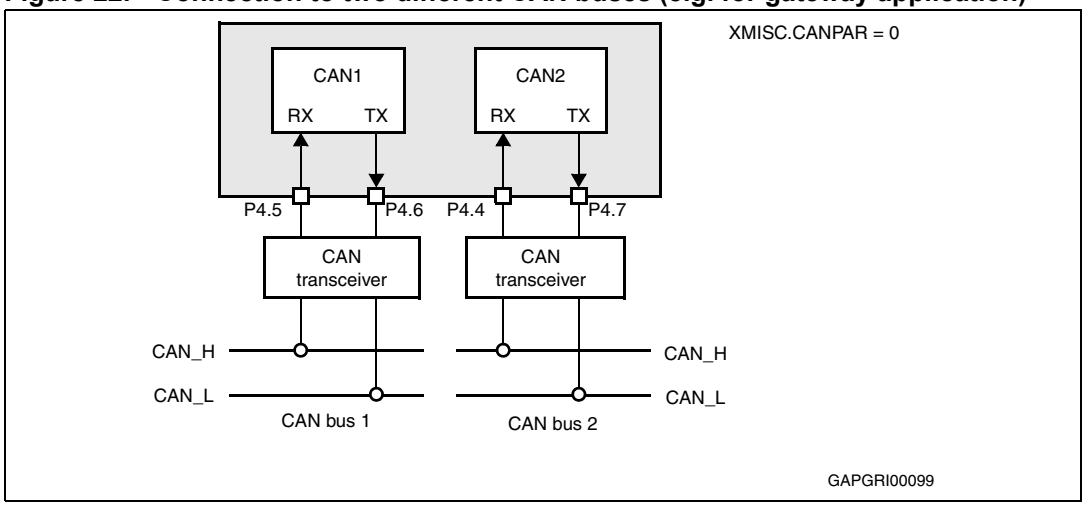
The SSCx supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSCx itself (master mode) or be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable.

This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A 16-bit Baud rate generator provides the SSCx with a separate serial clock signal. The serial channel SSCx has its own dedicated 16-bit Baud rate generator with 16-bit reload capability, allowing Baud rate generation independent from the timers.

Multiple CAN bus

The ST10F276E provides two CAN interfaces to support such kind of bus configuration as shown in *Figure 22*.

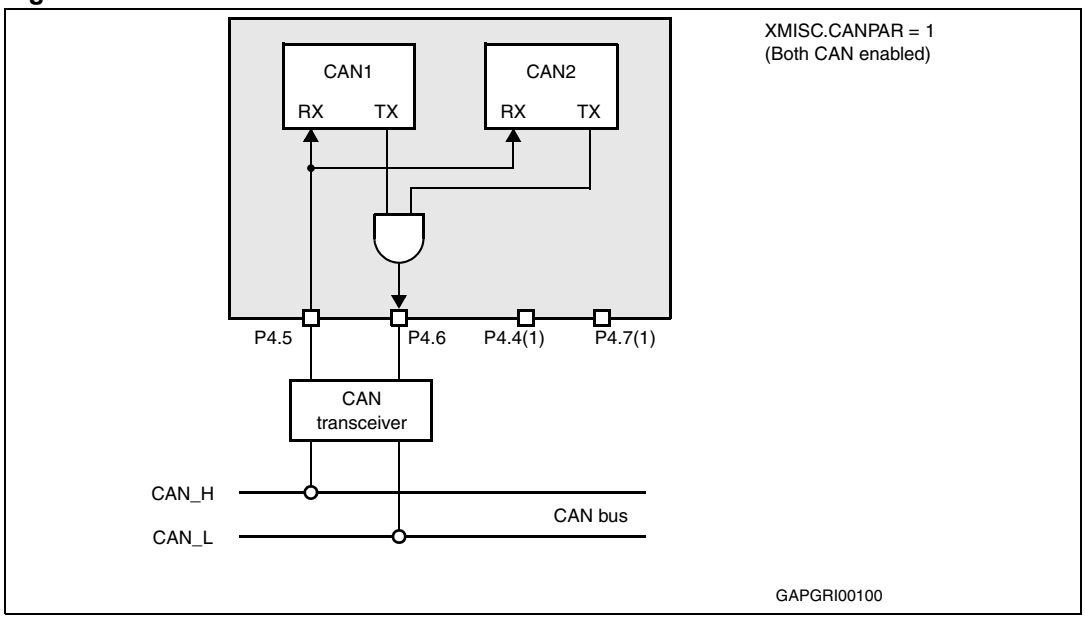
Figure 22. Connection to two different CAN buses (e.g. for gateway application)



Parallel Mode

In addition to previous configurations, a parallel mode is supported. This is shown in *Figure 23*.

Figure 23. Connection to one CAN bus with internal Parallel Mode enabled



1. P4.4 and P4.7 when not used as CAN functions can be used as general purpose I/O while they cannot be used as external bus address lines.

18 Watchdog timer

The Watchdog Timer is a fail-safe mechanism which prevents the microcontroller from malfunctioning for long periods of time.

The Watchdog Timer is always enabled after a reset of the chip and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed.

Therefore, the chip start-up procedure is always monitored. The software must be designed to service the watchdog timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the watchdog timer overflows and generates an internal hardware reset. It pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

Each of the different reset sources is indicated in the WDTCON register:

- Watchdog Timer Reset in case of an overflow
- Software Reset in case of execution of the SRST instruction
- Short, Long and Power-On Reset in case of hardware reset (and depending of reset pulse duration and RPD pin configuration)

The indicated bits are cleared with the EINIT instruction. The source of the reset can be identified during the initialization phase.

The Watchdog Timer is 16-bit, clocked with the system clock divided by 2 or 128. The high Byte of the watchdog timer register can be set to a pre-specified reload value (stored in WDTREL).

Each time it is serviced by the application software, the high byte of the watchdog timer is reloaded. For security, rewrite WDTCON each time before the watchdog timer is serviced

Table 58 and *Table 59* show the watchdog time range for 40 MHz and 64 MHz CPU clock respectively.

Table 58. WDTREL reload value (f_{CPU} = 40 MHz)

Reload value in WDTREL	Prescaler for f_{CPU} = 40 MHz	
	2 (WDTIN = '0')	128 (WDTIN = '1')
FFh	12.8µs	819.2µs
00h	3.277ms	209.7ms

Table 59. WDTREL reload value (f_{CPU} = 64 MHz)

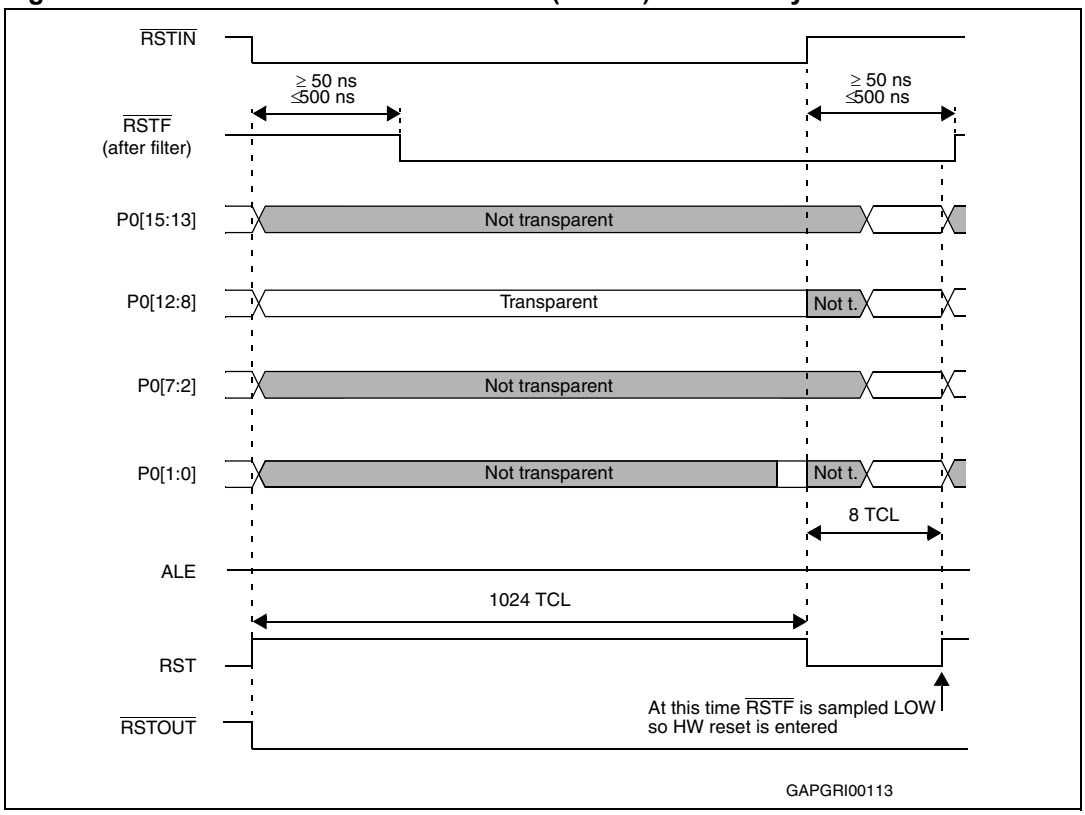
Reload value in WDTREL	Prescaler for f_{CPU} = 64 MHz	
	2 (WDTIN = '0')	128 (WDTIN = '1')
FFh	8µs	512µs
00h	2.048ms	131.1ms

sufficient: anyway, a maximum of 100nF on V_{18} pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is anyway recommended also to avoid risks of damage in case of temporary short between V_{18} and ground: the internal 1.8V drivers are sized to drive currents of several tens of Ampere, so the current shall be limited by the external hardware. The limit of current is imposed by power dissipation considerations (Refer to *Chapter 23: Electrical characteristics*).

In next figures *24* and *25* Asynchronous Power-on timing diagrams are reported, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded Flash module when selected.

Note: Never power the device without keeping $\overline{RSTIN}$ pin grounded: the device could enter in unpredictable states, risking also permanent damages.

Figure 36. SW / WDT bidirectional RESET ($\overline{EA}$ = 0) followed by a HW RESET



19.7 Reset circuitry

Internal reset circuitry is described in *Figure 39*. The $\overline{RSTIN}$ pin provides an internal pull-up resistor of 50kΩ to 250kΩ (The minimum reset time must be calculated using the lowest value).

It also provides a programmable (BDRSTEN bit of SYSCON register) pull-down to output internal reset state signal (synchronous reset, watchdog timer reset or software reset).

This bidirectional reset function is useful in applications where external devices require a reset signal but cannot be connected to $\overline{RSTOUT}$ pin.

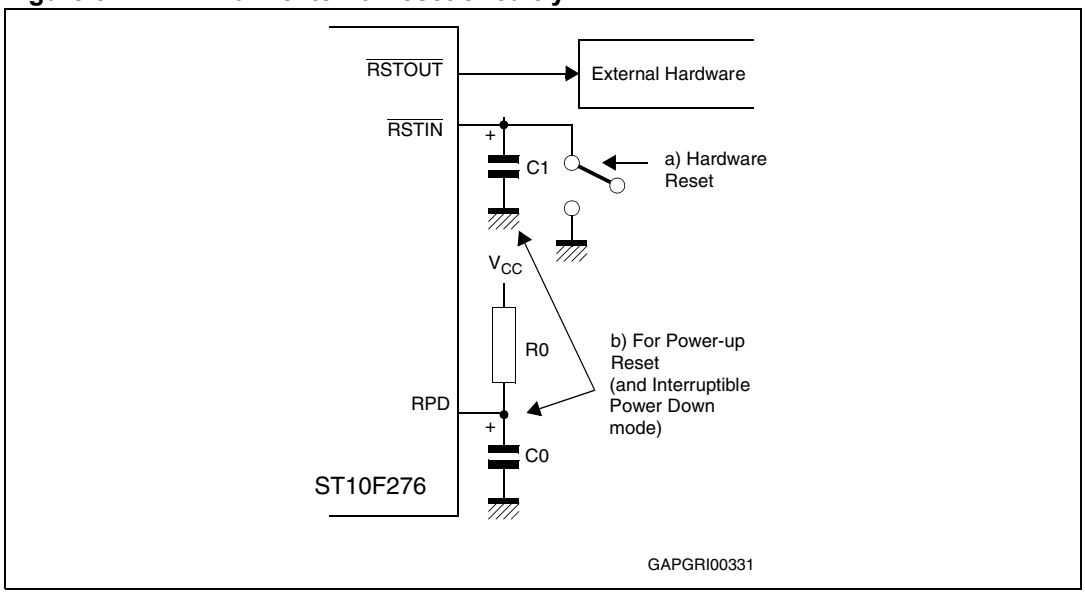
This is the case of an external memory running codes before EINIT (end of initialization) instruction is executed. $\overline{RSTOUT}$ pin is pulled high only when EINIT is executed.

The RPD pin provides an internal weak pull-down resistor which discharges external capacitor at a typical rate of 200µA. If bit PWDCFG of SYSCON register is set, an internal pull-up resistor is activated at the end of the reset sequence. This pull-up will charge any capacitor connected on RPD pin.

The simplest way to reset the ST10F276E is to insert a capacitor C1 between $\overline{RSTIN}$ pin and V_{SS}, and a capacitor between RPD pin and V_{SS} (C0) with a pull-up resistor R0 between RPD pin and V_{DD}. The input $\overline{RSTIN}$ provides an internal pull-up device equalling a resistor of 50kΩ to 250kΩ (the minimum reset time must be determined by the lowest value). Select C1 that produce a sufficient discharge time to permit the internal or external oscillator and / or internal PLL and the on-chip voltage regulator to stabilize.

To ensure correct power-up reset with controlled supply current consumption, specially if clock signal requires a long period of time to stabilize, an asynchronous hardware reset is required during power-up. For this reason, it is recommended to connect the external R0-C0 circuit shown in *Figure 37* to the RPD pin. On power-up, the logical low level on RPD pin forces an asynchronous hardware reset when $\overline{\text{RSTIN}}$ is asserted low. The external pull-up R0 will then charge the capacitor C0. Note that an internal pull-down device on RPD pin is turned on when $\overline{\text{RSTIN}}$ pin is low, and causes the external capacitor (C0) to begin discharging at a typical rate of 100-200µA. With this mechanism, after power-up reset, short low pulses applied on $\overline{\text{RSTIN}}$ produce synchronous hardware reset. If $\overline{\text{RSTIN}}$ is asserted longer than the time needed for C0 to be discharged by the internal pull-down device, then the device is forced in an asynchronous reset. This mechanism insures recovery from very catastrophic failure.

Figure 37. Minimum external reset circuitry



The minimum reset circuit of *Figure 37* is not adequate when the $\overline{\text{RSTIN}}$ pin is driven from the ST10F276E itself during software or watchdog triggered resets, because of the capacitor C1 that will keep the voltage on $\overline{\text{RSTIN}}$ pin above V_{IL} after the end of the internal reset sequence, and thus will trigger an asynchronous reset sequence.

Figure 38 shows an example of a reset circuit. In this example, R1-C1 external circuit is only used to generate power-up or manual reset, and R0-C0 circuit on RPD is used for power-up reset and to exit from Power Down mode. Diode D1 creates a wired-OR gate connection to the reset pin and may be replaced by open-collector Schmitt trigger buffer. Diode D2 provides a faster cycle time for repetitive power-on resets.

R2 is an optional pull-up for faster recovery and correct biasing of TTL Open Collector drivers.

Table 67. Special function registers ordered by address (continued)

Name	Physical address	8-bit address	Description	Reset value
CC15	FE9Eh	4Fh	CAPCOM register 15	0000h
CC15IC **b**	FF96h	CBh	CAPCOM register 15 interrupt control register	- - 00h
CC16	FE60h	30h	CAPCOM register 16	0000h
CC16IC **b**	F160h**E**	B0h	CAPCOM register 16 interrupt control register	- - 00h
CC17	FE62h	31h	CAPCOM register 17	0000h
CC17IC **b**	F162h**E**	B1h	CAPCOM register 17 interrupt control register	- - 00h
CC18	FE64h	32h	CAPCOM register 18	0000h
CC18IC **b**	F164h**E**	B2h	CAPCOM register 18 interrupt control register	- - 00h
CC19	FE66h	33h	CAPCOM register 19	0000h
CC19IC **b**	F166h**E**	B3h	CAPCOM register 19 interrupt control register	- - 00h
CC1IC **b**	FF7Ah	BDh	CAPCOM register 1 interrupt control register	- - 00h
CC2	FE84h	42h	CAPCOM register 2	0000h
CC20	FE68h	34h	CAPCOM register 20	0000h
CC20IC **b**	F168h**E**	B4h	CAPCOM register 20 interrupt control register	- - 00h
CC21	FE6Ah	35h	CAPCOM register 21	0000h
CC21IC **b**	F16Ah**E**	B5h	CAPCOM register 21 interrupt control register	- - 00h
CC22	FE6Ch	36h	CAPCOM register 22	0000h
CC22IC **b**	F16Ch**E**	B6h	CAPCOM register 22 interrupt control register	- - 00h
CC23	FE6Eh	37h	CAPCOM register 23	0000h
CC23IC **b**	F16Eh**E**	B7h	CAPCOM register 23 interrupt control register	- - 00h
CC24	FE70h	38h	CAPCOM register 24	0000h
CC24IC **b**	F170h**E**	B8h	CAPCOM register 24 interrupt control register	- - 00h
CC25	FE72h	39h	CAPCOM register 25	0000h
CC25IC **b**	F172h**E**	B9h	CAPCOM register 25 interrupt control register	- - 00h
CC26	FE74h	3Ah	CAPCOM register 26	0000h
CC26IC **b**	F174h**E**	BAh	CAPCOM register 26 interrupt control register	- - 00h
CC27	FE76h	3Bh	CAPCOM register 27	0000h
CC27IC **b**	F176h**E**	BBh	CAPCOM register 27 interrupt control register	- - 00h
CC28	FE78h	3Ch	CAPCOM register 28	0000h
CC28IC **b**	F178h**E**	BCh	CAPCOM register 28 interrupt control register	- - 00h
CC29	FE7Ah	3Dh	CAPCOM register 29	0000h
CC29IC **b**	F184h**E**	C2h	CAPCOM register 29 interrupt control register	- - 00h
CC2IC **b**	FF7Ch	BEh	CAPCOM register 2 interrupt control register	- - 00h
CC3	FE86h	43h	CAPCOM register 3	0000h

Table 69. X-Registers ordered by name (continued)

Name	Physical address	Description	Reset value
CAN1IF1M2	EF16h	CAN1: IF1 mask 2	FFFFh
CAN1IF1MC	EF1Ch	CAN1: IF1 message control	0000h
CAN1IF2A1	EF48h	CAN1: IF2 arbitration 1	0000h
CAN1IF2A2	EF4Ah	CAN1: IF2 arbitration 2	0000h
CAN1IF2CM	EF42h	CAN1: IF2 command mask	0000h
CAN1IF2CR	EF40h	CAN1: IF2 command request	0001h
CAN1IF2DA1	EF4Eh	CAN1: IF2 data A 1	0000h
CAN1IF2DA2	EF50h	CAN1: IF2 data A 2	0000h
CAN1IF2DB1	EF52h	CAN1: IF2 data B 1	0000h
CAN1IF2DB2	EF54h	CAN1: IF2 data B 2	0000h
CAN1IF2M1	EF44h	CAN1: IF2 mask 1	FFFFh
CAN1IF2M2	EF46h	CAN1: IF2 mask 2	FFFFh
CAN1IF2MC	EF4Ch	CAN1: IF2 message control	0000h
CAN1IP1	EFA0h	CAN1: interrupt pending 1	0000h
CAN1IP2	EFA2h	CAN1: interrupt pending 2	0000h
CAN1IR	EF08h	CAN1: interrupt register	0000h
CAN1MV1	EFB0h	CAN1: Message valid 1	0000h
CAN1MV2	EFB2h	CAN1: Message valid 2	0000h
CAN1ND1	EF90h	CAN1: New data 1	0000h
CAN1ND2	EF92h	CAN1: New data 2	0000h
CAN1SR	EF02h	CAN1: Status register	0000h
CAN1TR	EF0Ah	CAN1: Test register	00x0h
CAN1TR1	EF80h	CAN1: Transmission request 1	0000h
CAN1TR2	EF82h	CAN1: Transmission request 2	0000h
CAN2BRPER	EE0Ch	CAN2: BRP extension register	0000h
CAN2BTR	EE06h	CAN2: Bit timing register	2301h
CAN2CR	EE00h	CAN2: CAN control register	0001h
CAN2EC	EE04h	CAN2: Error counter	0000h
CAN2IF1A1	EE18h	CAN2: IF1 arbitration 1	0000h
CAN2IF1A2	EE1Ah	CAN2: IF1 arbitration 2	0000h
CAN2IF1CM	EE12h	CAN2: IF1 command mask	0000h
CAN2IF1CR	EE10h	CAN2: IF1 command request	0001h
CAN2IF1DA1	EE1Eh	CAN2: IF1 data A 1	0000h
CAN2IF1DA2	EE20h	CAN2: IF1 data A 2	0000h

Table 75. IDMEM description

Bit	Function
MEMSIZE	Internal memory size Internal memory size is 4 x (MEMSIZE) (in Kbyte) 0D0h for ST10F276E (832 Kbytes)
MEMTYP	Internal memory type 0h: ROM-Less 1h: (M) ROM memory 2h: (S) Standard Flash memory 3h: (H) High performance Flash memory (ST10F276E) 4h...Fh: *Reserved*

IDPROG (F078h / 3Ch) ESFR Reset value:0040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

Table 76. IDPROG description

Bit	Function
PROGVDD	Programming VDD voltage VDD voltage when programming EPROM or Flash devices is calculated using the following formula: VDD = 20 x [PROGVDD] / 256 (volts) - 40h for ST10F276E (5V).
PROGVPP	Programming VPP voltage (no need of external VPP) - 00h

Note: All identification words are read-only registers.

The values written inside different Identification Register bits are valid only after the Flash initialization phase is completed. When code execution is started from internal memory (pin $\overline{EA}$ held high during reset), the Flash has completed its initialization, so the bits of Identification Registers are immediately ready to be read out. On the contrary, when code execution is started from external memory (pin $\overline{EA}$ held low during reset), the Flash initialization is not yet completed, so the bits of Identification Registers are not ready. The user can poll bits 15 and 14 of IDMEM register: When both bits are read low, the Flash initialization is complete, so all Identification Register bits are correct.

Before Flash initialization completion, the default setting of the different identification registers are the following:

IDMANUF	0403h
IDCHIP	114xh (x = silicon revision)
IDMEM	F0D0h
IDPROG	0040h

Note: 1 BTYP (bit 6 and 7) is set according to the configuration of the bit I6 and I7 of PORT0 latched at the end of the reset sequence.

2 BUSCON0 is initialized with 0000h, if $\overline{EA}$ pin is high during reset. If $\overline{EA}$ pin is low during reset, bit BUSACT0 and ALECTRL0 are set ('1') and bit field BTYP is loaded with the bus configuration selected via PORT0.

RP0H (F108h / 84h) ESFR Reset value: --XXh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-								CLKSEL			SALSEL		CSSEL		WRC
								R			R		R		R

Table 79. RPOH description(1)

Bit	Function
WRC(2)	Write configuration control 0: Pin $\overline{WR}$ acts as $\overline{WRL}$, pin $\overline{BHE}$ acts as $\overline{WRH}$ 1: Pins $\overline{WR}$ and $\overline{BHE}$ retain their normal function
CSSEL(2)	Chip select line selection (number of active $\overline{CS}$ outputs) 00: 3 $\overline{CS}$ lines: $\overline{CS}$2...$\overline{CS}$0 01: 2 $\overline{CS}$ lines: $\overline{CS}$1...$\overline{CS}$0 10: No $\overline{CS}$ line at all 11: 5 $\overline{CS}$ lines: $\overline{CS}$4...$\overline{CS}$0 (Default without pull-downs)
SALSEL(2)	Segment address line selection (number of active segment address outputs) 00: 4-bit segment address: A19...A16 01: No segment address lines at all 10: 8-bit segment address: A23...A16 11: 2-bit segment address: A17...A16 (Default without pull-downs)
CLKSEL(2)(3)	System clock selection 000: $f_{CPU} = 16 \times f_{OSC}$ 001: $f_{CPU} = 0.5 \times f_{OSC}$ 010: $f_{CPU} = 10 \times f_{OSC}$ 011: $f_{CPU} = f_{OSC}$ 100: $f_{CPU} = 5 \times f_{OSC}$ 101: $f_{CPU} = 8 \times f_{OSC}$ 110: $f_{CPU} = 3 \times f_{OSC}$ 111: $f_{CPU} = 4 \times f_{OSC}$

1. RP0H is a read-only register.
2. These bits are set according to Port 0 configuration during any reset sequence.
3. RP0H.7 to RP0H.5 bits are loaded only during a long hardware reset. As pull-up resistors are active on each Port P0H pins during reset, RP0H default value is "FFh".

EXICON (F1C0h / E0h) ESFR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXI7ES		EXI6ES		EXI5ES		EXI4ES		EXI3ES		EXI2ES		EXI1ES		EXI0ES	
RW		RW		RW		RW		RW		RW		RW		RW	

Table 90. DC characteristics (continued)

Symbol	Parameter	Test condition	Limit values		Unit
			Min.	Max.	
I_{ALEH}	ALE active current(6)(8)	V_{OUT} = 2.4 V	-	300	µA
I_{P6H}	Port 6 inactive current (P6[4:0])(6)(7)	V_{OUT} = 2.4 V	-	-40	µA
I_{P6L}	Port 6 active current (P6[4:0])(6)(8)	V_{OUT} = 0.4V	-500	-	µA
I_{P0H}(6)	PORT0 configuration current(6)	V_{IN} = 2.0V	-	-10	µA
I_{P0L}(7)		V_{IN} = 0.8V	-100	-	µA
C_{IO} **CC**	Pin capacitance (digital inputs / outputs)	(4)(6)	-	10	pF
I_{CC1}	Run mode power supply current(9) (execution from internal RAM)	-	-	20 + 2 f_{CPU}	mA
I_{CC2}	Run mode power supply current(4)(10) (execution from internal Flash)	-	-	20 + 1.8 f_{CPU}	mA
I_{ID}	Idle mode supply current (11)	-	-	20 + 0.6 f_{CPU}	mA
I_{PD1}	Power Down supply current (12) (RTC off, oscillators off, main voltage regulator off)	T_A = 25°C	-	1	mA
I_{PD2}	Power Down supply current (12) (RTC on, main oscillator on, main voltage regulator off)	T_A = 25°C	-	8	mA
I_{PD3}	Power down supply current (12) (RTC on, 32 kHz oscillator on, main voltage regulator off)	T_A = 25°C	-	1.1	mA
I_{SB1}	Stand-by supply current (12) (RTC off, Oscillators off, VDD off, VSTBY on)	V_{STBY} = 5.5V $T_A = T_J$ = 25°C	-	250	µA
		V_{STBY} = 5.5V $T_A = T_J$ = 125°C	-	500	µA
I_{SB2}	Stand-by supply current (12) (RTC on, 32 kHz Oscillator on, main VDD off, VSTBY on)	V_{STBY} = 5.5V T_A = 25°C	-	250	µA
		V_{STBY} = 5.5V T_A = 125°C	-	500	µA
I_{SB3}	Stand-by supply current (4) (12) (VDD transient condition)	-	-	2.5	mA

1. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output floats and the voltage is imposed by the external circuitry.
2. Port 5 leakage values are granted for not selected A/D converter channel. One channels is always selected (by default, after reset, P5.0 is selected). For the selected channel the leakage value is similar to that of other port pins.
3. The leakage of P2.0 is higher than other pins due to the additional logic (pass gates active only in specific test modes) implemented on input path. Pay attention to not stress P2.0 input pin with negative overload beyond the specified limits: Failures in Flash reading may occur (sense amplifier perturbation). Refer to *Figure 44* for a scheme of the input circuitry.
4. Not 100% tested, guaranteed by design characterization.
5. Overload conditions occur if the standard operating conditions are exceeded, that is, the voltage on any pin exceeds the specified range (that is, $V_{OV} > V_{DD} + 0.3V$ or $V_{OV} < -0.3V$). The absolute sum of input overload currents on all port pins may not exceed 50mA. The supply voltage must remain within the specified limits.

23.7 A/D converter characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C, 4.5V ≤ V_{AREF} ≤ V_{DD},
V_{SS} ≤ V_{AGND} ≤ V_{SS} + 0.2V

Table 93. A/D converter characteristics

Symbol		Parameter	Test condition	Limit values		Unit
				Min.	Max.	
V_{AREF}	**SR**	Analog reference voltage(1)		4.5	V_{DD}	V
V_{AGND}	**SR**	Analog ground voltage		V_{SS}	V_{SS} + 0.2	V
V_{AIN}	**SR**	Analog Input voltage(2)		V_{AGND}	V_{AREF}	V
I_{AREF}	**CC**	Reference supply current	Running mode(3) Power Down mode	- -	5 1	mA µA
t_S	**CC**	Sample time	(4)	1	-	µs
t_C	**CC**	Conversion time	(5)	3	-	µs
DNL	**CC**	Differential nonlinearity(6)	No overload	-1	+1	LSB
INL	**CC**	Integral nonlinearity(6)	No overload	-1.5	+1.5	LSB
OFS	**CC**	Offset error(6)	No overload	-1.5	+1.5	LSB
TUE	**CC**	Total unadjusted error(6)	Port5 Port1 - No overload(3) Port1 - Overload(3)	-2.0 -5.0 -7.0	+2.0 +5.0 +7.0	LSB LSB LSB
K	**CC**	Coupling factor between inputs(3)(7)	On both Port5 and Port1	-	10^{-6}	-
C_{P1}	**CC**	Input pin capacitance(3)(8)		-	3	pF
C_{P2}	**CC**		Port5 Port1	-	4 6	pF pF
C_S	**CC**	Sampling capacitance(3)(8)		-	3.5	pF
R_{SW}	**CC**	Analog switch resistance(3)(8)	Port5 Port1	- -	600 1600	Ω Ω
R_{AD}	**CC**			-	1300	Ω

1. V_{AREF} can be tied to ground when A/D converter is not in use: An extra consumption (around 200µA) on main V_{DD} is added due to internal analog circuitry not completely turned off. Therefore, it is suggested to maintain the V_{AREF} at V_{DD} level even when not in use, and eventually switch off the A/D converter circuitry setting bit ADOFF in ADCON register.
2. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $0x000_H$ or $0x3FF_H$, respectively.
3. Not 100% tested, guaranteed by design characterization.
4. During the sample time, the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.
   Values for the sample clock t_S depend on programming and can be taken from *Table 94*.
5. This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result. Values for the conversion clock t_{CC} depend on programming and can be taken from next *Table 94*.

23.8.2 Definition of internal timing

The internal operation of the ST10F276E is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL”.

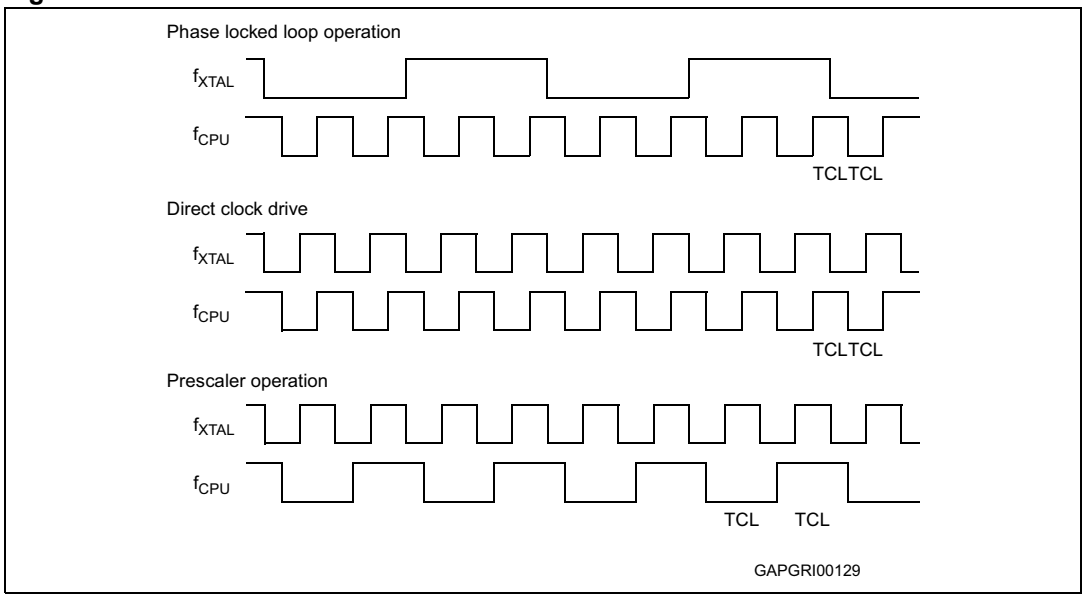
The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}.

This influence must be regarded when calculating the timings for the ST10F276E.

The example for PLL operation shown in *Figure 52* refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

Figure 52. Generation mechanisms for the CPU clock



23.8.12 PLL lock/unlock

During normal operation, if the PLL is unlocked for any reason, an interrupt request to the CPU is generated and the reference clock (oscillator) is automatically disconnected from the PLL input: In this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency F_{free}). This feature allows to recover from a crystal failure occurrence without risking to go into an undefined configuration: The system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between the reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the $\overline{RSTIN}$ pin low.

Note: The external RC circuit on $\overline{RSTIN}$ pin must be the right size in order to extend the duration of the low pulse to grant the PLL to be locked before the level at $\overline{RSTIN}$ pin is recognized high: Bidirectional reset internally drives $\overline{RSTIN}$ pin low for just 1024 TCL (definitely not sufficient to get the PLL locked starting from free-running mode).

Conditions: V_{DD} = 5V ±10%, T_A = -40 / +125°C

Table 97. PLL lock/unlock timing

Symbol	Parameter	Conditions	Value		Unit
			Min.	Max.	
T_{PSUP}	PLL Start-up time (1)	Stable V_{DD} and reference clock	-	300	µs
T_{LOCK}	PLL Lock-in time	Stable V_{DD} and reference clock, starting from free-running mode	-	250	
T_{JIT}	Single Period Jitter (1) (cycle to cycle = 2 TCL)	6 sigma time period variation (peak to peak)	-500	+500	ps
F_{free}	PLL free running frequency	Multiplication factors: 3, 4 Multiplication factors: 5, 8, 10, 16	250 500	2000 4000	kHz

1. Not 100% tested, guaranteed by design characterization.

23.8.13 Main oscillator specifications

Conditions: V_{DD} = 5V ±10%, T_A = -40 / +125°C

Table 98. Main oscillator specifications

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_m	Oscillator transconductance		8	17	35	mA/V
V_{OSC}	Oscillation amplitude(1)	Peak to peak	-	V_{DD} - 0.4	-	V
V_{AV}	Oscillation-voltage level(1)	Sine wave middle	-	V_{DD} / 2 -0.25	-	
t_{STUP}	Oscillator start-up time(1)	Stable V_{DD} - crystal	-	3	4	ms
		Stable V_{DD}, resonator	-	2	3	

1. Not 100% tested, guaranteed by design characterization

Figure 64. Demultiplexed bus, no R/W delay, extended ALE, R/W CS

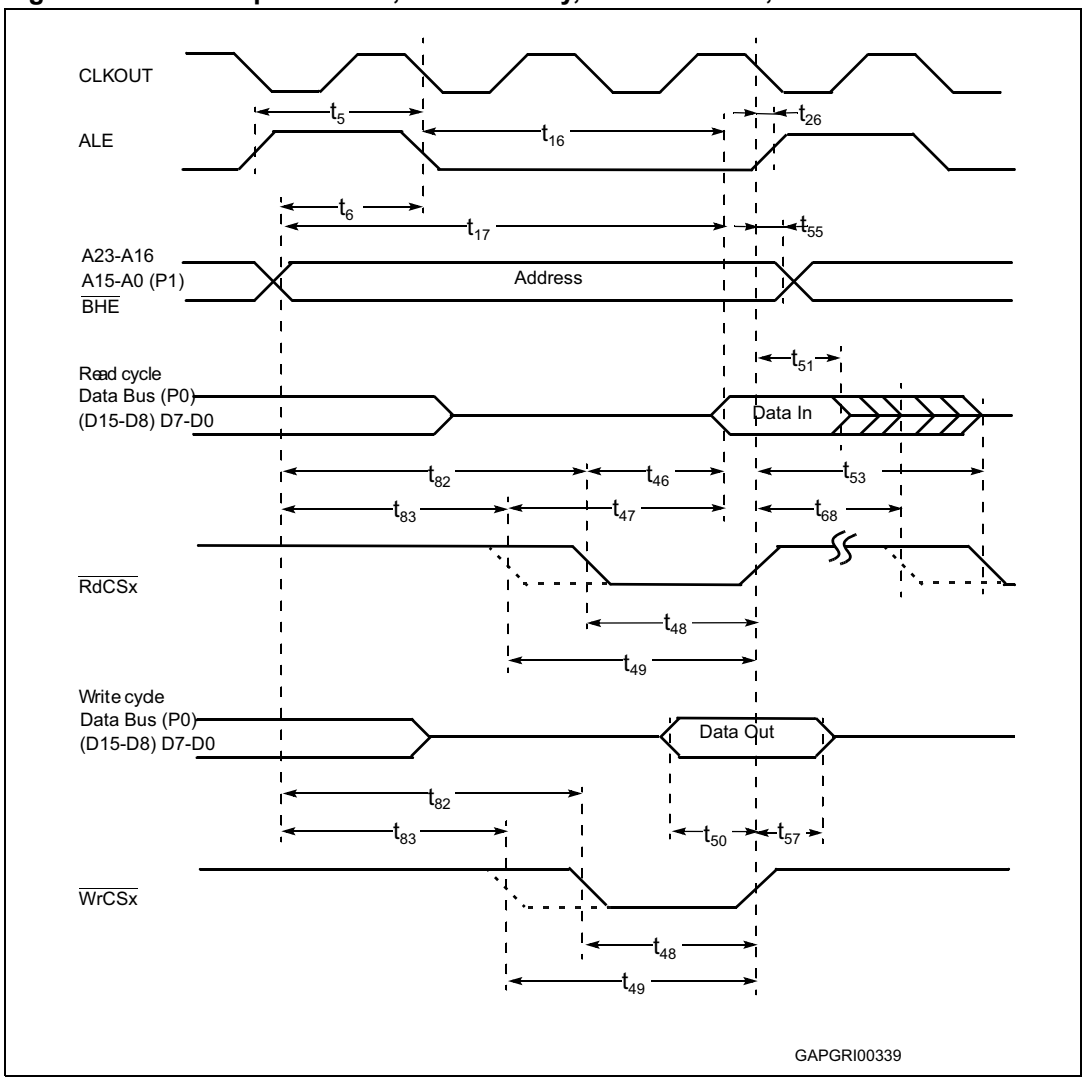
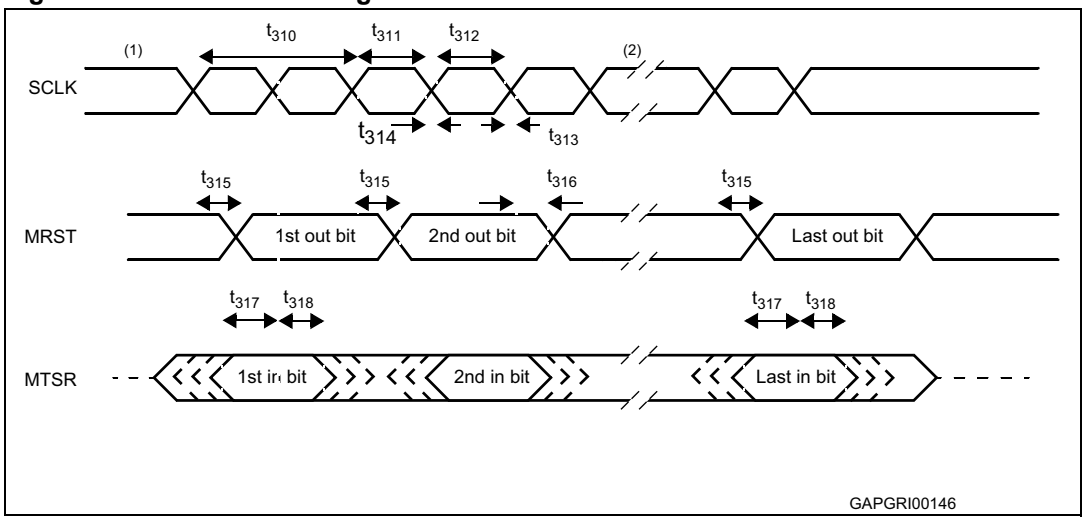


Figure 69. SSC slave timing



1. The phase and polarity of shift and latch edge of SCLK is programmable. This figure uses the leading clock edge as shift edge (drawn in bold), with latch on trailing edge (SSCPH = 0b), idle clock line is low, leading clock edge is low-to-high transition (SSCPO = 0b).
2. The bit timing is repeated for all bits to be transmitted or received.