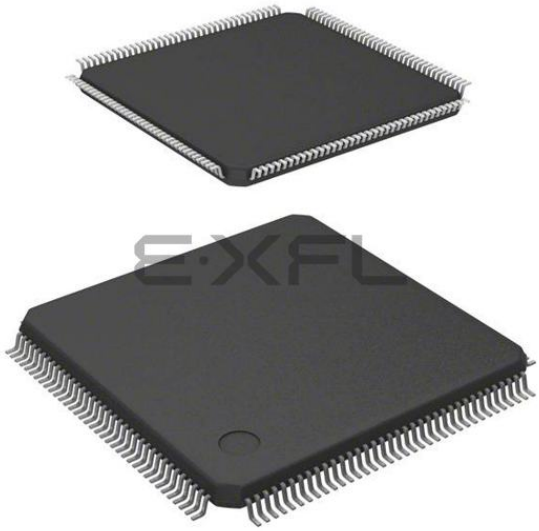

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	48MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f276-4tr3

Table 5. Control register interface

Bank	Description	Addresses	Size	ST10 bus size
FCR1-0	Flash control registers 1-0	0x000E 0000 - 0x000E 0007	8 byte	16-bit (X-BUS)
FDR1-0	Flash data registers 1-0	0x000E 0008 - 0x000E 000F	8 byte	
FAR	Flash address registers	0x000E 0010 - 0x000E 0013	4 byte	
FER	Flash error register	0x000E 0014 - 0x000E 0015	2 byte	
FNVWPXR	Flash non-volatile protection X register	0x000E DFB0 - 0x000E DFB3	4 byte	
FNVWPIR	Flash non-volatile protection I register	0x000E DFB4 - 0x000E DFB7	4 byte	
FNVAPR0	Flash non-volatile access protection register 0	0x000E DFB8 - 0x000E DFB9	2 byte	
FNVAPR1	Flash non-volatile access protection register 1	0x000E DFBC - 0x000E DFBF	4 byte	
XFICR	XFlash interface control register	0x000E E000 - 0x000E E001	2 byte	

4.2.3 Low power mode

The Flash modules are automatically switched off executing PWRDN instruction. The consumption is drastically reduced, but exiting this state can require a long time (t_{PD}).

Note: Recovery time from Power Down mode for the Flash modules is anyway shorter than the main oscillator start-up time. To avoid any problem in restarting to fetch code from the Flash, it is important to size properly the external circuit on RPD pin.

Power-off Flash mode is entered only at the end of the eventually running Flash write operation.

4.2.4 Write operation

The Flash modules have one single register interface mapped in the memory space of the XFlash module (0x0E 0000 to 0x0E 0013). All the operations are enabled through four 16-bit control registers: Flash Control Register 1-0 High/Low (FCR1H/L-FCR0H/L). Eight other 16-bit registers are used to store Flash Address and Data for Program operations (FARH/L and FDR1H/L-FDR0H/L) and Write Operation Error flags (FERH/L). All registers are accessible with 8 and 16-bit instructions (since mapped on ST10 XBUS).

Note: Before accessing the XFlash module (and consequently also the Flash register to be used for program/erasing operations), bit XFLASHEN in XPERCON register and bit XPEN in SYSCON register shall be set.

The four banks have their own dedicated sense amplifiers, so that any bank can be read while any other bank is written. However simultaneous write operations (“write” means either Program or Erase) on different banks are forbidden: when there is a write operation on going (Program or Erase) anywhere in the Flash, no other write operation can be performed.

During a Flash write operation any attempt to read the bank under modification will output invalid data (software trap 009Bh). This means that the Flash bank is not fetchable when a

4.4.8 Flash non-volatile access protection register 1 high

FNVAPR1H (0x0E DFBE) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9	PEN8	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 25. Flash non-volatile access protection register 1 high

Bit	Function
PEN15-0	Protections Enable 15-0 If bit PENx is programmed at 0 and bit PDSx+1 is erased at 1, the action of bit ACCP is enabled again. Bit PENx can be programmed at 0 only if bit PDSx has already been programmed at 0.

4.4.9 Access protection

The Flash modules have one level of access protection (access to data both in Reading and Writing): if bit ACCP of FNVAPR0 is programmed at 0, the IFlash module become access protected: data in the IFlash module can be read/written only if the current execution is from the IFlash module itself.

Protection can be permanently disabled by programming bit PDS0 of FNVAPR1H, in order to analyze rejects. Allowing PDS0 bit programming only when ACCP bit is programmed, guarantees that only an execution from the Flash itself can disable the protections.

Protection can be permanently enabled again by programming bit PEN0 of FNVAPR1L. The action to disable and enable again Access Protections in a permanent way can be executed a maximum of 16 times.

Trying to write into the access protected Flash from internal RAM will be unsuccessful. Trying to read into the access protected Flash from internal RAM will output a dummy data.

When the Flash module is protected in access, also the data access through PEC of a peripheral is forbidden. To read/write data in PEC mode from/to a protected bank, first it is necessary to temporary unprotect the Flash module.

Due to ST10 architecture, the XFLASH is seen as external memory: this makes impossible to access protect it from real external memory or internal RAM. *Table 26* summarizes all levels of possible Access protection: in particular, supposing to enable all possible access protections, when fetching from a memory as listed in the first column, what is possible and what is not possible to do (see column headers) is shown in the table.

Table 26. Summary of access protection level

Memory fetch source	Read IFLASH/ Jump to IFLASH	Read XFLASH/ Jump to XFLASH	Read FLASH Registers	Write FLASH Registers
Fetching from IFLASH	Yes / Yes	Yes / Yes	Yes	Yes
Fetching from XFLASH	No / Yes	Yes / Yes	Yes	No
Fetching from IRAM	No / Yes	Yes / Yes	Yes	No

Table 27. Flash write operations (continued)

Operation	Select bit	Address and data	Start bit
Set Protection	SPR	FDR0L/FDR0H	WMS
Program/Erase Suspend	SUSP	None	None

6.1 Multiplier-accumulator unit (MAC)

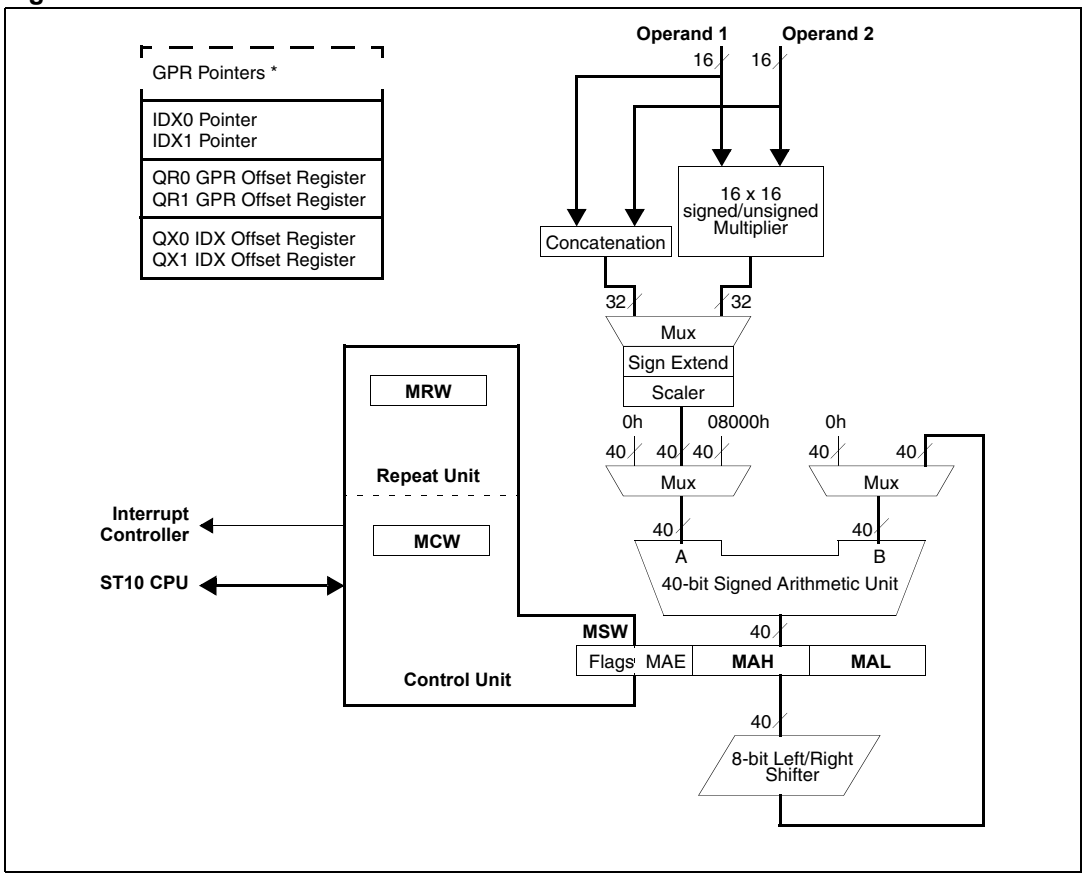
The MAC coprocessor is a specialized coprocessor added to the ST10 CPU Core in order to improve the performances of the ST10 Family in signal processing algorithms.

The standard ST10 CPU has been modified to include new addressing capabilities which enable the CPU to supply the new coprocessor with up to 2 operands per instruction cycle.

This new coprocessor (so-called MAC) contains a fast multiply-accumulate unit and a repeat unit.

The coprocessor instructions extend the ST10 CPU instruction set with multiply, multiply-accumulate, 32-bit signed arithmetic operations.

Figure 15. MAC unit architecture



13 A/D converter

A 10-bit A/D converter with 16+8 multiplexed input channels and a sample and hold circuit is integrated on-chip. An automatic self-calibration adjusts the A/D converter module to process parameter variations at each reset event. The sample time (for loading the capacitors) and the conversion time is programmable and can be adjusted to the external circuitry.

The ST10F276E has 16+8 multiplexed input channels on Port 5 and Port 1. The selection between Port 5 and Port 1 is made via a bit in a XBus register. Refer to the user manual for a detailed description.

A different accuracy is guaranteed (Total Unadjusted Error) on Port 5 and Port 1 analog channels (with higher restrictions when overload conditions occur); in particular, Port 5 channels are more accurate than the Port 1 ones. Refer to *Chapter 23: Electrical characteristics* for details.

The A/D converter input bandwidth is limited by the achievable accuracy: supposing a maximum error of 0.5 LSB (2mV) impacting the global TUE (TUE depends also on other causes), in worst case of temperature and process, the maximum frequency for a sine wave analog signal is around 7.5 kHz. Of course, to reduce the effect of the input signal variation on the accuracy down to 0.05 LSB, the maximum input frequency of the sine wave shall be reduced to 800 Hz.

If static signal is applied during sampling phase, series resistance shall not be greater than 20kΩ (this taking into account eventual input leakage). It is suggested to not connect any capacitance on analog input pins, in order to reduce the effect of charge partitioning (and consequent voltage drop error) between the external and the internal capacitance: in case an RC filter is necessary the external capacitance must be greater than 10nF to minimize the accuracy impact.

Overrun error detection / protection is controlled by the ADDAT register. Either an interrupt request is generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended until the previous result has been read. For applications which require less than 16+8 analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the ST10F276E supports different conversion modes:

- **Single channel single conversion**: The analog level of the selected channel is sampled once and converted. The result of the conversion is stored in the ADDAT register.
- **Single channel continuous conversion**: The analog level of the selected channel is repeatedly sampled and converted. The result of the conversion is stored in the ADDAT register.
- **Auto scan single conversion**: The analog level of the selected channels are sampled once and converted. After each conversion the result is stored in the ADDAT register. The data can be transferred to the RAM by interrupt software management or using the powerful Peripheral Event Controller (PEC) data transfer.
- **Auto scan continuous conversion**: The analog level of the selected channels are repeatedly sampled and converted. The result of the conversion is stored in the ADDAT

15 I2C interface

The integrated I^2C Bus Module handles the transmission and reception of frames over the two-line SDA/SCL in accordance with the I^2C Bus specification. The I^2C Module can operate in slave mode, in master mode or in multi-master mode. It can receive and transmit data using 7-bit or 10-bit addressing. Data can be transferred at speeds up to 400 Kbit/s (both Standard and Fast I^2C bus modes are supported).

The module can generate three different types of interrupt:

- Requests related to bus events, like start or stop events, arbitration lost, etc.
- Requests related to data transmission
- Requests related to data reception

These requests are issued to the interrupt controller by three different lines, and identified as Error, Transmit, and Receive interrupt lines.

When the I^2C module is enabled by setting bit XI2CEN in XPERCON register, pins P4.4 and P4.7 (where SCL and SDA are respectively mapped as alternate functions) are automatically configured as bidirectional open-drain: the value of the external pull-up resistor depends on the application. P4, DP4 and ODP4 cannot influence the pin configuration.

When the I^2C cell is disabled (clearing bit XI2CEN), P4.4 and P4.7 pins are standard I/ O controlled by P4, DP4 and ODP4.

The speed of the I^2C interface may be selected between Standard mode (0 to 100 kHz) and Fast I^2C mode (100 to 400 kHz).

The Bidirectional reset is not effective in case RPD is held low, when a Software or Watchdog reset event occurs. On the contrary, if a Software or Watchdog Bidirectional reset event is active and RPD becomes low, the $\overline{\text{RSTIN}}$ pin is immediately released, while the internal reset sequence is completed regardless of RPD status change (1024 TCL).

Note: The bidirectional reset function is disabled by any reset sequence (bit BDRSTEN of SYSCON is cleared). To be activated again it must be enabled during the initialization routine.

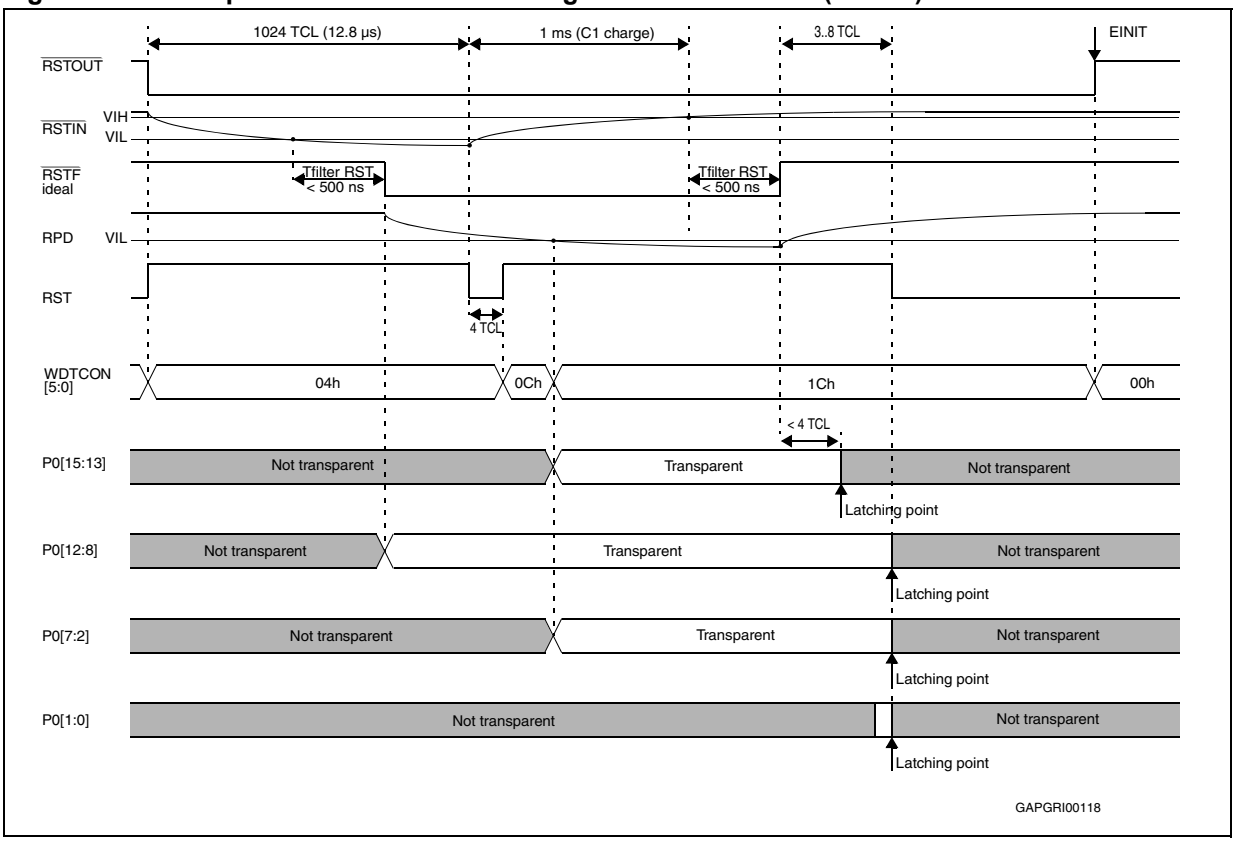
WDTCON flags

Similarly to what already highlighted in the previous section when discussing about Short reset and the degeneration into Long reset, similar situations may occur when Bidirectional reset is enabled. The presence of the internal filter on $\overline{\text{RSTIN}}$ pin introduces a delay: when $\overline{\text{RSTIN}}$ is released, the internal signal after the filter (see $\overline{\text{RSTF}}$ in the drawings) is delayed, so it remains still active (low) for a while. It means that depending on the internal clock speed, a short reset may be recognized as a long reset: the WDTCON flags are set accordingly.

Besides, when either Software or Watchdog bidirectional reset events occur, again when the $\overline{\text{RSTIN}}$ pin is released (at the end of the internal reset sequence), the $\overline{\text{RSTF}}$ internal signal (after the filter) remains low for a while, and depending on the clock frequency it is recognized high or low: 8TCL after the completion of the internal sequence, the level of $\overline{\text{RSTF}}$ signal is sampled, and if recognized still low a Hardware reset sequence starts, and WDTCON will flag this last event, masking the previous one (Software or Watchdog reset). Typically, a Short Hardware reset is recognized, unless the $\overline{\text{RSTIN}}$ pin (and consequently internal signal $\overline{\text{RSTF}}$) is sufficiently held low by the external hardware to inject a Long Hardware reset. After this occurrence, the initialization routine is not able to recognize a Software or Watchdog bidirectional reset event, since a different source is flagged inside WDTCON register. This phenomenon does not occur when internal Flash is selected during reset ($\overline{\text{EA}}$ = 1), since the initialization of the Flash itself extend the internal reset duration well beyond the filter delay.

Figures *34*, *35* and *36* summarize the timing for Software and Watchdog Timer Bidirectional reset events: In particular, *Figure 36* shows the degeneration into Hardware reset.

Figure 41. Example of software or watchdog bidirectional reset ($\overline{EA}$ = 0)



Warning: **During power-off phase, it is important that the external hardware maintains a stable ground level on RSTIN pin, without any glitch, in order to avoid spurious exiting from reset status with unstable power supply.**

20.3.2 Exiting stand-by mode

After the system has entered the Stand-by Mode, the procedure to exit this mode consists of a standard Power-on sequence, with the only difference that the RAM is already powered through V_{18SB} internal reference (derived from V_{STBY} pin external voltage).

It is recommended to held the device under RESET ($\overline{RSTIN}$ pin forced low) until external V_{DD} voltage pin is stable. Even though, at the very beginning of the power-on phase, the device is maintained under reset by the internal low voltage detector circuit (implemented inside the main voltage regulator) till the internal V_{18} becomes higher than about 1.0V, **there is no warranty that the device stays under reset status if RSTIN is at high level during power ramp up. So, it is important the external hardware is able to guarantee a stable ground level on RSTIN along the power-on phase, without any temporary glitch.**

The external hardware shall be responsible to drive low the $\overline{RSTIN}$ pin until the V_{DD} is stable, even though the internal LVD is active.

Once the internal Reset signal goes low, the RAM (still frozen) power supply is switched to the main V_{18}.

At this time, everything becomes stable, and the execution of the initialization routines can start: XRAM2EN bit can be set, enabling the RAM.

20.3.3 Real-time clock and stand-by mode

When Stand-by mode is entered (turning off the main supply V_{DD}), the Real-Time Clock counting can be maintained running in case the on-chip 32 kHz oscillator is used to provide the reference to the counter. This is not possible if the main oscillator is used as reference for the counter: Being the main oscillator powered by V_{DD}, once this is switched off, the oscillator is stopped.

22.4 Special function registers ordered by name

Table 67 lists in alphabetical order all SFRs which are implemented in the ST10F276E.

Bit-addressable SFRs are marked with the letter "**b**" in column "Name".

SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address".

Table 67. Special function registers ordered by address

Name	Physical address	8-bit address	Description	Reset value
ADCIC **b**	FF98h	CCh	A/D converter end of conversion interrupt control register	- - 00h
ADCON **b**	FFA0h	D0h	A/D converter control register	0000h
ADDAT	FEA0h	50h	A/D converter result register	0000h
ADDAT2	F0A0h**E**	50h	A/D converter 2 result register	0000h
ADDRSEL1	FE18h	0Ch	Address select register 1	0000h
ADDRSEL2	FE1Ah	0Dh	Address select register 2	0000h
ADDRSEL3	FE1Ch	0Eh	Address select register 3	0000h
ADDRSEL4	FE1Eh	0Fh	Address select register 4	0000h
ADEIC **b**	FF9Ah	CDh	A/D converter overrun error interrupt control register	- - 00h
BUSCON0 **b**	FF0Ch	86h	Bus configuration register 0	0xx0h
BUSCON1 **b**	FF14h	8Ah	Bus configuration register 1	0000h
BUSCON2 **b**	FF16h	8Bh	Bus configuration register 2	0000h
BUSCON3 **b**	FF18h	8Ch	Bus configuration register 3	0000h
BUSCON4 **b**	FF1Ah	8Dh	Bus configuration register 4	0000h
CAPREL	FE4Ah	25h	GPT2 capture/reload register	0000h
CC0	FE80h	40h	CAPCOM register 0	0000h
CC0IC b	FF78h	BCh	CAPCOM register 0 interrupt control register	- - 00h
CC1	FE82h	41h	CAPCOM register 1	0000h
CC10	FE94h	4Ah	CAPCOM register 10	0000h
CC10IC **b**	FF8Ch	C6h	CAPCOM register 10 interrupt control register	- - 00h
CC11	FE96h	4Bh	CAPCOM register 11	0000h
CC11IC **b**	FF8Eh	C7h	CAPCOM register 11 interrupt control register	- - 00h
CC12	FE98h	4Ch	CAPCOM register 12	0000h
CC12IC **b**	FF90h	C8h	CAPCOM register 12 interrupt control register	- - 00h
CC13	FE9Ah	4Dh	CAPCOM register 13	0000h
CC13IC **b**	FF92h	C9h	CAPCOM register 13 interrupt control register	- - 00h
CC14	FE9Ch	4Eh	CAPCOM register 14	0000h
CC14IC **b**	FF94h	CAh	CAPCOM register 14 interrupt control register	- - 00h

Table 69. X-Registers ordered by name (continued)

Name	Physical address	Description	Reset value
XSSCRB	E808h	XSSC receive buffer	XXXXh
XSSCTB	E806h	XSSC transmit buffer	0000h

Table 70. X-registers ordered by address (continued)

Name	Physical address	Description	Reset value
XPICON	EB26h	Extended port input threshold control register	- - 00h
XIR2SEL	EB30h	X-Interrupt 2 selection register	0000h
XIR2SET	EB32h	X-Interrupt 2 set register (write-only)	0000h
XIR2CLR	EB34h	X-Interrupt 2 clear register (write-only)	0000h
XP1DIDIS	EB36h	Port 1 digital disable register	0000h
XIR3SEL	EB40h	X-Interrupt 3 selection register	0000h
XIR3SET	EB42h	X-Interrupt 3 set selection register (write-only)	0000h
XIR3CLR	EB44h	X-Interrupt 3 clear selection register (write-only)	0000h
XMISC	EB46h	XBUS miscellaneous features register	0000h
XEMU0	EB76h	XBUS emulation register 0 (write-only)	XXXXh
XEMU1	EB78h	XBUS emulation register 1 (write-only)	XXXXh
XEMU2	EB7Ah	XBUS emulation register 2 (write-only)	XXXXh
XEMU3	EB7Ch	XBUS emulation register 3 (write-only)	XXXXh
XPEREMU	EB7Eh	XPERCON copy for emulation (write-only)	XXXXh
XPWMCON0	EC00h	XPWM module control register 0	0000h
XPWMCON1	EC02h	XPWM module control register 1	0000h
XPOLAR	EC04h	XPWM module channel polarity register	0000h
XPWMCON0SET	EC06h	XPWM module set control register 0 (write-only)	0000h
XPWMCON0CLR	EC08h	XPWM module clear control reg. 0 (write-only)	0000h
XPWMCON1SET	EC0Ah	XPWM module set control register 0 (write-only)	0000h
XPWMCON1CLR	EC0Ch	XPWM module clear control reg. 0 (write-only)	0000h
XPT0	EC10h	XPWM module up/down counter 0	0000h
XPT1	EC12h	XPWM module up/down counter 1	0000h
XPT2	EC14h	XPWM module up/down Counter 2	0000h
XPT3	EC16h	XPWM module up/down counter 3	0000h
XPP0	EC20h	XPWM module period register 0	0000h
XPP1	EC22h	XPWM module period register 1	0000h
XPP2	EC24h	XPWM module period register 2	0000h
XPP3	EC26h	XPWM module period register 3	0000h
XPW0	EC30h	XPWM module pulse width register 0	0000h

Table 70. X-registers ordered by address (continued)

Name	Physical address	Description	Reset value
CAN1IF2CR	EF40h	CAN1: IF2 command request	0001h
CAN1IF2CM	EF42h	CAN1: IF2 command mask	0000h
CAN1IF2M1	EF44h	CAN1: IF2 mask 1	FFFFh
CAN1IF2M2	EF46h	CAN1: IF2 mask 2	FFFFh
CAN1IF2A1	EF48h	CAN1: IF2 arbitration 1	0000h
CAN1IF2A2	EF4Ah	CAN1: IF2 arbitration 2	0000h
CAN1IF2MC	EF4Ch	CAN1: IF2 message control	0000h
CAN1IF2DA1	EF4Eh	CAN1: IF2 data A 1	0000h
CAN1IF2DA2	EF50h	CAN1: IF2 data A 2	0000h
CAN1IF2DB1	EF52h	CAN1: IF2 data B 1	0000h
CAN1IF2DB2	EF54h	CAN1: IF2 data B 2	0000h
CAN1TR1	EF80h	CAN1: transmission request 1	0000h
CAN1TR2	EF82h	CAN1: transmission request 2	0000h
CAN1ND1	EF90h	CAN1: new data 1	0000h
CAN1ND2	EF92h	CAN1: new data 2	0000h
CAN1IP1	EFA0h	CAN1: interrupt pending 1	0000h
CAN1IP2	EFA2h	CAN1: interrupt pending 2	0000h
CAN1MV1	EFB0h	CAN1: message valid 1	0000h
CAN1MV2	EFB2h	CAN1: message valid 2	0000h

Table 75. IDMEM description

Bit	Function
MEMSIZE	Internal memory size Internal memory size is 4 x (MEMSIZE) (in Kbyte) 0D0h for ST10F276E (832 Kbytes)
MEMTYP	Internal memory type 0h: ROM-Less 1h: (M) ROM memory 2h: (S) Standard Flash memory 3h: (H) High performance Flash memory (ST10F276E) 4h...Fh: *Reserved*

IDPROG (F078h / 3Ch) ESFR Reset value:0040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

Table 76. IDPROG description

Bit	Function
PROGVDD	Programming VDD voltage VDD voltage when programming EPROM or Flash devices is calculated using the following formula: VDD = 20 x [PROGVDD] / 256 (volts) - 40h for ST10F276E (5V).
PROGVPP	Programming VPP voltage (no need of external VPP) - 00h

Note: All identification words are read-only registers.

The values written inside different Identification Register bits are valid only after the Flash initialization phase is completed. When code execution is started from internal memory (pin $\overline{EA}$ held high during reset), the Flash has completed its initialization, so the bits of Identification Registers are immediately ready to be read out. On the contrary, when code execution is started from external memory (pin $\overline{EA}$ held low during reset), the Flash initialization is not yet completed, so the bits of Identification Registers are not ready. The user can poll bits 15 and 14 of IDMEM register: When both bits are read low, the Flash initialization is complete, so all Identification Register bits are correct.

Before Flash initialization completion, the default setting of the different identification registers are the following:

IDMANUF	0403h
IDCHIP	114xh (x = silicon revision)
IDMEM	F0D0h
IDPROG	0040h

Table 84. ESFR description (continued)

Bit	Function
XRAM2EN	XRAM2 enable bit 0: Accesses to the on-chip 64 Kbyte XRAM are disabled, external access performed. Address range 0F'0000h-0F'FFFFh is directed to external memory only if XFLASHEN is '0' also. 1: The on-chip 64 Kbyte XRAM is enabled and can be accessed.
XRTCEN	RTC enable 0: Accesses to the on-chip RTC module are disabled, external access performed. Address range 00'ED00h-00'EDFF is directed to external memory only if CAN1EN, CAN2EN, XASCEN, XSSCEN, XI2CEN, XPWMEN and XMISCEN are '0' also. 1: The on-chip RTC module is enabled and can be accessed.
XPWMEN	XPWM enable 0: Accesses to the on-chip XPWM module are disabled, external access performed. Address range 00'EC00h-00'ECFF is directed to external memory only if CAN1EN, CAN2EN, XASCEN, XSSCEN, XI2CEN, XRTCEN and XMISCEN are '0' also. 1: The on-chip XPWM module is enabled and can be accessed.
XFLASHEN	XFlash enable bit 0: Accesses to the on-chip XFlash and Flash registers are disabled, external access performed. Address range 09'0000h-0E'FFFFh is directed to external memory only if XRAM2EN is '0' also. 1: The on-chip XFlash is enabled and can be accessed.
XASCEN	XASC enable bit 0: Accesses to the on-chip XASC are disabled, external access performed. Address range 00'E900h-00'E9FFh is directed to external memory only if CAN1EN, CAN2EN, XRTCEN, XASCEN, XI2CEN, XPWMEN and XMISCEN are '0' also. 1: The on-chip XASC is enabled and can be accessed.
XSSCEN	XSSC enable bit 0: Accesses to the on-chip XSSC are disabled, external access performed. Address range 00'E800h-00'E8FFh is directed to external memory only if CAN1EN, CAN2EN, XRTCEN, XASCEN, XI2CEN, XPWMEN and XMISCEN are '0' also. 1: The on-chip XSSC is enabled and can be accessed.
XI2CEN	I^2C enable bit 0: Accesses to the on-chip I^2C are disabled, external access performed. Address range 00'EA00h-00'EAFFh is directed to external memory only if CAN1EN, CAN2EN, XRTCEN, XASCEN, XSSCEN, XPWMEN and XMISCEN are '0' also. 1: The on-chip I^2C is enabled and can be accessed.
XMISCEN	XBUS additional features enable bit 0: Accesses to the Additional Miscellaneous Features is disabled. Address range 00'EB00h-00'EBFFh is directed to external memory only if CAN1EN, CAN2EN, XRTCEN, XASCEN, XSSCEN, XPWMEN and XI2CEN are '0' also. 1: The Additional Features are enabled and can be accessed.

Table 89. Package characteristics

Package	Packing	Operating temperature	CPU frequency range
Die	Tape and reel	- 40 / +125°C	1 - 64 MHz
PQFP 144	Tray		
	Tape and reel		
LQFP 144	Tray		1 - 40 MHz
	Tape and reel	-40 / +105°C	1 - 48 MHz

23.4 Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10F276E and its demands on the system.

Where the ST10F276E logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column. Where the external system must provide signals with their respective timing characteristics to the ST10F276E, the symbol “SR” (System Requirement) is included in the “Symbol” column.

23.5 DC characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C

Table 90. DC characteristics

Symbol		Parameter	Test condition	Limit values		Unit
				Min.	Max.	
V_{IL}	SR	Input low voltage (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1, READY)	-	- 0.3	0.8	V
V_{ILS}	SR	Input low voltage (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1, READY)	-	- 0.3	0.3 V_{DD}	V
V_{IL1}	SR	Input low voltage $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD	-	- 0.3	0.3 V_{DD}	V
V_{IL2}	SR	Input low voltage XTAL1 (CMOS only)	Direct drive mode	- 0.3	0.3 V_{DD}	V
V_{IL3}	SR	Input low voltage READY (TTL only)	-	- 0.3	0.8	V
V_{IH}	SR	Input high voltage (TTL mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	-	2.0	V_{DD} + 0.3	V
V_{IHS}	SR	Input high voltage (CMOS mode) (except $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD, XTAL1)	-	0.7 V_{DD}	V_{DD} + 0.3	V
V_{IH1}	SR	Input high voltage $\overline{RSTIN}$, $\overline{EA}$, $\overline{NMI}$, RPD	-	0.7 V_{DD}	V_{DD} + 0.3	V
V_{IH2}	SR	Input high voltage XTAL1 (CMOS only)	Direct Drive mode	0.7 V_{DD}	V_{DD} + 0.3	V
V_{IH3}	SR	Input high voltage READY (TTL only)	-	2.0	V_{DD} + 0.3	

23.8.12 PLL lock/unlock

During normal operation, if the PLL is unlocked for any reason, an interrupt request to the CPU is generated and the reference clock (oscillator) is automatically disconnected from the PLL input: In this way, the PLL goes into free-running mode, providing the system with a backup clock signal (free running frequency F_{free}). This feature allows to recover from a crystal failure occurrence without risking to go into an undefined configuration: The system is provided with a clock allowing the execution of the PLL unlock interrupt routine in a safe mode.

The path between the reference clock and PLL input can be restored only by a hardware reset, or by a bidirectional software or watchdog reset event that forces the $\overline{RSTIN}$ pin low.

Note: The external RC circuit on $\overline{RSTIN}$ pin must be the right size in order to extend the duration of the low pulse to grant the PLL to be locked before the level at $\overline{RSTIN}$ pin is recognized high: Bidirectional reset internally drives $\overline{RSTIN}$ pin low for just 1024 TCL (definitely not sufficient to get the PLL locked starting from free-running mode).

Conditions: V_{DD} = 5V ±10%, T_A = -40 / +125°C

Table 97. PLL lock/unlock timing

Symbol	Parameter	Conditions	Value		Unit
			Min.	Max.	
T_{PSUP}	PLL Start-up time (1)	Stable V_{DD} and reference clock	-	300	µs
T_{LOCK}	PLL Lock-in time	Stable V_{DD} and reference clock, starting from free-running mode	-	250	
T_{JIT}	Single Period Jitter (1) (cycle to cycle = 2 TCL)	6 sigma time period variation (peak to peak)	-500	+500	ps
F_{free}	PLL free running frequency	Multiplication factors: 3, 4 Multiplication factors: 5, 8, 10, 16	250 500	2000 4000	kHz

1. Not 100% tested, guaranteed by design characterization.

23.8.13 Main oscillator specifications

Conditions: V_{DD} = 5V ±10%, T_A = -40 / +125°C

Table 98. Main oscillator specifications

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
g_m	Oscillator transconductance		8	17	35	mA/V
V_{OSC}	Oscillation amplitude(1)	Peak to peak	-	V_{DD} - 0.4	-	V
V_{AV}	Oscillation-voltage level(1)	Sine wave middle	-	V_{DD} / 2 -0.25	-	
t_{STUP}	Oscillator start-up time(1)	Stable V_{DD} - crystal	-	3	4	ms
		Stable V_{DD}, resonator	-	2	3	

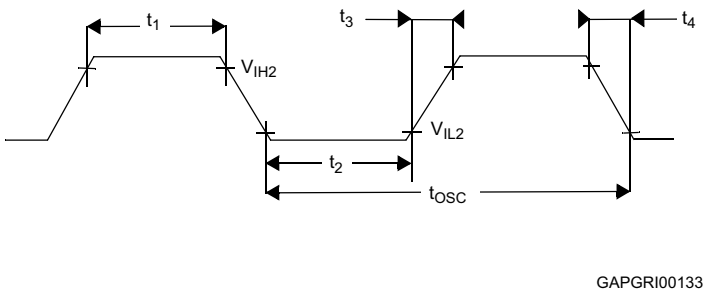
1. Not 100% tested, guaranteed by design characterization

Table 102. External clock drive timing

Symbol		Parameter	Direct drive $f_{CPU} = f_{XTAL}$		Direct drive with prescaler $f_{CPU} = f_{XTAL} / 2$		PLL usage $f_{CPU} = f_{XTAL} \times F$		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{OSC}	SR	XTAL1 period(1) (2)	15.625	-	83.3	250	83.3	250	ns
t_1	SR	High time(3)	6	-	3	-	6	-	
t_2	SR	Low time(3)							
t_3	SR	Rise time(3)	-	2	-	2	-	2	
t_4	SR	Fall time(3)							

1. The minimum value for the XTAL1 signal period is considered as the theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.
2. 4-12 MHz is the input frequency range when using an external clock source. 64 MHz can be applied with an external clock source only when Direct Drive mode is selected: In this case, the oscillator amplifier is bypassed so it does not limit the input frequency.
3. The input clock signal must reach the defined levels V_{IL2} and V_{IH2}.

Figure 56. External clock drive XTAL1



Note: When Direct Drive is selected, an external clock source can be used to drive XTAL1. The maximum frequency of the external clock source depends on the duty cycle: When 64 MHz is used, 50% duty cycle is granted (low phase = high phase = 7.8ns); when for instance 32 MHz is used, a 25% duty cycle can be accepted (minimum phase, high or low, again equal to 7.8ns).

23.8.16 Memory cycle variables

The tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. *Table 103* describes how these variables are computed.

Table 103. Memory cycle variables

Symbol	Description	Values
t_A	ALE extension	TCL x [ALECTL]
t_C	Memory cycle time wait states	2TCL x (15 - [MCTC])
t_F	Memory tri-state time	2TCL x (1 - [MTTC])

Figure 62. Demultiplexed bus with/without R/W delay and extended ALE

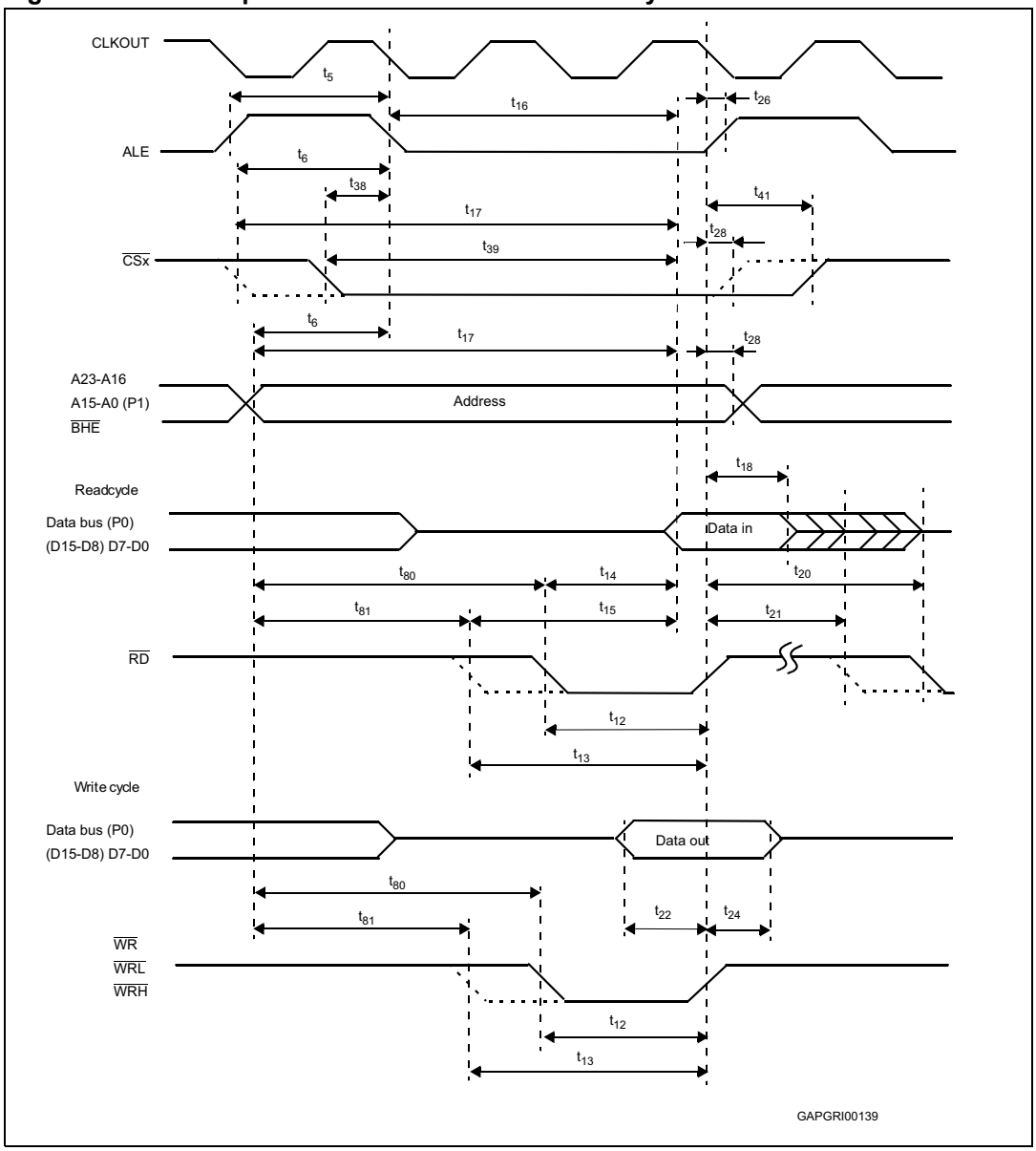
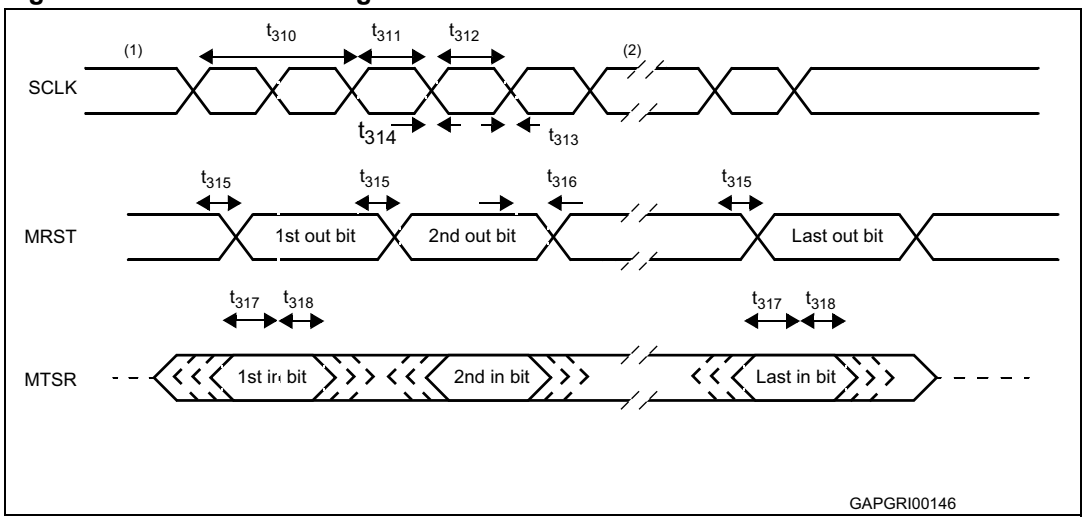


Figure 69. SSC slave timing



1. The phase and polarity of shift and latch edge of SCLK is programmable. This figure uses the leading clock edge as shift edge (drawn in bold), with latch on trailing edge (SSCPH = 0b), idle clock line is low, leading clock edge is low-to-high transition (SSCPO = 0b).
2. The bit timing is repeated for all bits to be transmitted or received.