Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	832KB (832K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	68K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f276-6qr3

List of figures

4.3.4 Flash control register 1 high

The Flash control register 1 high (FCR1H), together with Flash control register 1 low (FCR1L), is used to select the sectors to erase, or during any write operation to monitor the status of each sector and each bank of the module selected by SMOD bit of FCR0H. First diagram shows FCR1H meaning when SMOD = 0; the second one when SMOD = 1.

FCR1H (0x0E 0006) SMOD = 0 FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						B3S	B2S	Reserved						B3F1	B3F0
						RS	RS							RS	RS

FCR1H (0x0E 0006) SMOD = 1 FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						B1S	B0S	Reserved						B1F1	B1F0
-						RS	RS							RS	RS

Table 9. Flash control register 1 high

Bit	Function
SMOD = 0 (XFLASH selected)	
B3F(1:0)	Bank 3 XFLASH sector 1:0 status During any erase operation, these bits are automatically set and give the status of the two sectors of Bank 3 (B3F1-B3F0). The meaning of B3Fy bit for sector y of Bank 1 is given by *Table 10*. These bits are automatically reset at the end of a erase operation if no errors are detected.
B(3:2)S	Bank 3-2 status (XFLASH) During any erase operation, these bits are automatically modified and give the status of the two banks (B3-B2). The meaning of BxS bit for bank x is given in *Table 10*. These bits are automatically reset at the end of a erase operation if no errors are detected.
SMOD = 1 (IFLASH selected)	
B1F(1:0)	Bank 1 IFLASH sector 1:0 status During any erase operation, these bits are automatically set and give the status of the two sectors of Bank 1 (B1F1-B1F0). The meaning of B1Fy bit for sector y of Bank 1 is given by *Table 10*. These bits are automatically reset at the end of a erase operation if no errors are detected.
B(1:0)S	Bank 1-0 status (IFLASH) During any erase operation, these bits are automatically modified and give the status of the two banks (B1-B0). The meaning of BxS bit for bank x is given in *Table 10*. These bits are automatically reset at the end of a erase operation if no errors are detected.

During any erase operation, these bits are automatically set and give the status of the two sectors of Bank 1 (B1F1-B1F0). The meaning of B1Fy bit for sector y of Bank 1 is given by *Table 10*. These bits are automatically reset at the end of a erase operation if no errors are detected.

4.4.3 Flash non-volatile write protection X register high

FNVWPXRH (0x0E DF B2) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														W3P1	W3P0
														RW	RW

Table 20. Flash non-volatile write protection X register high

Bit	Function
W3P(1:0)	Write Protection Bank 3 / Sectors 1-0 (XFLASH) These bits, if programmed at 0, disable any write access to the sectors of Bank 3 (XFLASH).

4.4.4 Flash non-volatile write protection I register low

FNVWPIRL (0x0E DFB4) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						W0P9	W0P8	W0P7	W0P6	W0P5	W0P4	W0P3	W0P2	W0P1	W0P0
						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 21. Flash non-volatile write protection I register low

Bit	Function
W0P(9:0)	Write Protection Bank 0 / Sectors 9-0 (IFLASH) These bits, if programmed at 0, disable any write access to the sectors of Bank 0 (IFLASH).

4.4.5 Flash non-volatile write protection I register high

FNVWPIRH (0x0E DFB6) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														W1P1	W1P0
														RW	RW

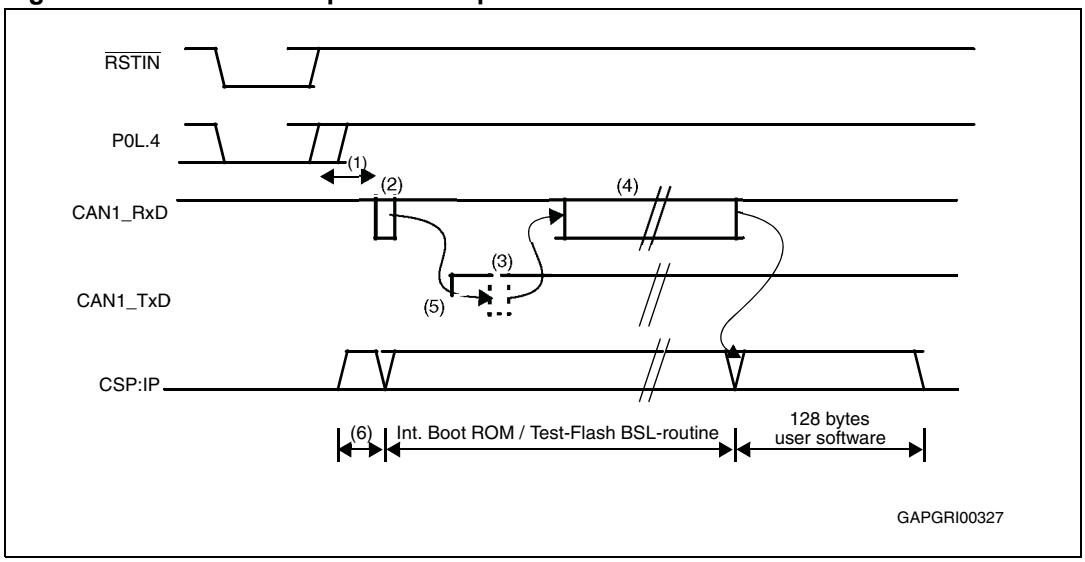
Table 22. Flash non-volatile write protection I register high

Bit	Function
W1P(1:0)	Write Protection Bank 1 / Sectors 1-0 (IFLASH) These bits, if programmed at 0, disable any write access to the sectors of Bank 1 (IFLASH).

Table 27. Flash write operations (continued)

Operation	Select bit	Address and data	Start bit
Set Protection	SPR	FDR0L/FDR0H	WMS
Program/Erase Suspend	SUSP	None	None

Figure 11. CAN bootstrap loader sequence



1. BSL initialization time, > 1ms @ f_{CPU} = 40 MHz
2. Zero frame (CAN message: standard ID = 0, DLC = 0), sent by host
3. CAN message (standard ID = E6h, DLC = 3, Data0 = D5h, Data1-Data2 = IDCHIP_low-high), sent by ST10F276E on request
4. 128 bytes of code / data, sent by host
5. Caution: CAN1_TxD is only driven a certain time after reception of the zero byte (1.3ms @ f_{CPU} = 40 MHz).
6. Internal Boot ROM / Test-Flash

The Bootstrap Loader can load

- the complete application software into ROM-less systems,
- temporary software into complete systems for testing or calibration,
- a programming routine for Flash devices.

The BSL mechanism may be used for standard system start-up as well as for only special occasions like system maintenance (firmware update) or end-of-line programming or testing.

5.4.2 Entering the CAN bootstrap loader

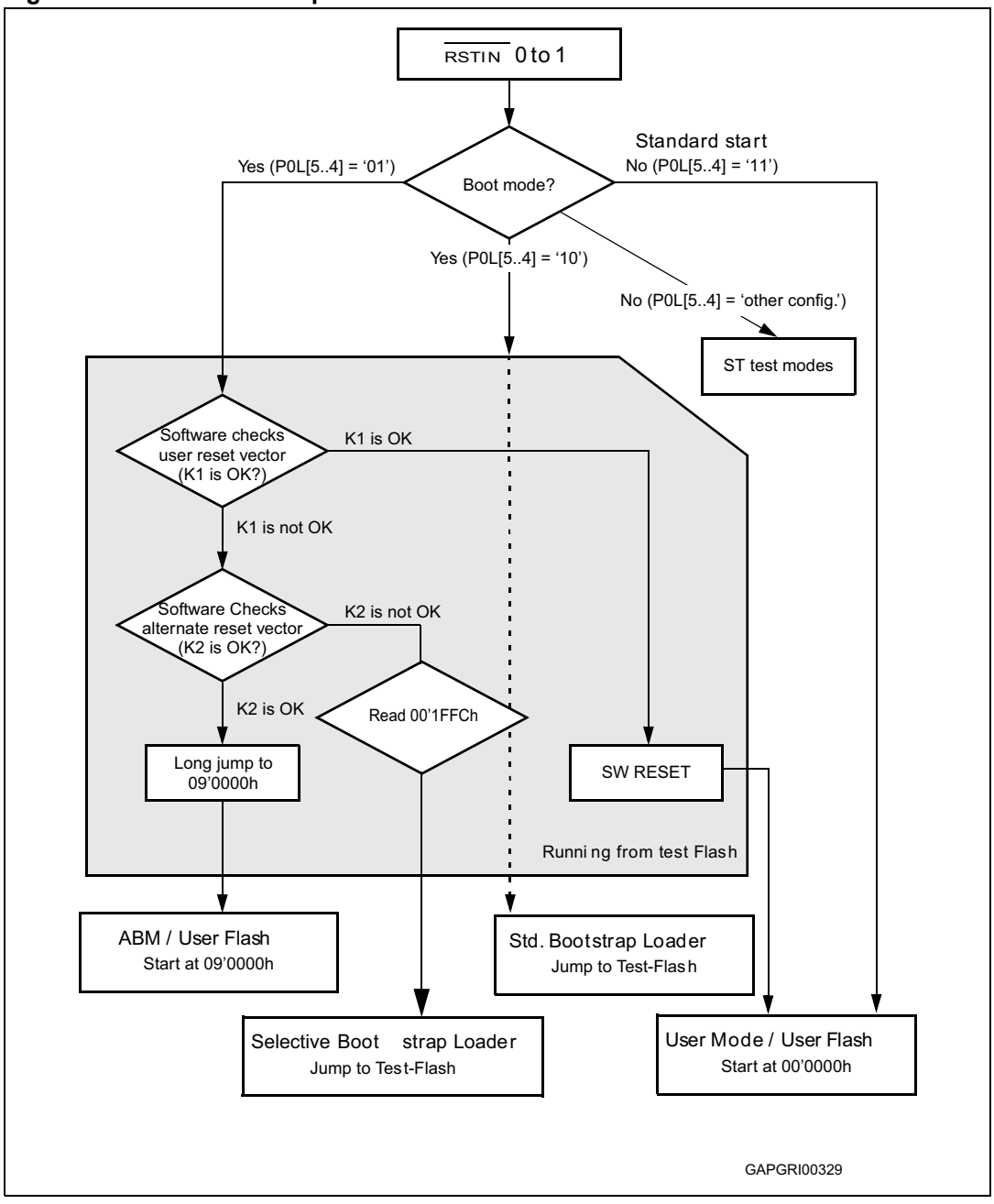
The ST10F276E enters BSL mode if pin P0L.4 is sampled low at the end of a hardware reset. In this case, the built-in bootstrap loader is activated independently of the selected bus mode. The bootstrap loader code is stored in a special Test-Flash; no part of the standard mask ROM or Flash memory area is required for this.

After entering BSL mode and the respective initialization, the ST10F276E scans the CAN1_TxD line to receive the following initialization frame:

- Standard identifier = 0h
- DLC = 0h

As all the bits to be transmitted are dominant bits, a succession of 5 dominant bits and 1 stuff bit on the CAN network is used. From the duration of this frame, it calculates the corresponding baud rate factor with respect to the current CPU clock, initializes the CAN1 interface accordingly, switches pin CAN1_TxD to output and enables the CAN1 interface to take part in the network communication. Using this baud rate, a Message Object is

Figure 13. Reset boot sequence



8 Interrupt system

The interrupt response time for internal program execution is from 78ns to 187.5ns at 64 MHz CPU clock.

The ST10F276E architecture supports several mechanisms for fast and flexible response to service requests that can be generated from various sources (internal or external) to the microcontroller. Any of these interrupt requests can be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single Byte or Word data transfer between any two memory locations with an additional increment of either the PEC source or destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited to perform the transmission or the reception of blocks of data. The ST10F276E has 8 PEC channels, each of them offers such fast interrupt-driven data transfer capabilities.

An interrupt control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit-field is dedicated to each existing interrupt source. Thanks to its related register, each source can be programmed to one of sixteen interrupt priority levels. Once starting to be processed by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Fast external interrupts may also have interrupt sources selected from other peripherals; for example the CANx controller receive signals (CANx_RxD) and I^2C serial clock signal can be used to interrupt the system.

Table 40 shows all the available ST10F276E interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Table 40. Interrupt sources

Source of interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	00'0040h	10h
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	00'0044h	11h
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	00'0048h	12h
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	00'004Ch	13h
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	00'0050h	14h
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	00'0054h	15h

12.2.2 Input threshold control

The standard inputs of the ST10F276E determine the status of input signals according to TTL levels. In order to accept and recognize noisy signals, CMOS input thresholds can be selected instead of the standard TTL thresholds for all the pins. These CMOS thresholds are defined above the TTL thresholds and feature a higher hysteresis to prevent the inputs from toggling while the respective input signal level is near the thresholds.

The Port Input Control registers PICON and XPICON are used to select these thresholds for each Byte of the indicated ports, this means the 8-bit ports P0L, P0H, P1L, P1H, P4, P7 and P8 are controlled by one bit each while ports P2, P3 and P5 are controlled by two bits each.

All options for individual direction and output mode control are available for each pin, independent of the selected input threshold.

12.3 Alternate port functions

Each port line has one associated programmable alternate input or output function.

- PORT0 and PORT1 may be used as address and data lines when accessing external memory. Besides, PORT1 provides also:
  - Input capture lines
  - 8 additional analog input channels to the A/D converter
- Port 2, Port 7 and Port 8 are associated with the capture inputs or compare outputs of the CAPCOM units and/or with the outputs of the PWM0 module, of the PWM1 module and of the ASC1.
  Port 2 is also used for fast external interrupt inputs and for timer 7 input.
- Port 3 includes the alternate functions of timers, serial interfaces, the optional bus control signal $\overline{BHE}$ and the system clock output (CLKOUT).
- Port 4 outputs the additional segment address bit A23...A16 in systems where more than 64 Kbytes of memory are to be access directly. In addition, CAN1, CAN2 and I^2C lines are provided.
- Port 5 is used as analog input channels of the A/D converter or as timer control signals.
- Port 6 provides optional bus arbitration signals ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) and chip select signals and the SSC1 lines.

If the alternate output function of a pin is to be used, the direction of this pin must be programmed for output (DPx.y='1'), except for some signals that are used directly after reset and are configured automatically. Otherwise the pin remains in the high-impedance state and is not effected by the alternate output function. The respective port latch should hold a '1', because its output is ANDed with the alternate output data (except for PWM output signals).

If the alternate input function of a pin is used, the direction of the pin must be programmed for input (DPx.y='0') if an external device is driving the pin. The input direction is the default after reset. If no external device is connected to the pin, however, one can also set the direction for this pin to output. In this case, the pin reflects the state of the port output latch. Thus, the alternate input function reads the value stored in the port output latch. This can be used for testing purposes to allow a software trigger of an alternate input function by writing to the port output latch.

On most of the port lines, the user software is responsible for setting the proper direction when using an alternate input or output function of a pin.

19.2 Asynchronous reset

An asynchronous reset is triggered when $\overline{\text{RSTIN}}$ pin is pulled low while RPD pin is at low level. Then the ST10F276E is immediately (after the input filter delay) forced in reset default state. It pulls low $\overline{\text{RSTOUT}}$ pin, it cancels pending internal hold states if any, it aborts all internal/external bus cycles, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, it pulls high Port0 pins.

Note: If an asynchronous reset occurs during a read or write phase in internal memories, the content of the memory itself could be corrupted: to avoid this, synchronous reset usage is strongly recommended.

Power-on reset

The asynchronous reset must be used during the power-on of the device. Depending on crystal or resonator frequency, the on-chip oscillator needs about 1ms to 10ms to stabilize (refer to *Chapter 23: Electrical characteristics*), with an already stable V_{DD}. The logic of the ST10F276E does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the $\overline{\text{RSTIN}}$ pin and the RPD pin must be held at low level until the device clock signal is stabilized and the system configuration value on Port0 is settled.

At Power-on it is important to respect some additional constraints introduced by the start-up phase of the different embedded modules.

In particular the on-chip voltage regulator needs at least 1ms to stabilize the internal 1.8V for the core logic: this time is computed from when the external reference (V_{DD}) becomes stable (inside specification range, that is at least 4.5V). This is a constraint for the application hardware (external voltage regulator): the $\overline{\text{RSTIN}}$ pin assertion shall be extended to guarantee the voltage regulator stabilization.

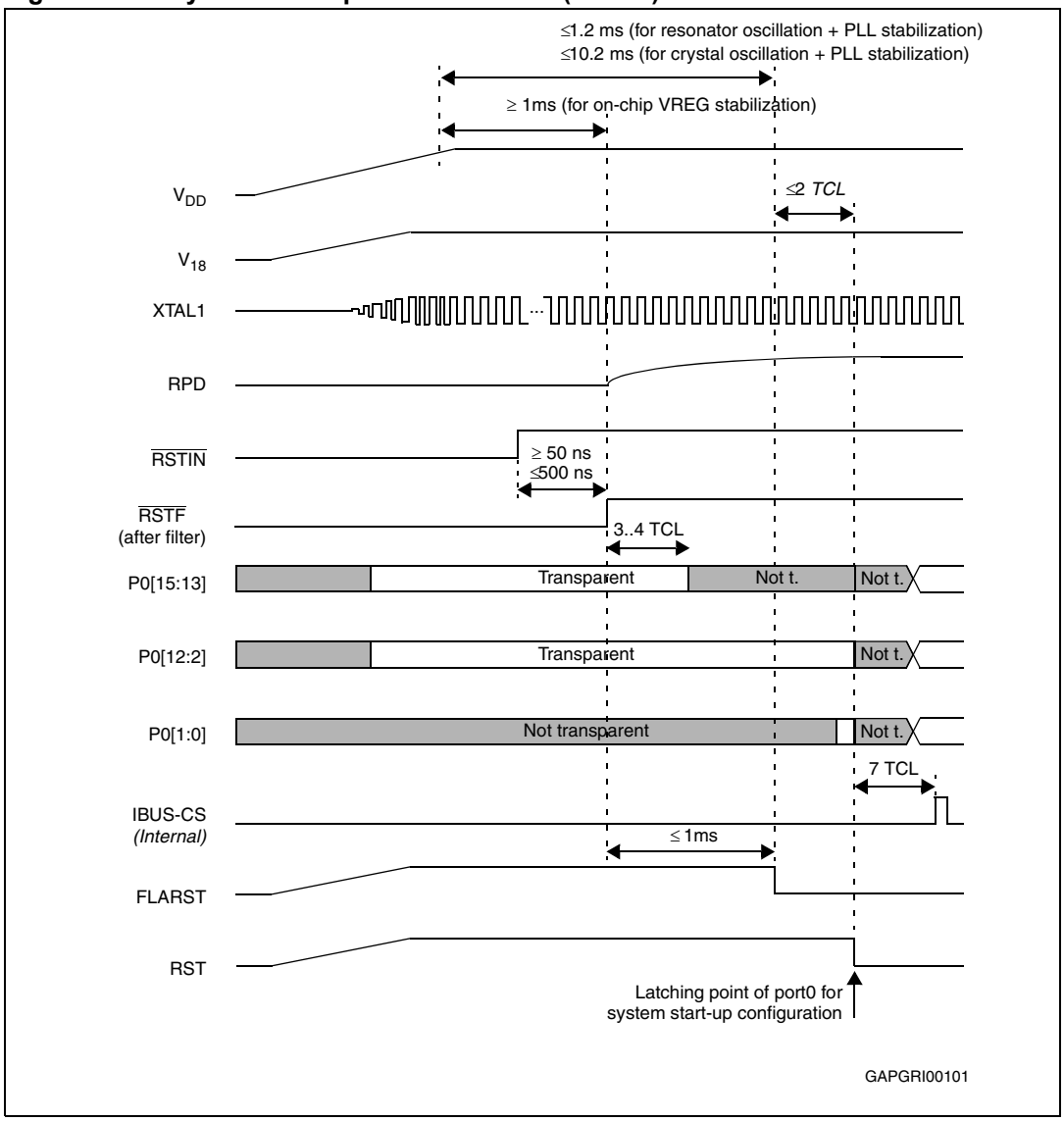
A second constraint is imposed by the embedded Flash. When booting from internal memory, starting from $\overline{\text{RSTIN}}$ releasing, it needs a maximum of 1ms for its initialization: before that, the internal reset (RST signal) is not released, so the CPU does not start code execution in internal memory.

Note: This is not true if external memory is used (pin $\overline{EA}$ held low during reset phase). In this case, once $\overline{RSTIN}$ pin is released, and after few CPU clock (Filter delay plus 3...8 TCL), the internal reset signal RST is released as well, so the code execution can start immediately after. Obviously, an eventual access to the data in internal Flash is forbidden before its initialization phase is completed: an eventual access during starting phase will return FFFFh (just at the beginning), while later 009Bh (an illegal opcode trap can be generated).

At Power-on, the $\overline{\text{RSTIN}}$ pin shall be tied low for a minimum time that includes also the start-up time of the main oscillator (t_{STUP} = 1ms for resonator, 10ms for crystal) and PLL synchronization time (t_{PSUP} = 200µs): this means that if the internal Flash is used, the $\overline{\text{RSTIN}}$ pin could be released before the main oscillator and PLL are stable to recover some time in the start-up phase (Flash initialization only needs stable V_{18}, but does not need stable system clock since an internal dedicated oscillator is used).

Warning: It is recommended to provide the external hardware with a current limitation circuitry. This is necessary to avoid permanent damages of the device during the power-on transient, when the capacitance on V_{18} pin is charged. For the on-chip voltage regulator functionality 10nF are

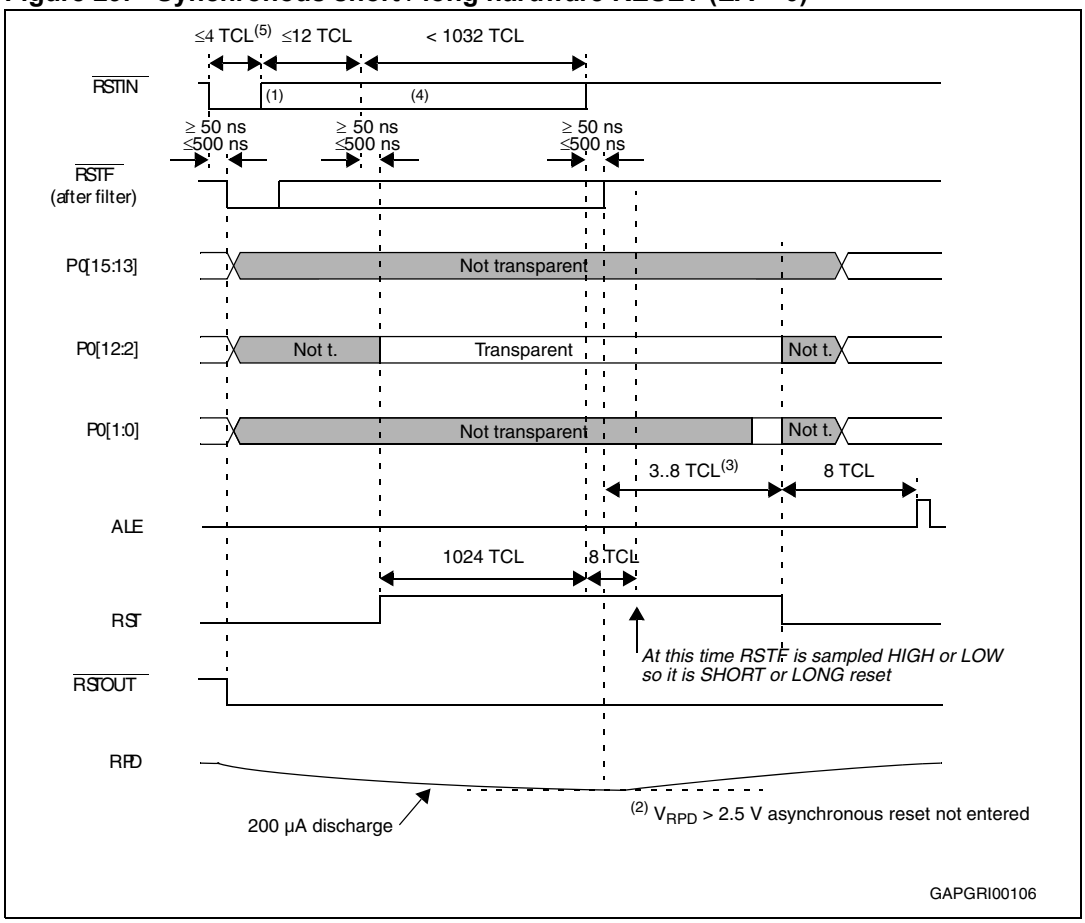
Figure 24. Asynchronous power-on RESET ($\overline{EA}$ = 1)



5 V operation), the asynchronous reset is then immediately entered.

3. RSTIN pin is pulled low if bit BDRSTEN (bit 3 of SYSCON register) was previously set by software. Bit BDRSTEN is cleared after reset.
4. Minimum RSTIN low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to *Section 19.1*).

Figure 29. Synchronous short / long hardware RESET ($\overline{EA}$ = 0)



1. RSTIN assertion can be released there. Refer also to *Section 19.1* for details on minimum pulse duration.
2. If during the reset condition (RSTIN low), RPD voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.
3. 3 to 8 TCL depending on clock source selection.
4. RSTIN pin is pulled low if bit BDRSTEN (bit 3 of SYSCON register) was previously set by software. Bit BDRSTEN is cleared after reset.
5. Minimum RSTIN low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to *Section 19.1*).

19.8 Reset application examples

Next two timing diagrams (*Figure 40* and *Figure 41*) provides additional examples of bidirectional internal reset events (Software and Watchdog) including in particular the external capacitances charge and discharge transients (refer also to *Figure 38* for the external circuit scheme).

Figure 40. Example of software or watchdog bidirectional reset ($\overline{EA}$ = 1)

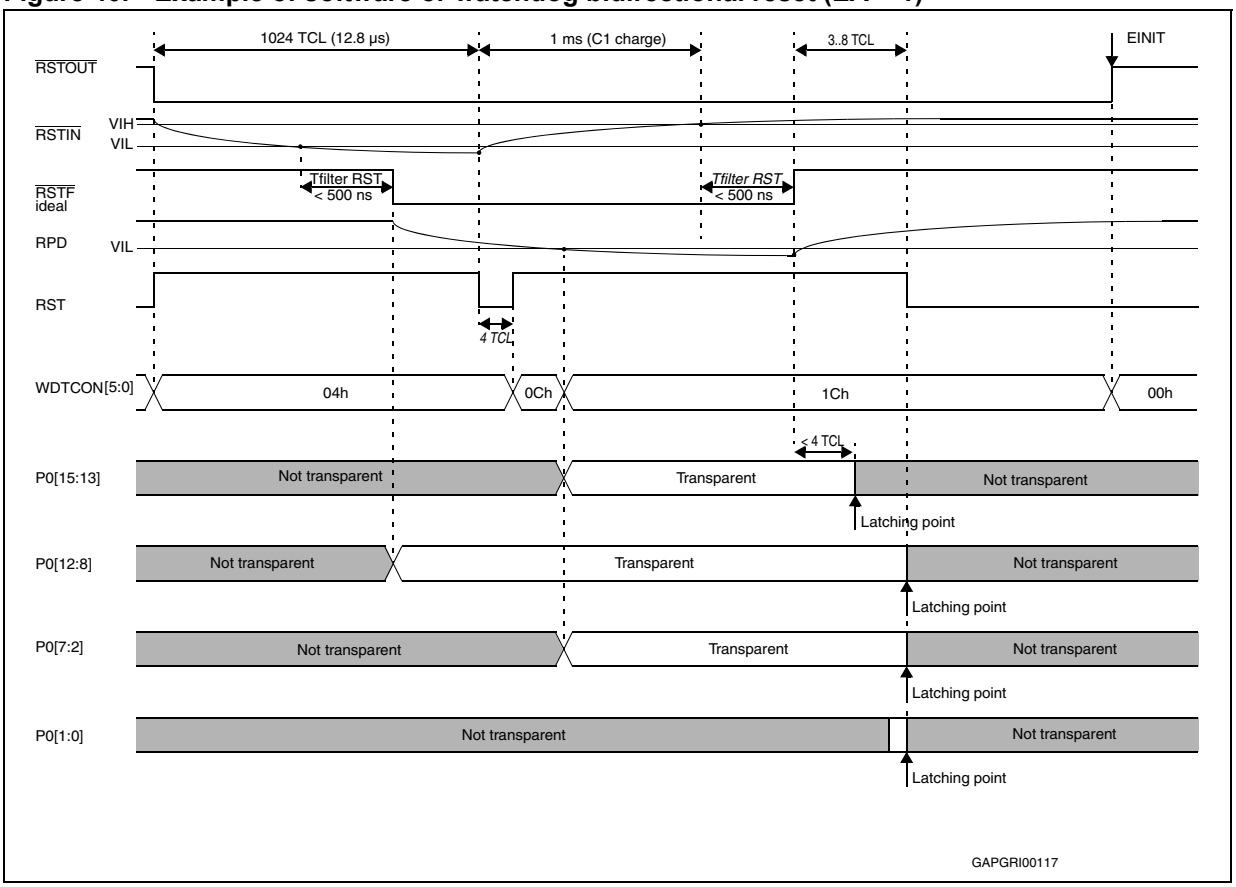


Figure 42. PORT0 bits latched into the different registers after reset

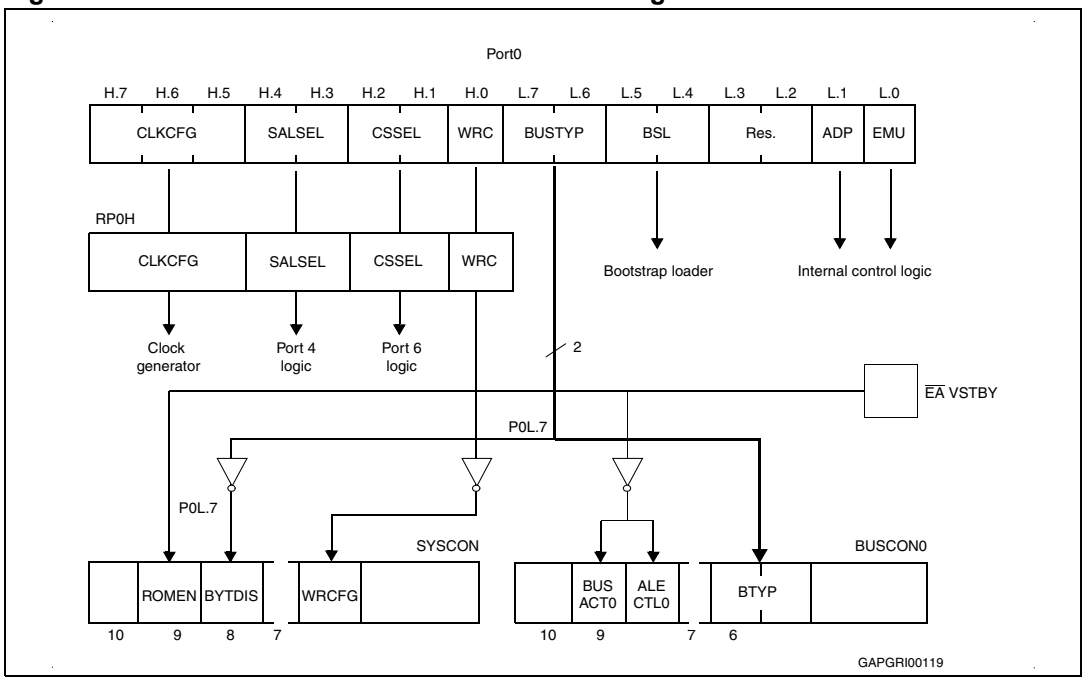


Table 69. X-Registers ordered by name (continued)

Name	Physical address	Description	Reset value
XSSCRB	E808h	XSSC receive buffer	XXXXh
XSSCTB	E806h	XSSC transmit buffer	0000h

Table 70. X-registers ordered by address (continued)

Name	Physical address	Description	Reset value
XPICON	EB26h	Extended port input threshold control register	- - 00h
XIR2SEL	EB30h	X-Interrupt 2 selection register	0000h
XIR2SET	EB32h	X-Interrupt 2 set register (write-only)	0000h
XIR2CLR	EB34h	X-Interrupt 2 clear register (write-only)	0000h
XP1DIDIS	EB36h	Port 1 digital disable register	0000h
XIR3SEL	EB40h	X-Interrupt 3 selection register	0000h
XIR3SET	EB42h	X-Interrupt 3 set selection register (write-only)	0000h
XIR3CLR	EB44h	X-Interrupt 3 clear selection register (write-only)	0000h
XMISC	EB46h	XBUS miscellaneous features register	0000h
XEMU0	EB76h	XBUS emulation register 0 (write-only)	XXXXh
XEMU1	EB78h	XBUS emulation register 1 (write-only)	XXXXh
XEMU2	EB7Ah	XBUS emulation register 2 (write-only)	XXXXh
XEMU3	EB7Ch	XBUS emulation register 3 (write-only)	XXXXh
XPEREMU	EB7Eh	XPERCON copy for emulation (write-only)	XXXXh
XPWMCON0	EC00h	XPWM module control register 0	0000h
XPWMCON1	EC02h	XPWM module control register 1	0000h
XPOLAR	EC04h	XPWM module channel polarity register	0000h
XPWMCON0SET	EC06h	XPWM module set control register 0 (write-only)	0000h
XPWMCON0CLR	EC08h	XPWM module clear control reg. 0 (write-only)	0000h
XPWMCON1SET	EC0Ah	XPWM module set control register 0 (write-only)	0000h
XPWMCON1CLR	EC0Ch	XPWM module clear control reg. 0 (write-only)	0000h
XPT0	EC10h	XPWM module up/down counter 0	0000h
XPT1	EC12h	XPWM module up/down counter 1	0000h
XPT2	EC14h	XPWM module up/down Counter 2	0000h
XPT3	EC16h	XPWM module up/down counter 3	0000h
XPP0	EC20h	XPWM module period register 0	0000h
XPP1	EC22h	XPWM module period register 1	0000h
XPP2	EC24h	XPWM module period register 2	0000h
XPP3	EC26h	XPWM module period register 3	0000h
XPW0	EC30h	XPWM module pulse width register 0	0000h

23.7 A/D converter characteristics

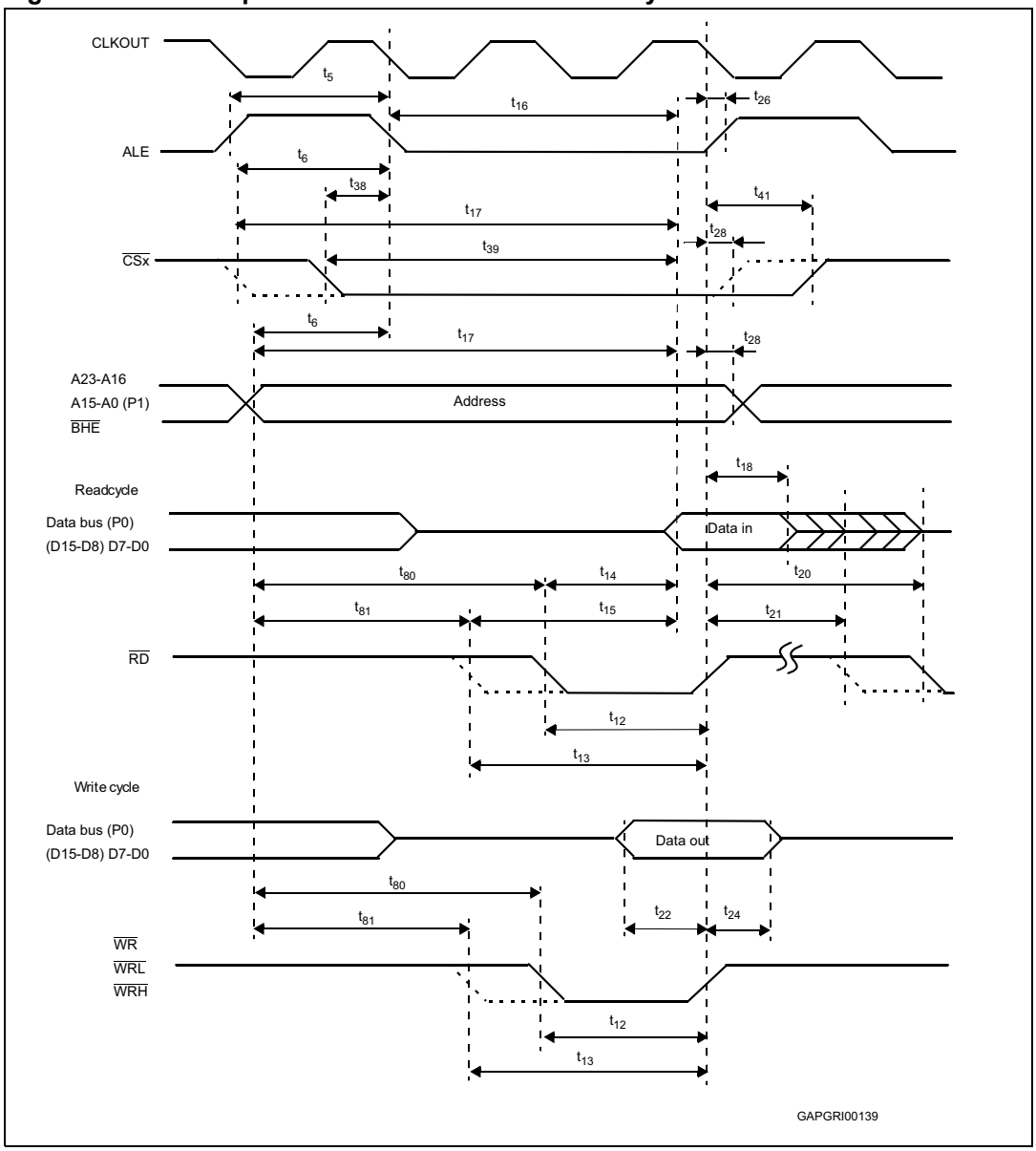
V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40 to +125°C, 4.5V ≤ V_{AREF} ≤ V_{DD},
V_{SS} ≤ V_{AGND} ≤ V_{SS} + 0.2V

Table 93. A/D converter characteristics

Symbol		Parameter	Test condition	Limit values		Unit
				Min.	Max.	
V_{AREF}	**SR**	Analog reference voltage(1)		4.5	V_{DD}	V
V_{AGND}	**SR**	Analog ground voltage		V_{SS}	V_{SS} + 0.2	V
V_{AIN}	**SR**	Analog Input voltage(2)		V_{AGND}	V_{AREF}	V
I_{AREF}	**CC**	Reference supply current	Running mode(3) Power Down mode	- -	5 1	mA µA
t_S	**CC**	Sample time	(4)	1	-	µs
t_C	**CC**	Conversion time	(5)	3	-	µs
DNL	**CC**	Differential nonlinearity(6)	No overload	-1	+1	LSB
INL	**CC**	Integral nonlinearity(6)	No overload	-1.5	+1.5	LSB
OFS	**CC**	Offset error(6)	No overload	-1.5	+1.5	LSB
TUE	**CC**	Total unadjusted error(6)	Port5 Port1 - No overload(3) Port1 - Overload(3)	-2.0 -5.0 -7.0	+2.0 +5.0 +7.0	LSB LSB LSB
K	**CC**	Coupling factor between inputs(3)(7)	On both Port5 and Port1	-	10^{-6}	-
C_{P1}	**CC**	Input pin capacitance(3)(8)		-	3	pF
C_{P2}	**CC**		Port5 Port1	-	4 6	pF pF
C_S	**CC**	Sampling capacitance(3)(8)		-	3.5	pF
R_{SW}	**CC**	Analog switch resistance(3)(8)	Port5 Port1	- -	600 1600	Ω Ω
R_{AD}	**CC**			-	1300	Ω

1. V_{AREF} can be tied to ground when A/D converter is not in use: An extra consumption (around 200µA) on main V_{DD} is added due to internal analog circuitry not completely turned off. Therefore, it is suggested to maintain the V_{AREF} at V_{DD} level even when not in use, and eventually switch off the A/D converter circuitry setting bit ADOFF in ADCON register.
2. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $0x000_H$ or $0x3FF_H$, respectively.
3. Not 100% tested, guaranteed by design characterization.
4. During the sample time, the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.
   Values for the sample clock t_S depend on programming and can be taken from *Table 94*.
5. This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result. Values for the conversion clock t_{CC} depend on programming and can be taken from next *Table 94*.

Figure 62. Demultiplexed bus with/without R/W delay and extended ALE



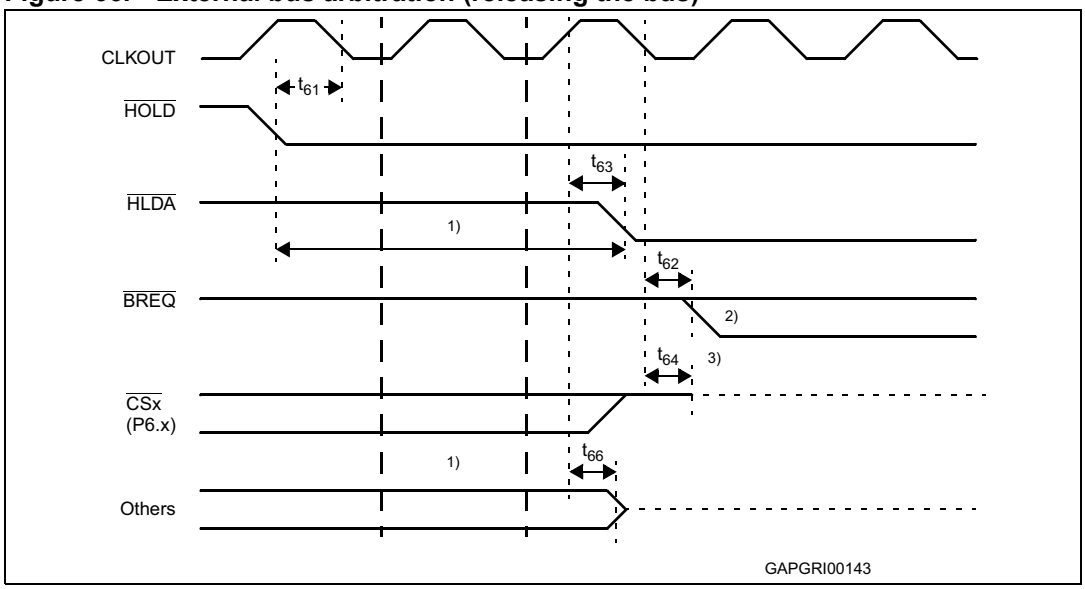
23.8.21 External bus arbitration

V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40 to +125°C, C_L = 50pF

Table 107. External bus arbitration

Symbol	Parameter	f_{CPU} = 40 MHz TCL = 12.5ns		Variable CPU Clock 1/2 TCL = 1 to 64 MHz		Unit
		Min.	Max.	Min.	Max.	
t_{61} **SR**	$\overline{HOLD}$ input setup time to CLKOUT	18.5	-	18.5	-	ns
t_{62} **CC**	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	-	12.5	-	12.5	
t_{63} **CC**	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay					
t_{64} **CC**	$\overline{CSx}$ release		20		20	
t_{65} **CC**	$\overline{CSx}$ drive	- 4	15	- 4	15	
t_{66} **CC**	Other signals release	-	20	-	20	
t_{67} **CC**	Other signals drive	- 4	15	- 4	15	

Figure 66. External bus arbitration (releasing the bus)



1. The ST10F276E will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.

Figure 70. PQFP144 mechanical data