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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	77
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 7x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0vll6r

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[2] ADC1_P[2] GPIO[22]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	54	76	92
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 — — —	— — — — ADC0_P[3] ADC1_P[3] GPIO[23]	— — — — ADC_0 ADC_1 SIUL	— — — — I I I	I	Tristate	55	77	93
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL[7] WKUP[25] ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKUP ADC_0 ADC_1	I — — — — I I I	I	—	39	53	61
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL[7] WKUP[26] ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKUP ADC_0 ADC_1	I — — — — I I I	I	—	38	52	60
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — —	GPIO[26] — — — WKUP[8][4] ADC0_S[2] ADC1_S[6]	SIUL — — — WKUP ADC_0 ADC_1	I/O — — — I I I	J	Tristate	40	54	62
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	J	Tristate	—	—	97
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	61	83	101

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	68	82
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	69	83
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	70	84
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	49	71	87
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	56	78	94
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	57	79	95
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	58	80	96
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	—	—	100

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	95	139	167
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC_0 SIUL	I/O I/O O O I	M	Tristate	96	140	168
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX E0UC[22] CAN3TX	SIUL FlexCAN_2 eMIOS_0 FlexCAN_3	I/O O I/O O	M	Tristate	9	13	21
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKUP[7][4] CAN2RX CAN3RX	SIUL — eMIOS_0 — WKUP FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	10	14	22
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 E1UC[30] EIRQ[10]	SIUL LINFlex_3 DSPI_1 eMIOS_1 SIUL	I/O O O I/O I	S	Tristate	11	15	23
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] E0UC[24] CS4_1 — LIN3RX WKUP[14][4]	SIUL eMIOS_0 DSPI_1 — LINFlex_3 WKUP	I/O I/O O — I I	S	Tristate	13	17	25
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — — —	GPIO[76] — E1UC[19][10] — EIRQ[11] SIN_2 ADC1_S[7]	SIUL — eMIOS_1 — SIUL DSPI_2 ADC_1	I/O — I/O — I I I	J	Tristate	76	109	133
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT_2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	103	127

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	J	Tristate	—	62	70
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	34	42
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — WKUP[22][4] CAN2RX CAN3RX	SIUL eMIOS_1 DSPI_0 — WKUP FlexCAN_2 FlexCAN_3	I/O I/O O — I I I	S	Tristate	—	33	41
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlex_4 eMIOS_1	I/O O O I/O	M	Tristate	—	38	46
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — WKUP[15][4] LIN4RX	SIUL DSPI_0 eMIOS_1 — WKUP LINFlex_4	I/O O I/O — I I	S	Tristate	—	39	47
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlex_5 —	I/O I/O O —	M	Tristate	—	35	43
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 — —	GPIO[93] E1UC[26] — — WKUP[16][4] LIN5RX	SIUL eMIOS_1 — — WKUP LINFlex_5	I/O I/O — — I I	S	Tristate	—	41	49
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_1	I/O O I/O O	M	Tristate	—	102	126

[4] All WKUP pins also support external interrupt capability. See the WKPU chapter of the *MPC5606BK Microcontroller Reference Manual* for further details.

[5] NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

[6] "Not applicable" because these functions are available only while the device is booting. See the BAM chapter of the *MPC5606BK Microcontroller Reference Manual* for details.

[7] Value of PCR.IBE bit must be 0.

[8] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

[9] PC[1] is a fast/medium pad but is in medium configuration by default. This pad is in Alternate Function 2 mode after reset which has TDO functionality. The reset value of PCR.OBE is 1, but this setting has no impact as long as this pad stays in AF2 mode. After configuring this pad as GPIO (PCR.PA = 0), output buffer is enabled as reset value of PCR.OBE = 1.

[10] Not available in 100LQFP package.

Table 3. Pad types

Type	Description
F	Fast
I	Input only with analog feature
J	Input/output with analog feature
M	Medium
S	Slow

3 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 4 are used and the parameters are tagged accordingly in the tables where appropriate.

Table 4. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the *MPC5606BK Microcontroller Reference Manual*.

3.2.1 NVUSRO[PAD3V5V] field description

Table 5 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 5. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 6 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 6. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	3.0[7]	0.25 V/µs	V/s

3.5 Thermal characteristics

3.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in Table 11 LQFP thermal characteristics, considering a thermal resistance of 144 LQFP as 48.3 °C/W, at ambient temperature T_A = 125 °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than (150 – 125)/48.3 = 517 mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD\_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in Section 3.5.2, Package thermal characteristics, it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV}) < 80$ mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD\_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV}. For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 ms/V. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage monitor generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD\_BV})$ possible across the external resistor.

3.5.2 Package thermal characteristics

Table 11. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board — 1s	100	—	—	64	°C/W
					144	—	—	64	
					176	—	—	64	
				Four-layer board — 2s2p	100	—	—	49.7	
					144	—	—	48.3	
					176	—	—	47.3	
$R_{\theta JB}$	CC		Thermal resistance, junction-to-board[4]	Single-layer board — 1s	100	—	—	36	°C/W
					144	—	—	38	
					176	—	—	38	
				Four-layer board — 2s2p	100	—	—	33.6	
					144	—	—	33.4	
					176	—	—	33.4	

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
1	—	—	PH[15]	2%	3%	3%	3%	—	—	—	—
	—	—	PH[13]	3%	4%	3%	4%	—	—	—	—
	—	—	PH[14]	3%	4%	4%	4%	—	—	—	—
	—	—	PI[6]	4%	—	4%	—	—	—	—	—
	—	—	PI[7]	4%	—	4%	—	—	—	—	—
	4	—	PG[5]	4%	—	5%	—	10%	—	12%	—
		—	PG[4]	4%	6%	5%	5%	9%	13%	11%	12%
		—	PG[3]	4%	—	5%	—	9%	—	11%	—
		—	PG[2]	4%	6%	5%	5%	9%	12%	10%	11%
		4	PA[2]	4%	—	5%	—	8%	—	10%	—
			PE[0]	4%	—	5%	—	8%	—	9%	—
			PA[1]	4%	—	5%	—	8%	—	9%	—
			PE[1]	4%	6%	5%	6%	7%	10%	9%	9%
			PE[8]	4%	6%	5%	6%	7%	10%	8%	9%
			PE[9]	4%	—	5%	—	6%	—	8%	—
			PE[10]	4%	—	5%	—	6%	—	7%	—
			PA[0]	4%	6%	5%	5%	6%	8%	7%	7%
			PE[11]	4%	—	5%	—	5%	—	6%	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PC[0]	6%	9%	7%	8%	7%	10%	8%	8%
			PH[9]	7%	—	8%	—	7%	—	9%	—
			PE[2]	7%	10%	8%	9%	8%	11%	9%	10%
			PE[3]	7%	10%	9%	9%	8%	12%	10%	10%
			PC[5]	7%	11%	9%	9%	8%	12%	10%	11%
			PC[4]	8%	11%	9%	10%	9%	13%	10%	11%
			PE[4]	8%	11%	9%	10%	9%	13%	11%	12%
			PE[5]	8%	11%	10%	10%	9%	14%	11%	12%
		—	PH[4]	8%	12%	10%	10%	10%	14%	12%	12%
		—	PH[5]	8%	—	10%	—	10%	—	12%	—
		—	PH[6]	8%	12%	10%	11%	10%	15%	12%	13%
		—	PH[7]	9%	12%	10%	11%	11%	15%	13%	13%
		—	PH[8]	9%	12%	10%	11%	11%	16%	13%	14%
		4	PE[6]	9%	12%	10%	11%	11%	16%	13%	14%
			PE[7]	9%	12%	10%	11%	11%	16%	14%	14%
	—	—	PI[3]	9%	—	10%	—	—	—	—	—
	—	—	PI[2]	9%	—	10%	—	—	—	—	—
	—	—	PI[1]	9%	—	10%	—	—	—	—	—
	—	—	PI[0]	9%	—	10%	—	—	—	—	—
	4	4	PC[12]	8%	12%	10%	11%	12%	18%	15%	16%
			PC[13]	8%	—	10%	—	13%	—	15%	—
			PC[8]	8%	—	10%	—	13%	—	15%	—
			PB[2]	8%	11%	9%	10%	13%	18%	15%	16%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 SRC is the Slew Rate Control bit in SIU_PCR*x*

3.7 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

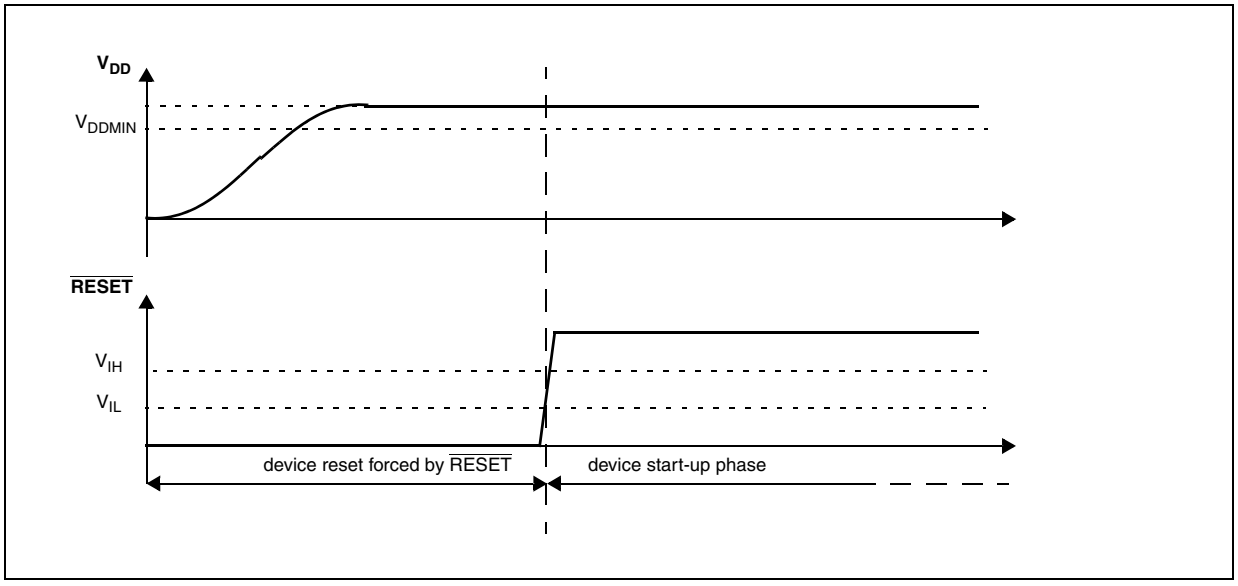


Figure 6. Start-up reset requirements

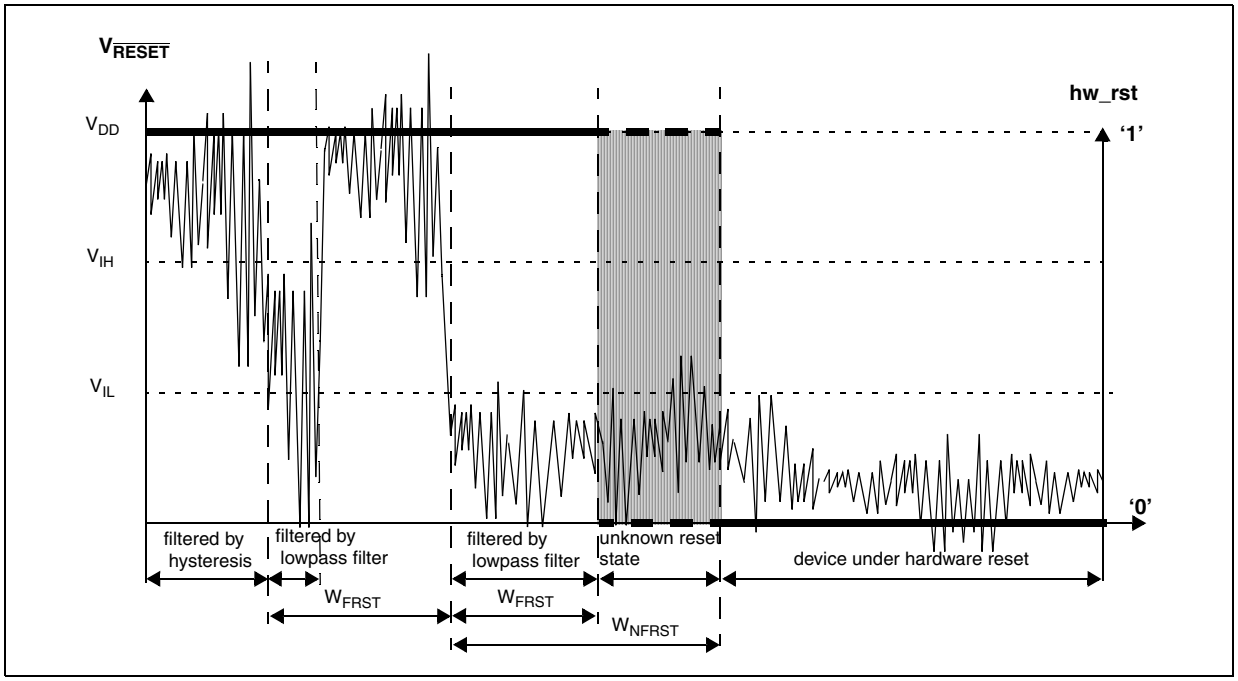


Figure 7. Noise filtering on reset signal

Table 21. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V

Table 28. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions[1]		Value			Unit
					Min	Typ	Max	
I_{CFREAD}	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 64 MHz[2]	Code Flash	—	—	33	mA
I_{DFREAD}				Data Flash	—	—	33	
I_{CFMOD}	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program /Erase on-going while reading Flash registers f_{CPU} = 64 MHz[2]	Code Flash	—	—	52	mA
I_{DFMOD}				Data Flash	—	—	33	
I_{CFLPW}	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I_{DFLPW}				Data Flash	—	—	900	µA
I_{CFPWD}	CC	Sum of the current consumption on V_{DDHV} and V_{DDBV} during Flash power down mode	—	Code Flash	—	—	150	µA
I_{DFPWD}				Data Flash	—	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 f_{CPU} 64 MHz can be achieved at up to 125 °C.

3.10.3 Start-up/Switch-off timings

Table 29. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$T_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	—	—	—	125	µs
$T_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	—	—	—	0.5	
$T_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	—	—	—	30	
$T_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	—	—	—	0.5	
$T_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	—	—	—	1.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

3.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

- Software recommendations – The software flowchart must include the management of runaway conditions such as:
  - — Corrupted program counter
  - — Unexpected reset
  - — Critical data corruption (control registers...)
- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

3.11.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC61967-1 standard, which specifies the general conditions for EMI measurements.

Table 30. EMI radiated emission measurement[1,2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150		1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	64	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP144 package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 64 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

3.11.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

3.11.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts×(n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
T_{FIRCSU}	CC	C	Fast internal RC oscillator start-up time	V_{DD} = 5.0 V ± 10%	—	1.1	2.0	µs
$\Delta_{FIRCPRE}$	CC	C	Fast internal RC oscillator precision after software trimming of f_{FIRC}	T_A = 25 °C	–1	—	1	%
$\Delta_{FIRCTRIM}$	CC	C	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6		%
$\Delta_{FIRCVAR}$	CC	C	Fast internal RC oscillator variation over temperature and supply with respect to f_{FIRC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.16 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz low power internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SIRC}	CC	P	Slow internal RC oscillator low frequency	T_A = 25 °C, trimmed	—	128	—	kHz
	SR	—		—	100	—	150	
I_{SIRC}[2],	CC	C	Slow internal RC oscillator low frequency current	T_A = 25 °C, trimmed	—	—	5	µA
T_{SIRCSU}	CC	P	Slow internal RC oscillator start-up time	T_A = 25 °C, V_{DD} = 5.0 V ± 10%	—	8	12	µs
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

3.17 ADC electrical characteristics

3.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

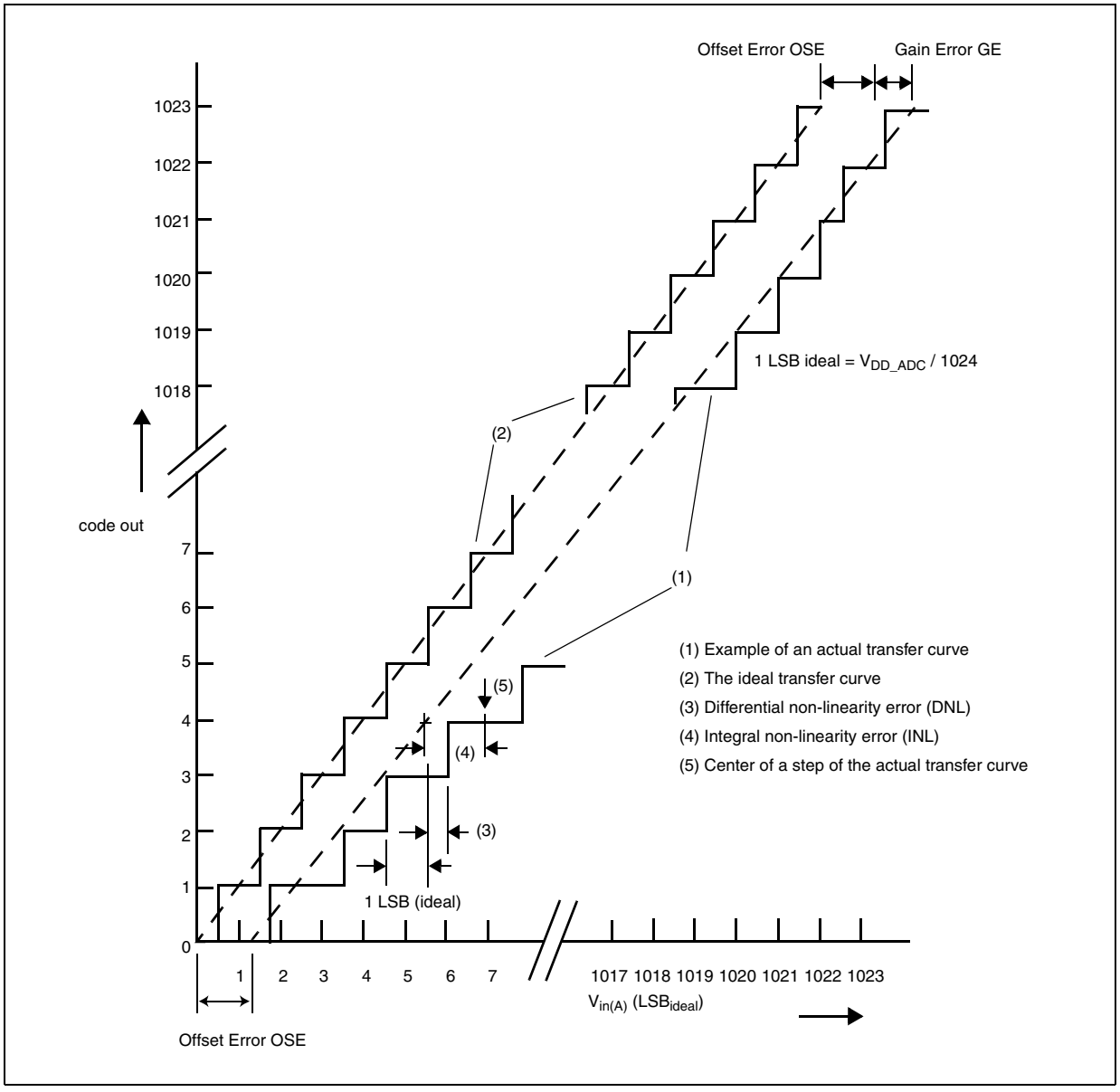


Figure 17. ADC_0 characteristic and error definitions

3.17.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as antialiasing.

Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sample time[4] VDD = 3.3 V	f_{ADC1} = 20 MHz, ADC1_conf_sample_input = 12	600	—	—	ns
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 17	500	—	—	
			Sample time[4] VDD = 3.3 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	µs
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] VDD = 3.3 V	f_{ADC1} = 20MHz, ADC1_conf_comp = 0	2.4	—	—	µs
			Conversion time[5] VDD = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, ADC1_conf_comp = 0	1.5	—	—	µs
			Conversion time[5] VDD = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
			Conversion time[5] VDD = 5.0 V	f_{ADC1} = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Table 43. On-chip peripherals current consumption[1] (continued)

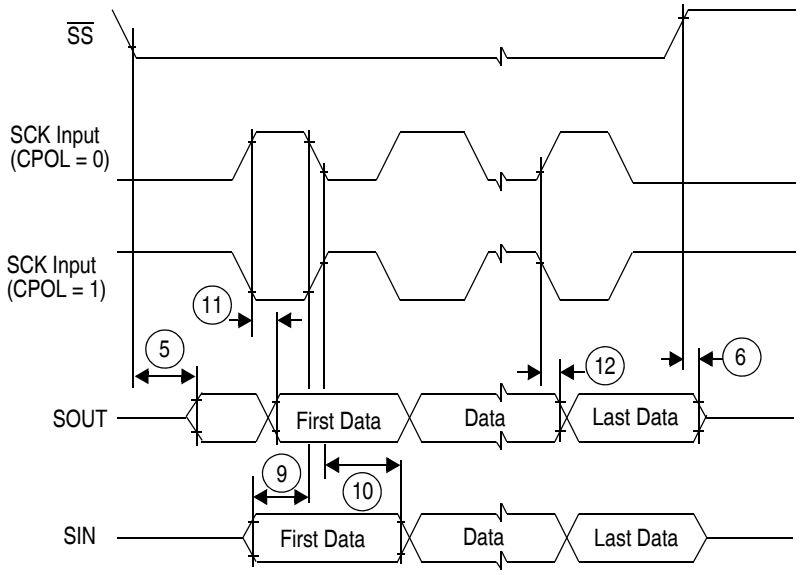
Symbol		C	Parameter	Conditions		Value	Unit
						Typ	
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_BV(PLL)}$	CC	T	PLL supply current on V_{DD_BV}	V_{DD} = 5.5 V	—	2.5	mA

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz

3.18.2 DSPI characteristics

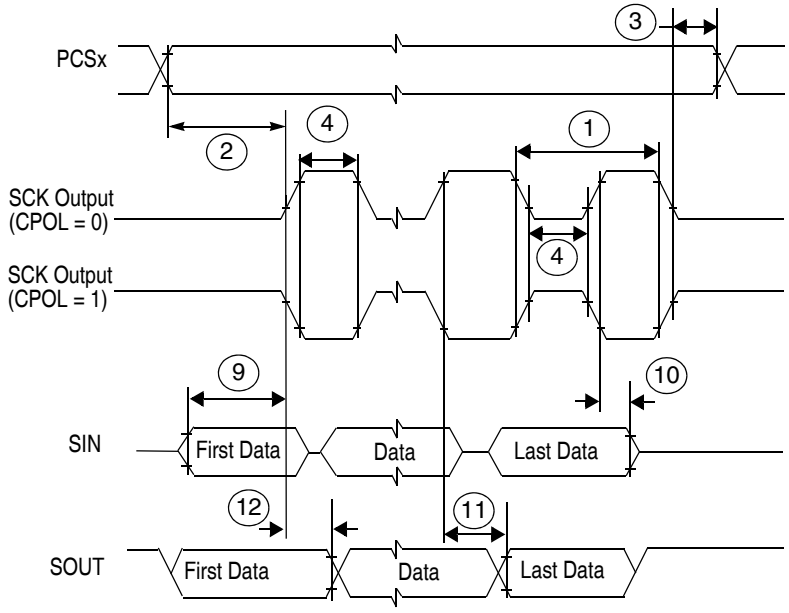
Table 44. DSPI characteristics[1]

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI5/DSPI6			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t_{SCK}	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333[2]	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	145	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	145	—	—	
—	f_{DSPI}	SR	D	DSPI digital controller frequency		—	—	f_{CPU}	—	—	f_{CPU}	MHz
2	t_{CSCext}[3]	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t_{ASCext}[4]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI} + 5$	—	—	$1/f_{DSPI} + 5$	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	Slave mode	—	—	$1/f_{DSPI} + 70$	—	—	$1/f_{DSPI} + 130$	ns
6	t_{DI}	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
7	t_{PCSC}	CC	D	PCS*x* to $\overline{PCSS}$ time	—	13[5]	—	—	13[5]	—	—	
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCS*x* time	—	13[5]	—	—	13[5]	—	—	
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2[6]	—	—	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	



Note: Numbers shown reference Table 44.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Numbers shown reference Table 44.

Figure 27. DSPI modified transfer format timing — master, CPHA = 0