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What is "Embedded - Microcontrollers"?

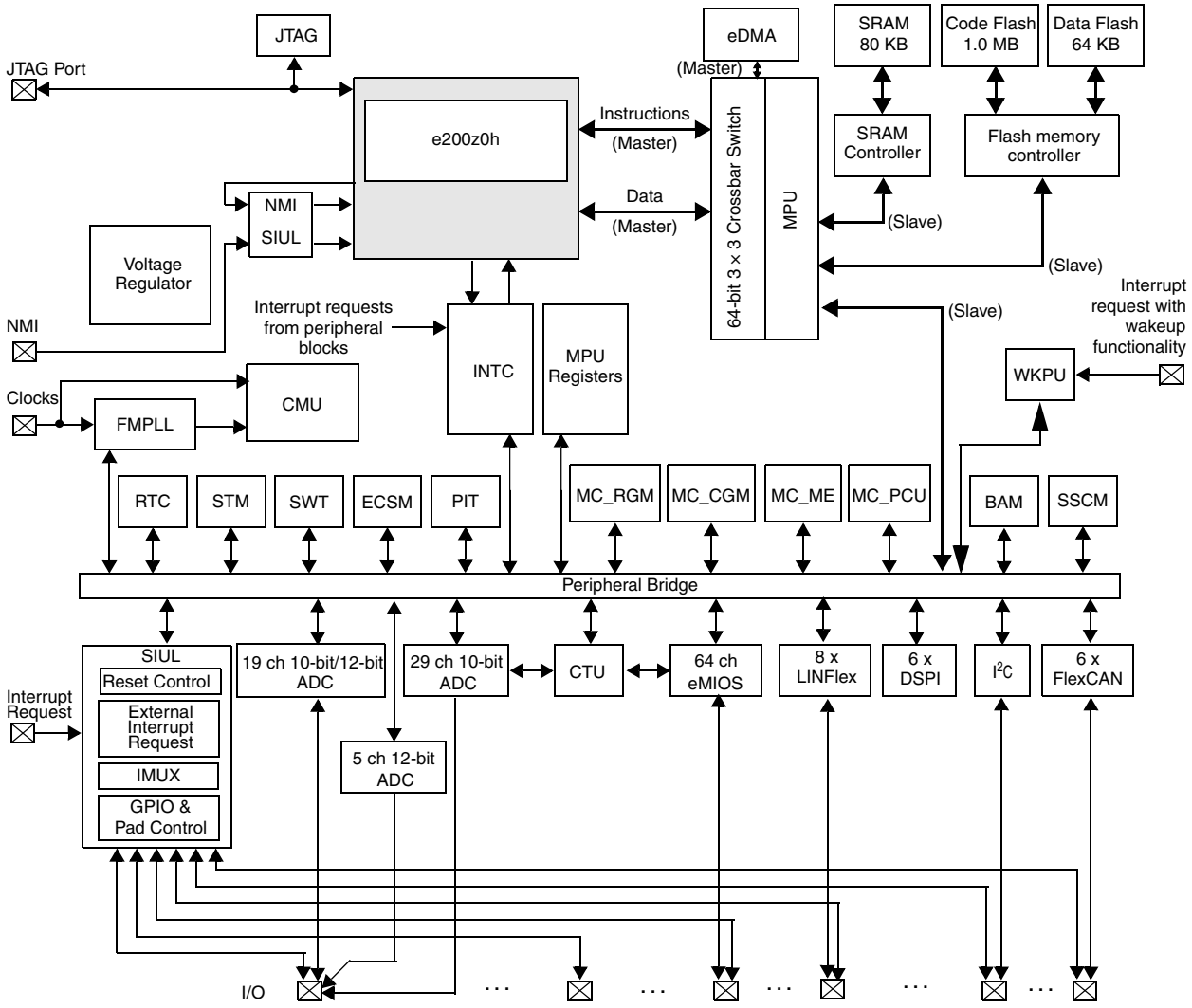
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0vlq6

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5606BK.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
FlexCAN	Controller Area Network
CFlash	Code flash memory
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DFlash	Data flash memory
DSPI	Deserial Serial Peripheral Interface
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
FMPLL	Frequency-Modulated Phase-Locked Loop
I^2C	Inter-integrated Circuit Bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MPU	Memory Protection Unit
NMI	Non-Maskable Interrupt
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit

Figure 1. MPC5606BK block diagram

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	68	82
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	69	83
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	70	84
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	49	71	87
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	56	78	94
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	57	79	95
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	58	80	96
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	—	—	100

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	140
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O I/O —	M	Tristate	—	—	141
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O —	M	Tristate	—	—	9
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O I/O —	M	Tristate	—	—	10
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — —	M	Tristate	—	—	8
Port I										
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	172
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKUP[24][4] —	SIUL eMIOS_0 — — WKUP —	I/O I/O — — I —	S	Tristate	—	—	171
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	170
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKUP[23][4] —	SIUL eMIOS_0 — — WKUP —	I/O I/O — — I —	S	Tristate	—	—	169
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	143

Table 4. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the *MPC5606BK Microcontroller Reference Manual*.

3.2.1 NVUSRO[PAD3V5V] field description

Table 5 shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 5. PAD3V5V field description[1]

Value[2]	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

3.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

Table 6 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 6. OSCILLATOR_MARGIN field description[1]

Value[2]	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is ‘1’. This value can be programmed by the customer in Shadow Flash.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value.

3.2.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 7 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 7. WATCHDOG_EN field description[1]

Value[2]	Description
0	Disable after reset
1	Enable after reset

1 See the *MPC5606BK Microcontroller Reference Manual* for more information on the NVUSRO register.

2 The default manufacturing value is '1'. This value can be programmed by the customer in Shadow Flash.

3.3 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	–0.3	6.0	V
V_{SS_LV}	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	—	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$T_{A\ C\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	85	°C
$T_{J\ C\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	110	
$T_{A\ V\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	105	
$T_{J\ V\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	130	
$T_{A\ M\text{-}Grade\ Part}$	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	125	
$T_{J\ M\text{-}Grade\ Part}$	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

3 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on VDD_BV should always be faster or equal to slope of VDD_HV. Otherwise, device may enter regulator bypass mode if slope on VDD_BV is slower.

4 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/O DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, the device is reset.

6 Guaranteed by device validation

7 Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

8 This frequency includes the 4% frequency modulation guard band.

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
V_{SS_LV}[3]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[4]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	3.0	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_ADC}[5]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop[2]	3.0	5.5	
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	3.0[7]	0.25 V/µs	V/s
T_{A} C-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	85	°C
T_{J} C-Grade Part	SR	Junction temperature under bias	—	–40	110	
T_{A} V-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	105	
T_{J} V-Grade Part	SR	Junction temperature under bias	—	–40	130	
T_{A} M-Grade Part	SR	Ambient temperature under bias	f_{CPU} < 64 MHz[8]	–40	125	
T_{J} M-Grade Part	SR	Junction temperature under bias	—	–40	150	

1 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.

2 Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.

4 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD\_HV}$ in order to ensure the device does not enter regulator bypass mode.

5 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.

6 Guaranteed by device validation. Please refer to Section 3.5.1, External ballast resistor recommendations for minimum V_{DD} slope to be guaranteed to ensure correct power up in case of external resistor usage.

7 Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

8 This frequency includes the 4% frequency modulation guard band.

NOTE

RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

3.5 Thermal characteristics

3.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in Table 11 LQFP thermal characteristics, considering a thermal resistance of 144 LQFP as 48.3 °C/W, at ambient temperature T_A = 125 °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than (150 – 125)/48.3 = 517 mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD\_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in Section 3.5.2, Package thermal characteristics, it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV}) < 80$ mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD\_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV}. For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 ms/V. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage monitor generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD\_BV})$ possible across the external resistor.

3.5.2 Package thermal characteristics

Table 11. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board — 1s	100	—	—	64	°C/W
					144	—	—	64	
					176	—	—	64	
				Four-layer board — 2s2p	100	—	—	49.7	
					144	—	—	48.3	
					176	—	—	47.3	
$R_{\theta JB}$	CC		Thermal resistance, junction-to-board[4]	Single-layer board — 1s	100	—	—	36	°C/W
					144	—	—	38	
					176	—	—	38	
				Four-layer board — 2s2p	100	—	—	33.6	
					144	—	—	33.4	
					176	—	—	33.4	

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.6 I/O pad electrical characteristics

3.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads — are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads — provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads — provide maximum speed. These are used for improved debugging capability.
- Input only pads — are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.6.2 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in Figure 5.

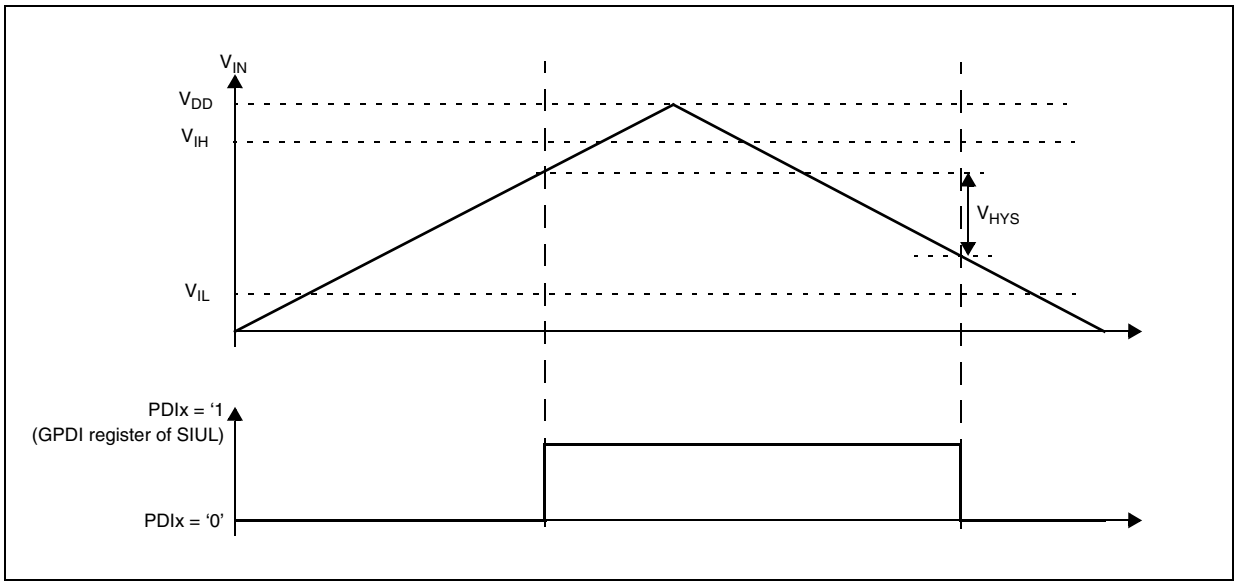


Figure 5. I/O input DC electrical characteristics definition

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
1	—	—	PH[15]	2%	3%	3%	3%	—	—	—	—
	—	—	PH[13]	3%	4%	3%	4%	—	—	—	—
	—	—	PH[14]	3%	4%	4%	4%	—	—	—	—
	—	—	PI[6]	4%	—	4%	—	—	—	—	—
	—	—	PI[7]	4%	—	4%	—	—	—	—	—
	4	—	PG[5]	4%	—	5%	—	10%	—	12%	—
		—	PG[4]	4%	6%	5%	5%	9%	13%	11%	12%
		—	PG[3]	4%	—	5%	—	9%	—	11%	—
		—	PG[2]	4%	6%	5%	5%	9%	12%	10%	11%
		4	PA[2]	4%	—	5%	—	8%	—	10%	—
			PE[0]	4%	—	5%	—	8%	—	9%	—
			PA[1]	4%	—	5%	—	8%	—	9%	—
			PE[1]	4%	6%	5%	6%	7%	10%	9%	9%
			PE[8]	4%	6%	5%	6%	7%	10%	8%	9%
			PE[9]	4%	—	5%	—	6%	—	8%	—
			PE[10]	4%	—	5%	—	6%	—	7%	—
			PA[0]	4%	6%	5%	5%	6%	8%	7%	7%
			PE[11]	4%	—	5%	—	5%	—	6%	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
2	1	—	PG[9]	9%	—	10%	—	9%	—	10%	—
		—	PG[8]	9%	—	11%	—	9%	—	11%	—
		1	PC[11]	9%	—	11%	—	9%	—	11%	—
			PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
		—	PG[7]	9%	—	11%	—	9%	—	11%	—
		—	PG[6]	10%	14%	11%	12%	10%	14%	11%	12%
		1	PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
			PB[1]	10%	—	12%	—	10%	—	12%	—
		—	PF[9]	10%	—	12%	—	10%	—	12%	—
		—	PF[8]	10%	14%	12%	13%	10%	14%	12%	13%
		—	PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
		1	PC[6]	10%	—	12%	—	10%	—	12%	—
			PC[7]	10%	—	12%	—	10%	—	12%	—
		—	PF[10]	10%	14%	11%	12%	10%	14%	11%	12%
		—	PF[11]	9%	—	11%	—	9%	—	11%	—
		1	PA[15]	8%	12%	10%	10%	8%	12%	10%	10%
		—	PF[13]	8%	—	10%	—	8%	—	10%	—
		1	PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
			PA[4]	7%	—	9%	—	7%	—	9%	—
			PA[13]	7%	10%	8%	9%	7%	10%	8%	9%
			PA[12]	7%	—	8%	—	7%	—	8%	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
3	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	5%	—	6%	—	6%	—	7%	—
		—	PF[0]	5%	—	6%	—	6%	—	8%	—
		—	PF[1]	5%	—	6%	—	7%	—	8%	—
		—	PF[2]	6%	—	7%	—	7%	—	9%	—
		—	PF[3]	6%	—	7%	—	8%	—	9%	—
		—	PF[4]	6%	—	7%	—	8%	—	10%	—
		—	PF[5]	6%	—	7%	—	9%	—	10%	—
		—	PF[6]	6%	—	7%	—	9%	—	11%	—
		—	PF[7]	6%	—	7%	—	9%	—	11%	—
	—	—	PJ[3]	6%	—	7%	—	—	—	—	—
	—	—	PJ[2]	6%	—	7%	—	—	—	—	—
	—	—	PJ[1]	6%	—	7%	—	—	—	—	—
	—	—	PJ[0]	6%	—	7%	—	—	—	—	—
	—	—	PI[15]	6%	—	7%	—	—	—	—	—
	—	—	PI[14]	6%	—	7%	—	—	—	—	—
	2	2	PD[0]	1%	—	1%	—	1%	—	1%	—
			PD[1]	1%	—	1%	—	1%	—	1%	—
			PD[2]	1%	—	1%	—	1%	—	1%	—
			PD[3]	1%	—	1%	—	1%	—	1%	—
			PD[4]	1%	—	1%	—	1%	—	1%	—
			PD[5]	1%	—	1%	—	1%	—	1%	—
			PD[6]	1%	—	1%	—	1%	—	2%	—
			PD[7]	1%	—	1%	—	1%	—	2%	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
5	3	—	PF[15]	4%	—	4%	—	4%	—	4%	—
		—	PF[14]	4%	6%	5%	5%	4%	6%	5%	5%
		—	PE[13]	4%	—	5%	—	4%	—	5%	—
		3	PA[7]	5%	—	6%	—	5%	—	6%	—
			PA[8]	5%	—	6%	—	5%	—	6%	—
			PA[9]	6%	—	7%	—	6%	—	7%	—
			PA[10]	6%	—	8%	—	6%	—	8%	—
			PA[11]	8%	—	9%	—	8%	—	9%	—
			PE[12]	8%	—	9%	—	8%	—	9%	—
		—	PG[14]	8%	—	9%	—	8%	—	9%	—
		—	PG[15]	8%	11%	9%	10%	8%	11%	9%	10%
		—	PE[14]	8%	—	9%	—	8%	—	9%	—
		—	PE[15]	8%	11%	9%	10%	8%	11%	9%	10%
		—	PG[10]	8%	—	9%	—	8%	—	9%	—
		—	PG[11]	7%	11%	9%	9%	7%	11%	9%	9%
	—	—	PH[11]	7%	10%	9%	9%	—	—	—	—
	—	—	PH[12]	7%	10%	8%	9%	—	—	—	—
	—	—	PI[5]	7%	—	8%	—	—	—	—	—
	—	—	PI[4]	7%	—	8%	—	—	—	—	—
	3	3	PC[3]	6%	—	8%	—	6%	—	8%	—
			PC[2]	6%	8%	7%	7%	6%	8%	7%	7%
			PA[5]	6%	8%	7%	7%	6%	8%	7%	7%
			PA[6]	5%	—	6%	—	5%	—	6%	—
			PH[10]	5%	7%	6%	6%	5%	7%	6%	6%
			PC[1]	5%	19%	5%	13%	5%	19%	5%	13%

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PC[0]	6%	9%	7%	8%	7%	10%	8%	8%
			PH[9]	7%	—	8%	—	7%	—	9%	—
			PE[2]	7%	10%	8%	9%	8%	11%	9%	10%
			PE[3]	7%	10%	9%	9%	8%	12%	10%	10%
			PC[5]	7%	11%	9%	9%	8%	12%	10%	11%
			PC[4]	8%	11%	9%	10%	9%	13%	10%	11%
			PE[4]	8%	11%	9%	10%	9%	13%	11%	12%
			PE[5]	8%	11%	10%	10%	9%	14%	11%	12%
		—	PH[4]	8%	12%	10%	10%	10%	14%	12%	12%
		—	PH[5]	8%	—	10%	—	10%	—	12%	—
		—	PH[6]	8%	12%	10%	11%	10%	15%	12%	13%
		—	PH[7]	9%	12%	10%	11%	11%	15%	13%	13%
		—	PH[8]	9%	12%	10%	11%	11%	16%	13%	14%
		4	PE[6]	9%	12%	10%	11%	11%	16%	13%	14%
			PE[7]	9%	12%	10%	11%	11%	16%	14%	14%
	—	—	PI[3]	9%	—	10%	—	—	—	—	—
	—	—	PI[2]	9%	—	10%	—	—	—	—	—
	—	—	PI[1]	9%	—	10%	—	—	—	—	—
	—	—	PI[0]	9%	—	10%	—	—	—	—	—
	4	4	PC[12]	8%	12%	10%	11%	12%	18%	15%	16%
			PC[13]	8%	—	10%	—	13%	—	15%	—
			PC[8]	8%	—	10%	—	13%	—	15%	—
			PB[2]	8%	11%	9%	10%	13%	18%	15%	16%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 SRC is the Slew Rate Control bit in SIU_PCR*x*

3.7 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

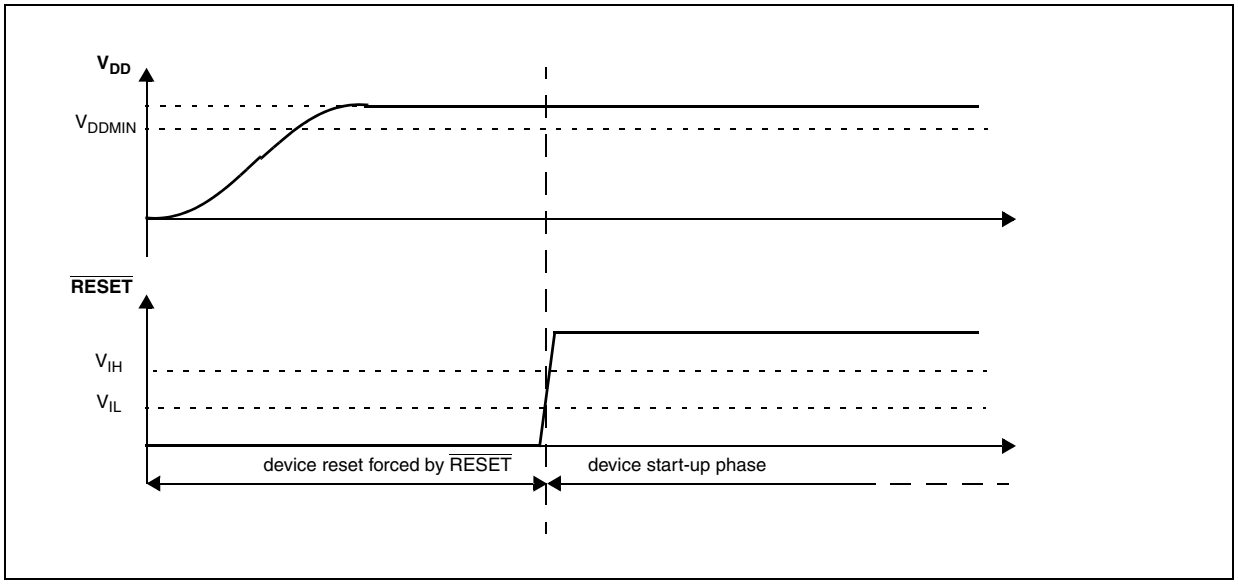


Figure 6. Start-up reset requirements

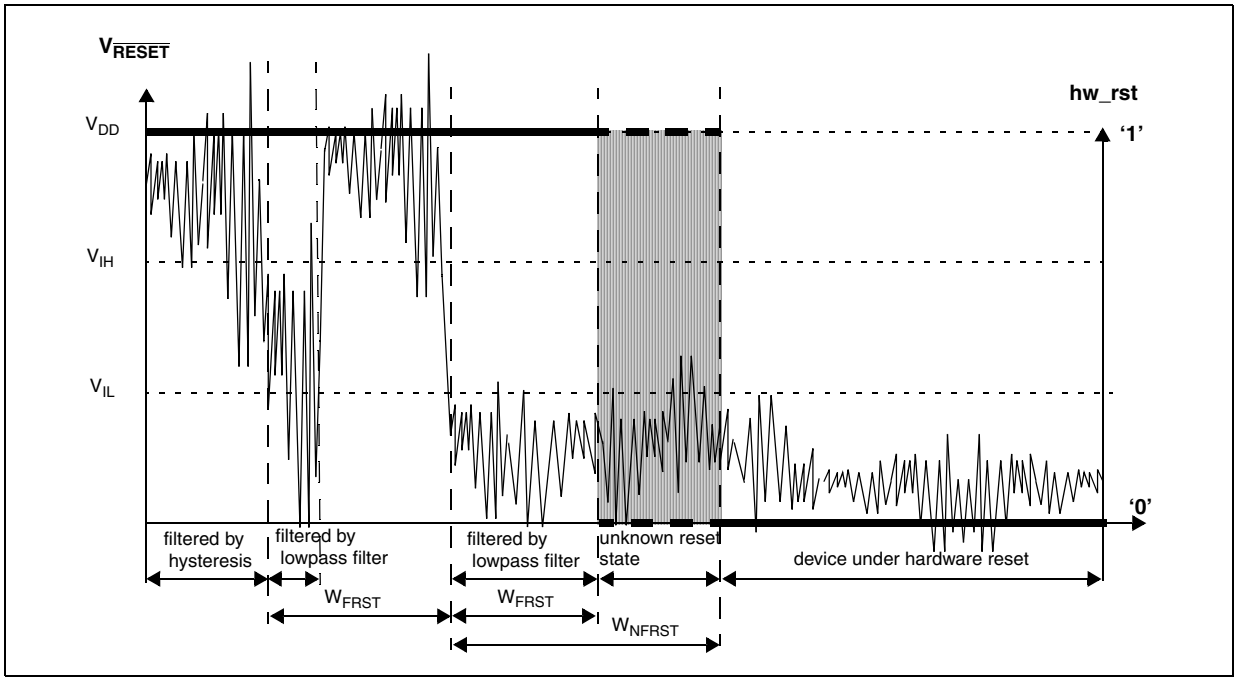


Figure 7. Noise filtering on reset signal

Table 21. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

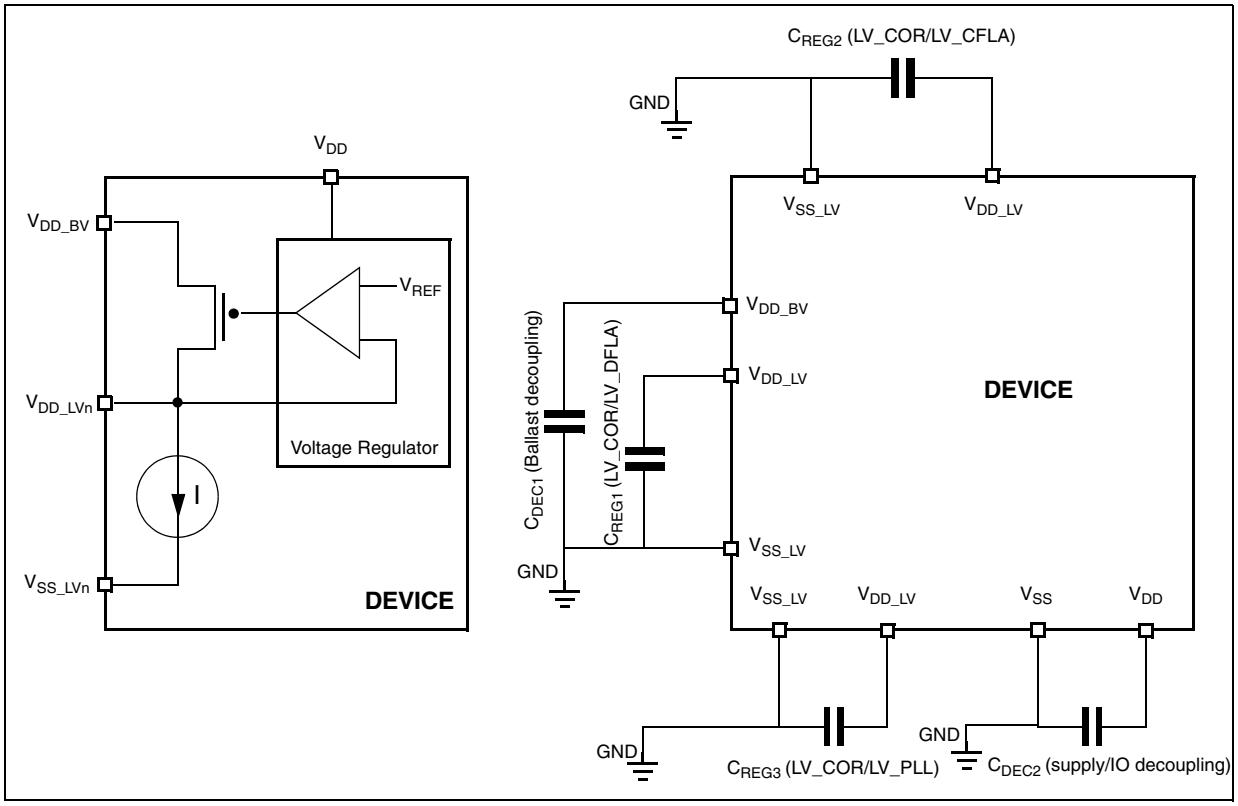


Figure 8. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

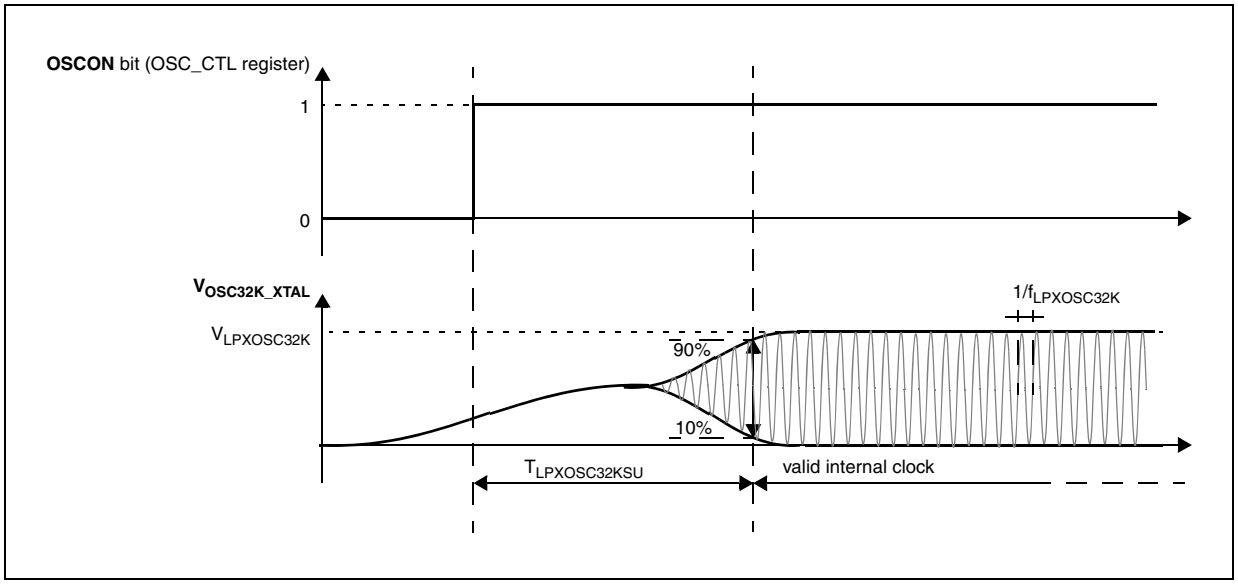


Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 36. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the FXOSC or FIRC sources.

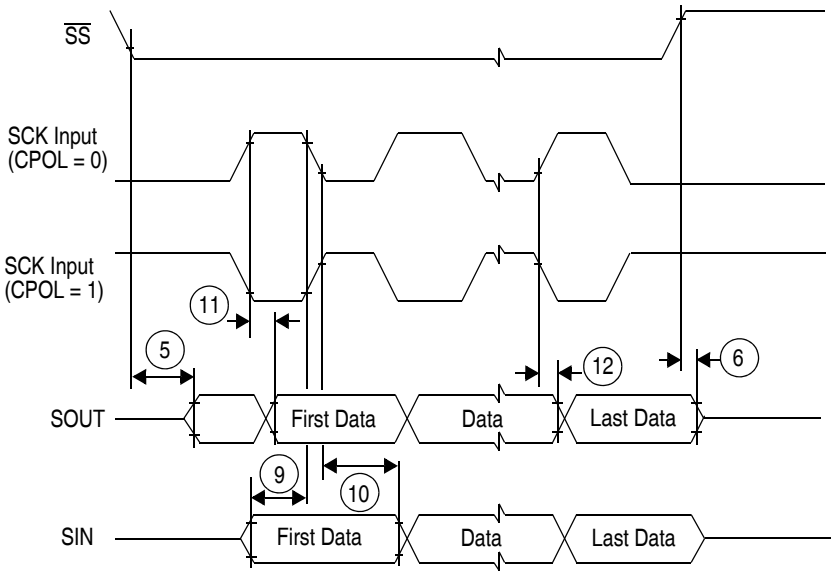
Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%

Table 43. On-chip peripherals current consumption[1] (continued)

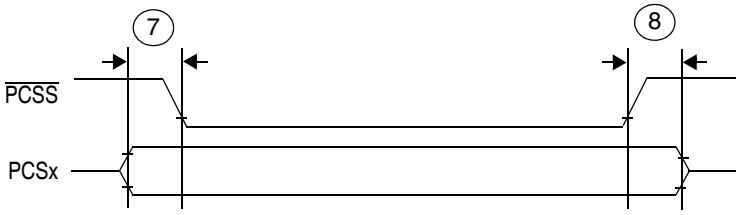
Symbol		C	Parameter	Conditions		Value	Unit
						Typ	
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_BV(PLL)}$	CC	T	PLL supply current on V_{DD_BV}	V_{DD} = 5.5 V	—	2.5	mA

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz



Note: Numbers shown reference Table 44.

Figure 30. DSPI modified transfer format timing — slave, CPHA = 1



Note: Numbers shown reference Table 44.

Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.18.3 JTAG characteristics

Table 45. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns

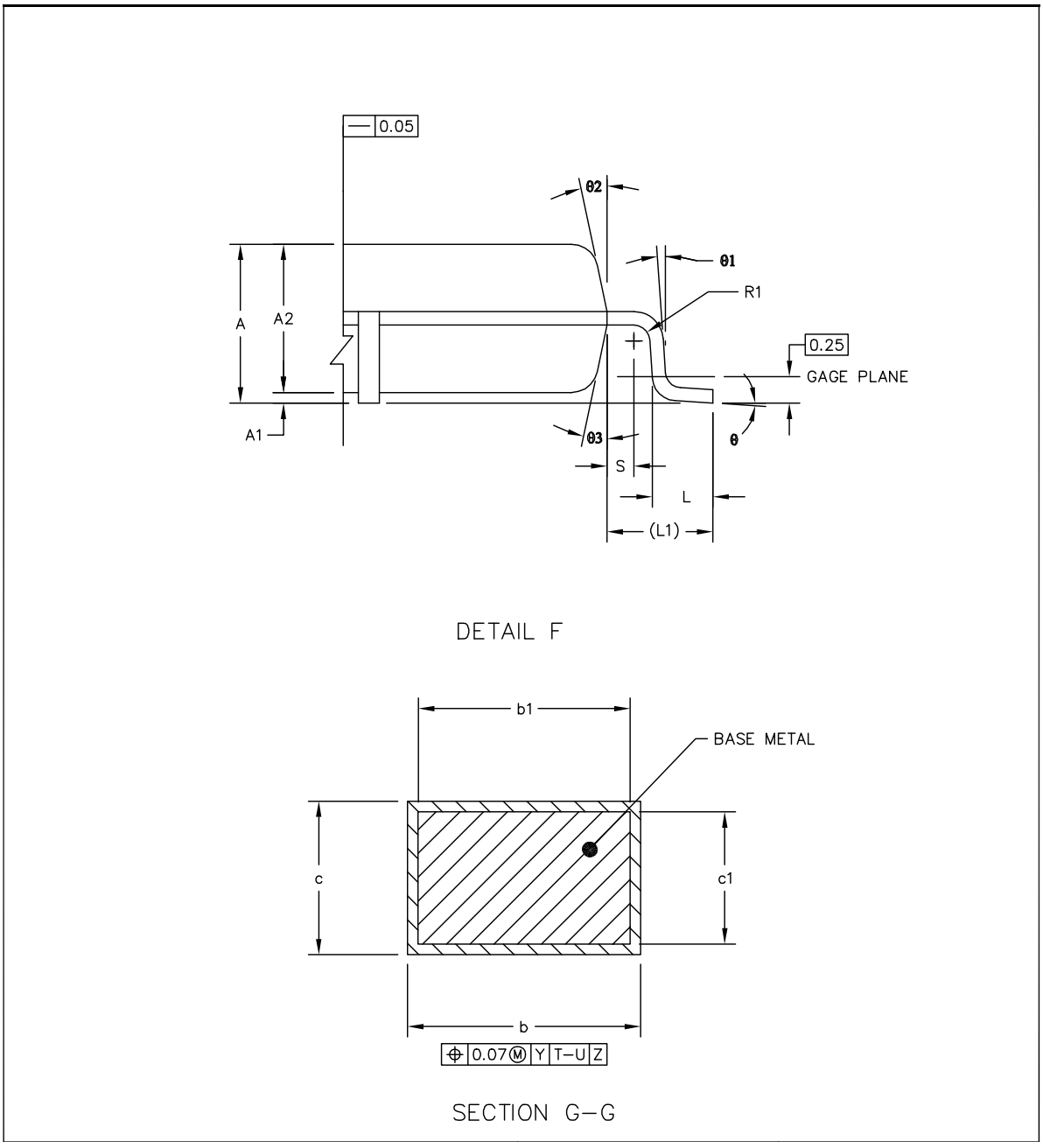


Figure 34. 176 LQFP package mechanical drawing (Part 2 of 3)