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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 15x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0vlq6r

2 Package pinouts and signal descriptions

2.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please see Table 2.

Figure 2 shows the MPC5606BK in the 176 LQFP package.

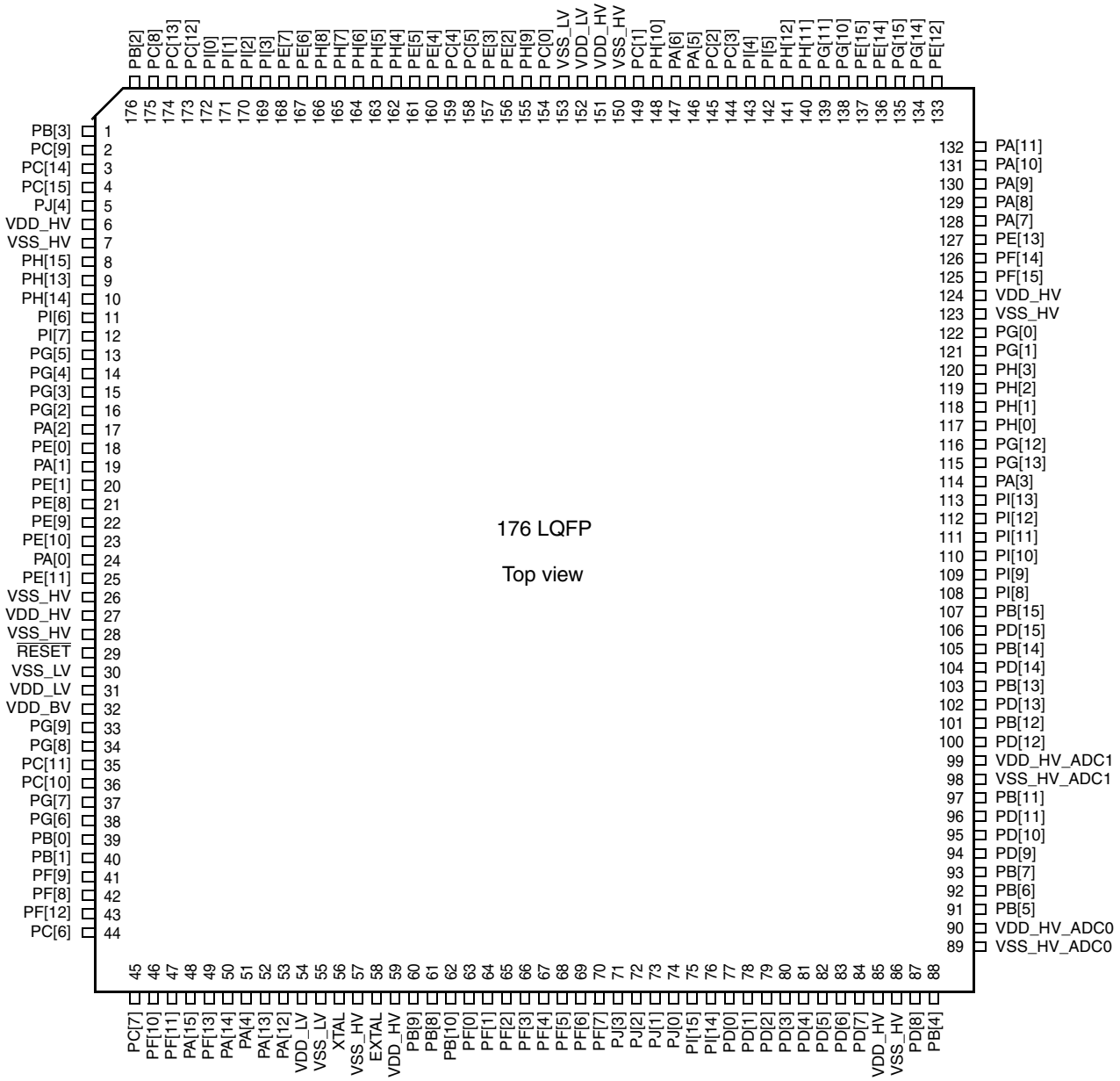


Figure 2. 176 LQFP pinout

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlex_3 — SIUL ADC_1	I/O I/O O — I I	J	Tristate	71	104	128
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	105	129
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I^2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	108	132
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	31	45	53
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M	Tristate	30	44	52
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	28	42	50

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	68	82
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	69	83
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	70	84
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 — —	GPIO[56] — — — ADC0_P[12] ADC1_P[12]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	49	71	87
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 — —	GPIO[57] — — — ADC0_P[13] ADC1_P[13]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	56	78	94
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 — —	GPIO[58] — — — ADC0_P[14] ADC1_P[14]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	57	79	95
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 — —	GPIO[59] — — — ADC0_P[15] ADC1_P[15]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	58	80	96
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	—	—	100

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	112	136
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	113	137
Port F										
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ADC0_S[8]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	55	63
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ADC0_S[9]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	56	64
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ADC0_S[10]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	57	65
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	58	66
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	59	67
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	60	68
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	61	69

K is a constant for the particular part, which may be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations 1 and 2 iteratively for any value of T_A.

3.6 I/O pad electrical characteristics

3.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads — are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads — provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads — provide maximum speed. These are used for improved debugging capability.
- Input only pads — are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

3.6.2 I/O input DC characteristics

Table 12 provides input DC electrical characteristics as described in Figure 5.

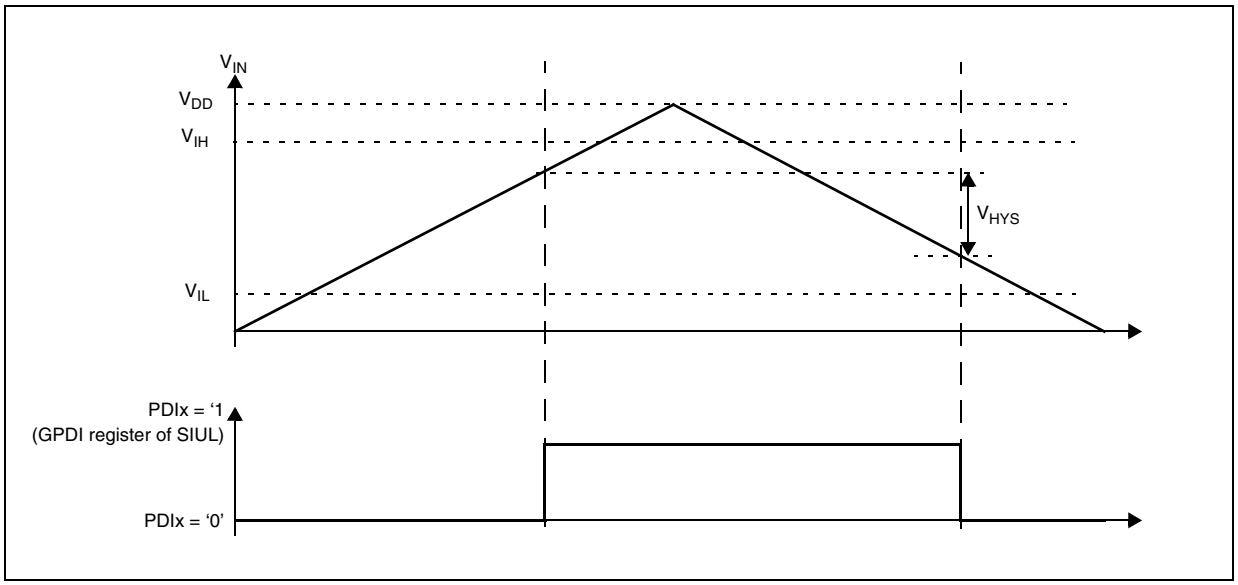


Figure 5. I/O input DC electrical characteristics definition

Table 12. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	
I_{LKG}	CC	P	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	—	nA
		P			T_A = 25 °C	—	2	—	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W_{NFI}[2]	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

3.6.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 13 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 14 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 15 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 16 provides output driver characteristics for I/O pads when in FAST configuration.

Table 13. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\lvert I_{WPD} \rvert$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

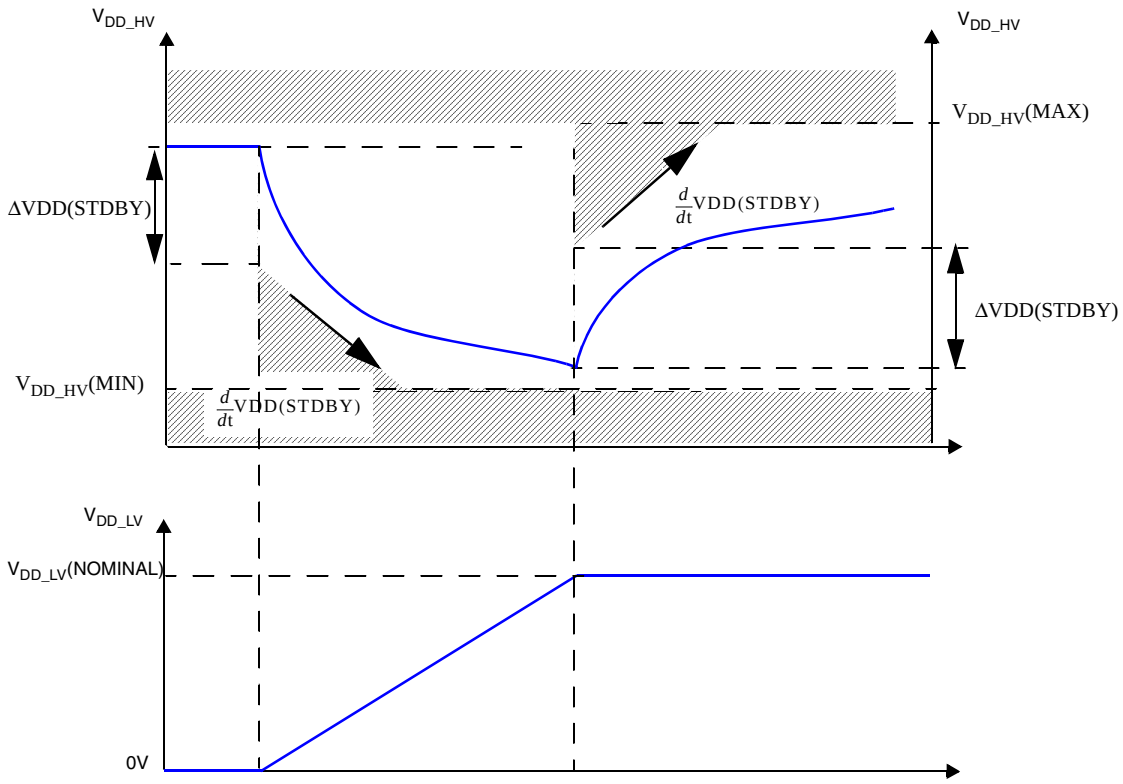


Figure 10. V_{DD} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 22. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	P	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
				After trimming	1.15	1.28	1.32	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors VDD_BV to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

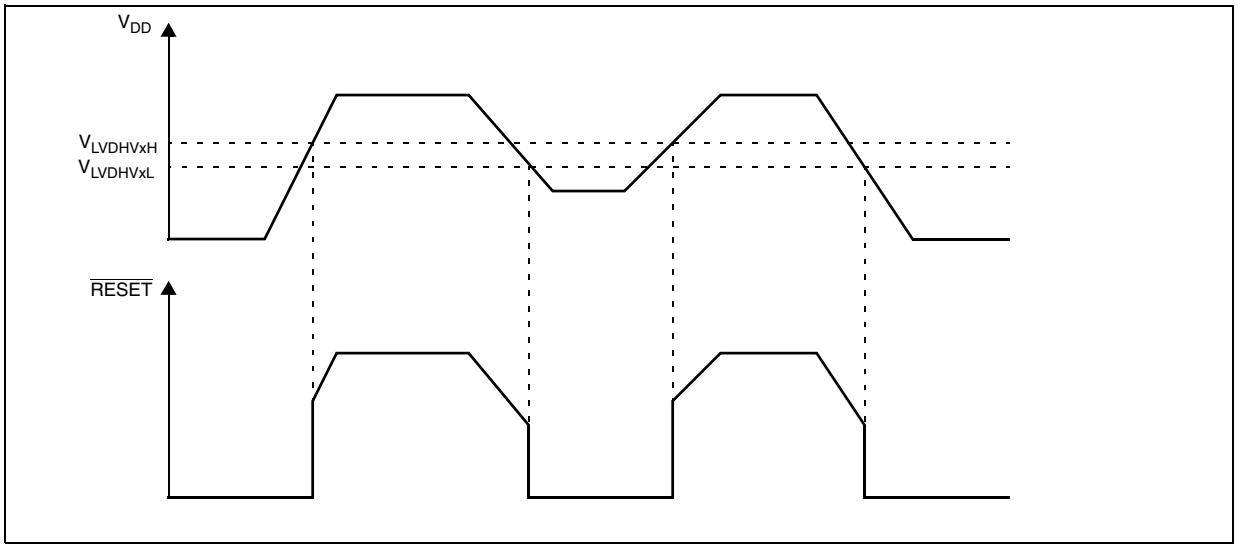


Figure 11. Low voltage monitor vs. reset

Table 23. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	D	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV3BH}$	CC	T	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3BL low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.14	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

Table 31. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 32. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 12 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 33 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

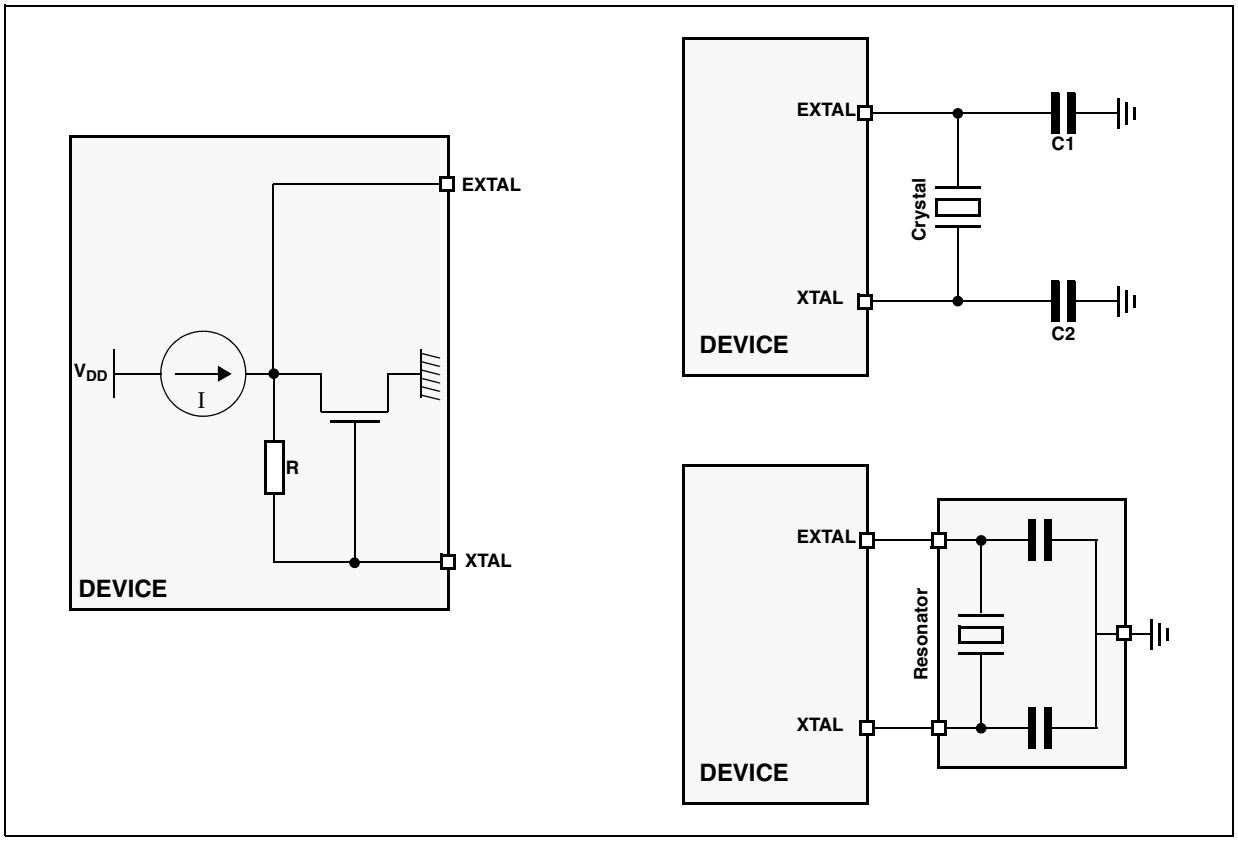


Figure 12. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 33. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

[1] The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

[2] The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

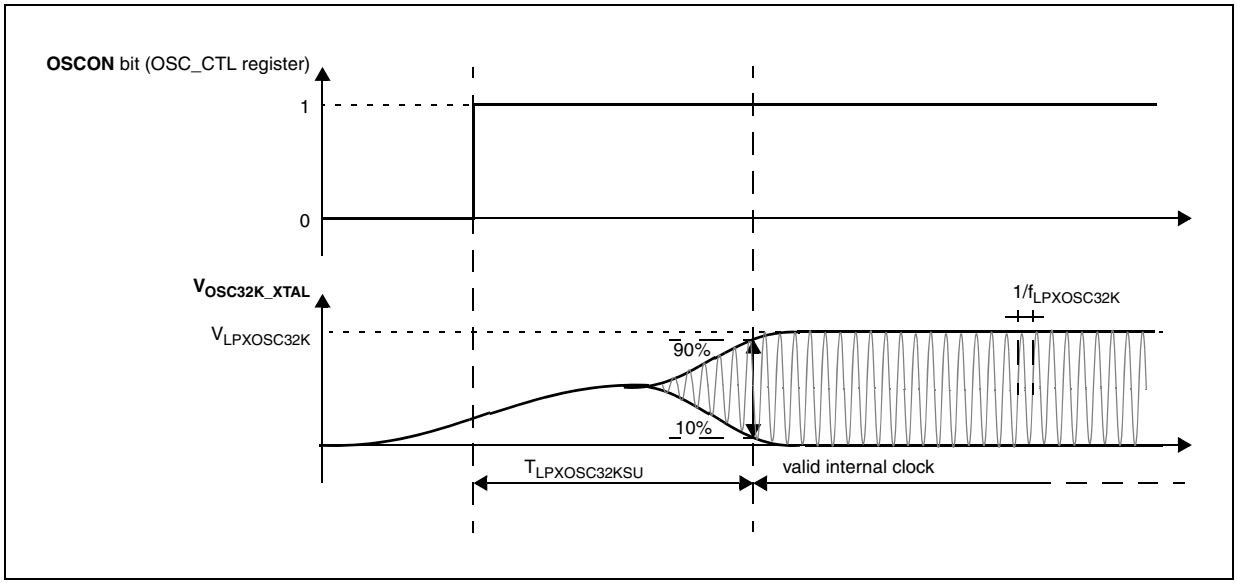


Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics

Table 36. Slow external crystal oscillator (32 kHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{SXOSC}	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V_{SXOSC}	CC	T	Oscillation amplitude	—	—	2.1	—	V
$I_{SXOSCBIAS}$	CC	T	Oscillation bias current	—		2.5		µA
I_{SXOSC}	CC	T	Slow external crystal oscillator consumption	—	—	—	8	µA
$T_{SXOSCSU}$	CC	T	Slow external crystal oscillator start-up time	—	—	—	2[2]	s

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

3.14 FMPLL electrical characteristics

The device provides a frequency modulated phase locked loop (FMPLL) module to generate a fast system clock from the FXOSC or FIRC sources.

Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	64	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[2]	—	40	—	60	%

3.17.3 ADC electrical characteristics

Table 40. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		D		T_A = 85°C			3	100	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 41. ADC_0 conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
$I_{ADC0pwd}$	SR	—	ADC_0 consumption in power down mode	—	—	—	50	µA
$I_{ADC0run}$	SR	—	ADC_0 consumption in running mode	—	—	—	5	mA
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC0_SYS}	SR	—	ADC_0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sample time[5]	f_{ADC} = 32 MHz, ADC0_conf_sample_input = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t_{ADC0_C}	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, ADC_conf_comp = 2	0.625	—	—	µs
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF
C_{P1}	CC	D	ADC_0 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_0 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_0 input pin capacitance 3	—	—	—	1	pF

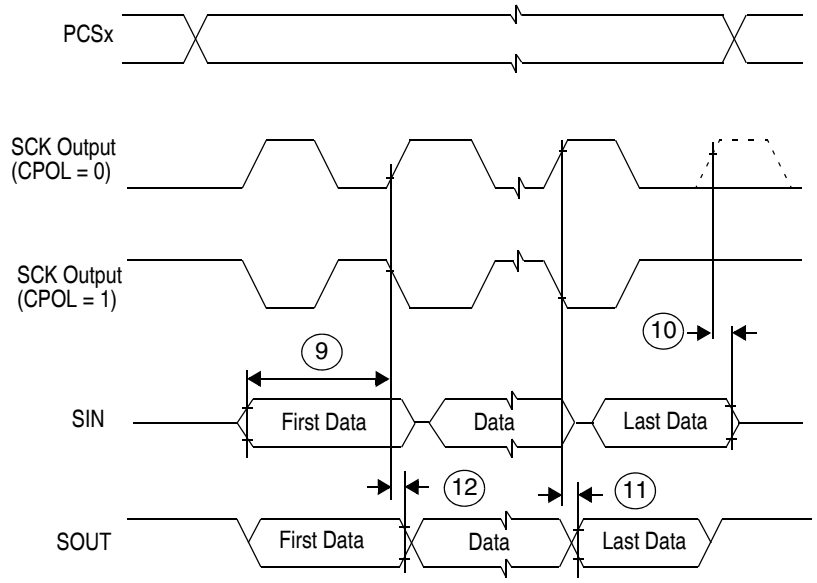
Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC1} – 0.1	—	V_{DD_ADC1} + 0.1	V
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sample time[4] VDD = 3.3 V	f_{ADC1} = 20 MHz, ADC1_conf_sample_input = 12	600	—	—	ns
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 32 MHz, ADC1_conf_sample_input = 17	500	—	—	
			Sample time[4] VDD = 3.3 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	µs
			Sample time[4] VDD = 5.0 V	f_{ADC1}= 3.33 MHz, ADC1_conf_sample_input = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] VDD = 3.3 V	f_{ADC1} = 20MHz, ADC1_conf_comp = 0	2.4	—	—	µs
			Conversion time[5] VDD = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, ADC1_conf_comp = 0	1.5	—	—	µs
			Conversion time[5] VDD = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
			Conversion time[5] VDD = 5.0 V	f_{ADC1} = 13.33 MHz, ADC1_conf_comp = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Table 43. On-chip peripherals current consumption[1] (continued)

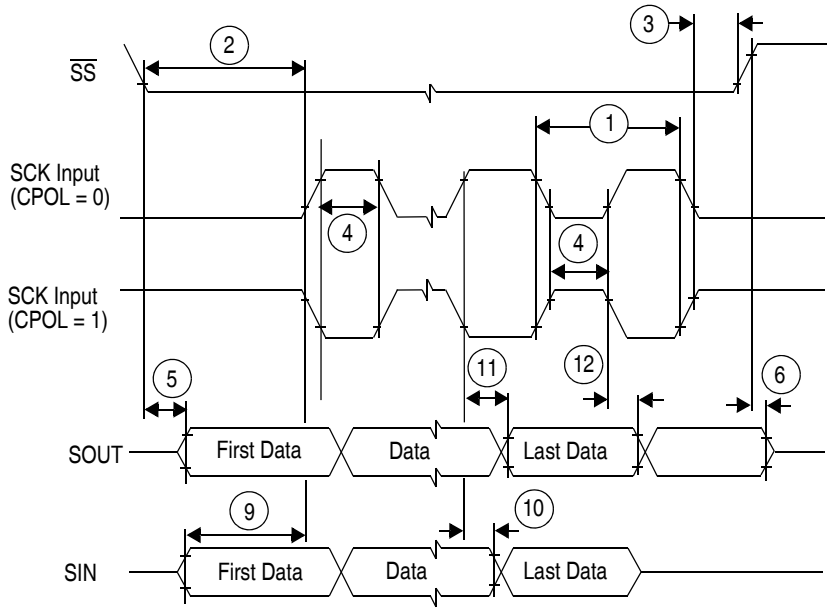
Symbol		C	Parameter	Conditions		Value	Unit
						Typ	
$I_{DD\_HV\_ADC1}$	CC	T	ADC_1 supply current on $V_{DD\_HV\_ADC1}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	300 * f_{periph}	µA
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	4	mA
$I_{DD\_HV(FLASH)}$	CC	T	CFlash + DFlash supply current on V_{DD_HV}	V_{DD} = 5.5 V	—	12	mA
$I_{DD\_BV(PLL)}$	CC	T	PLL supply current on V_{DD_BV}	V_{DD} = 5.5 V	—	2.5	mA

1 Operating conditions: T_A = 25 °C, f_{periph} = 8 MHz to 64 MHz



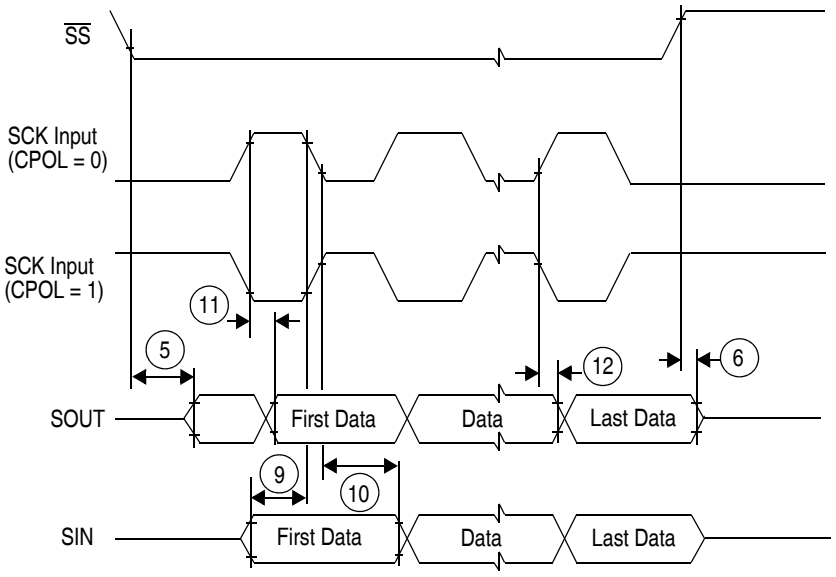
Note: Numbers shown reference Table 44.

Figure 28. DSPI modified transfer format timing — master, CPHA = 1



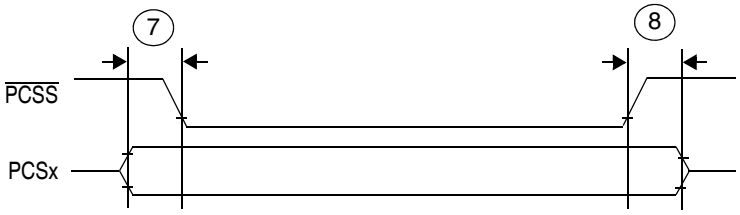
Note: Numbers shown reference Table 44.

Figure 29. DSPI modified transfer format timing — slave, CPHA = 0



Note: Numbers shown reference Table 44.

Figure 30. DSPI modified transfer format timing — slave, CPHA = 1



Note: Numbers shown reference Table 44.

Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.18.3 JTAG characteristics

Table 45. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns

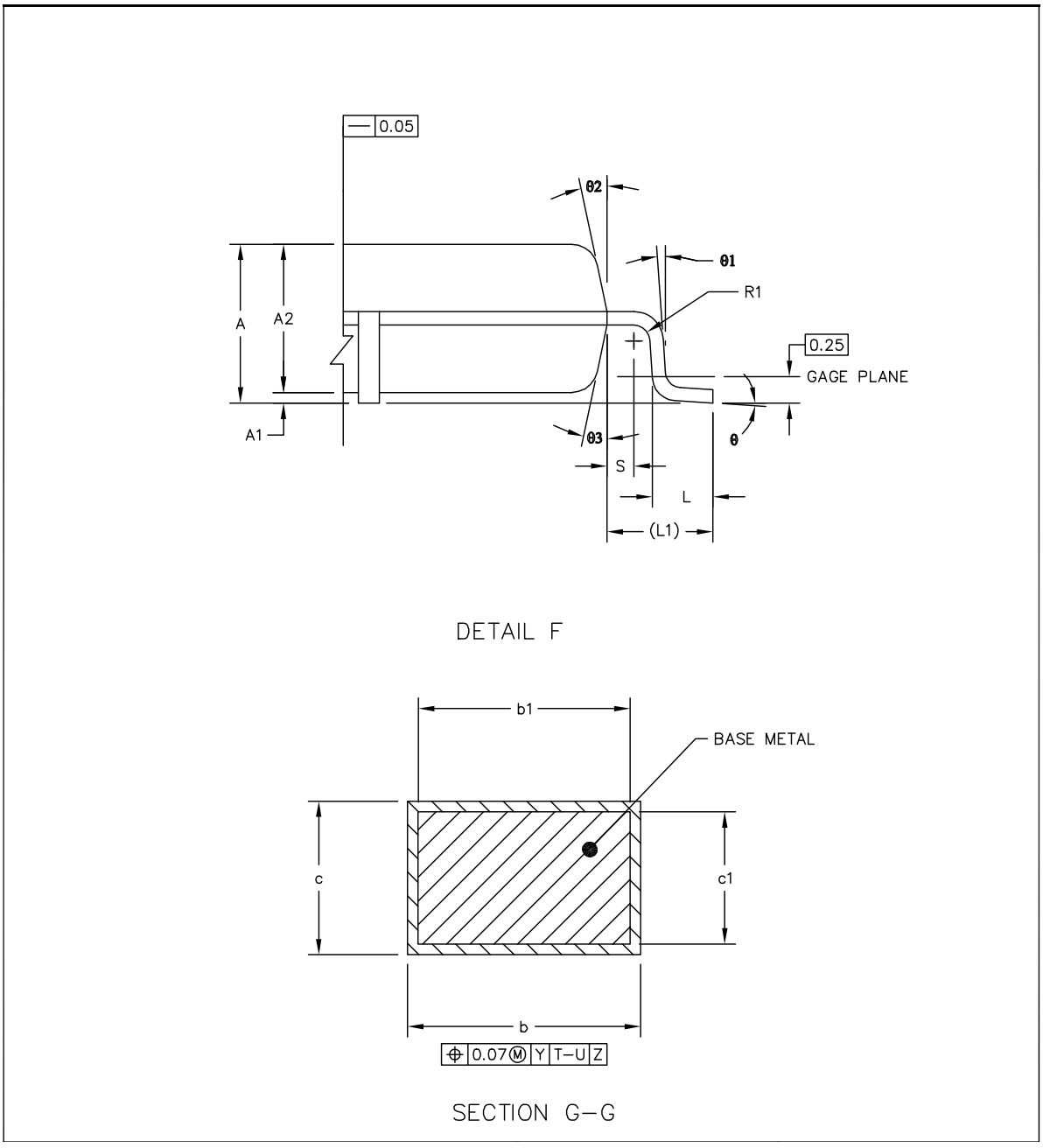


Figure 34. 176 LQFP package mechanical drawing (Part 2 of 3)

4.1.3 100 LQFP

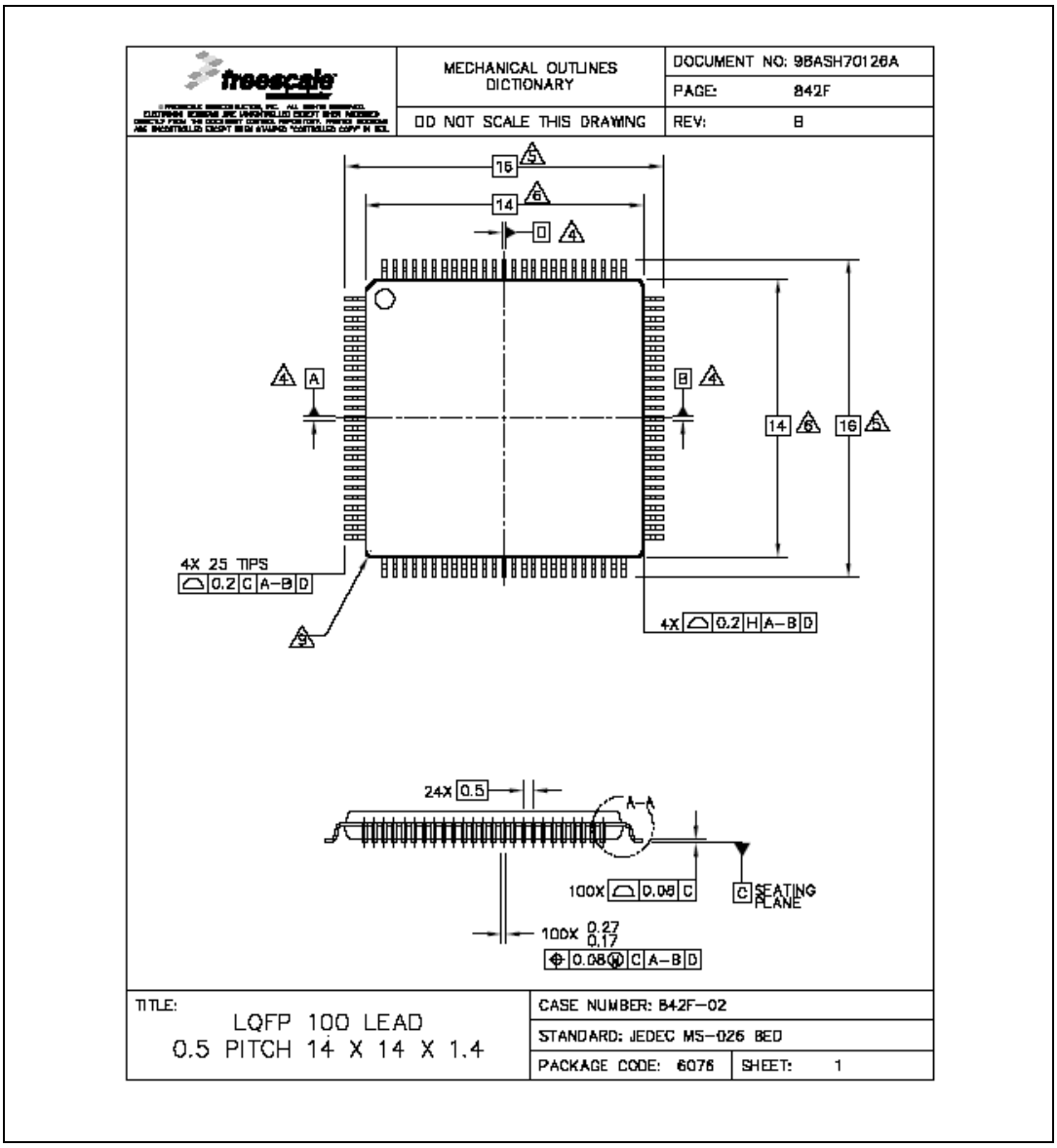


Figure 38. 100 LQFP package mechanical drawing (Part 1 of 3)

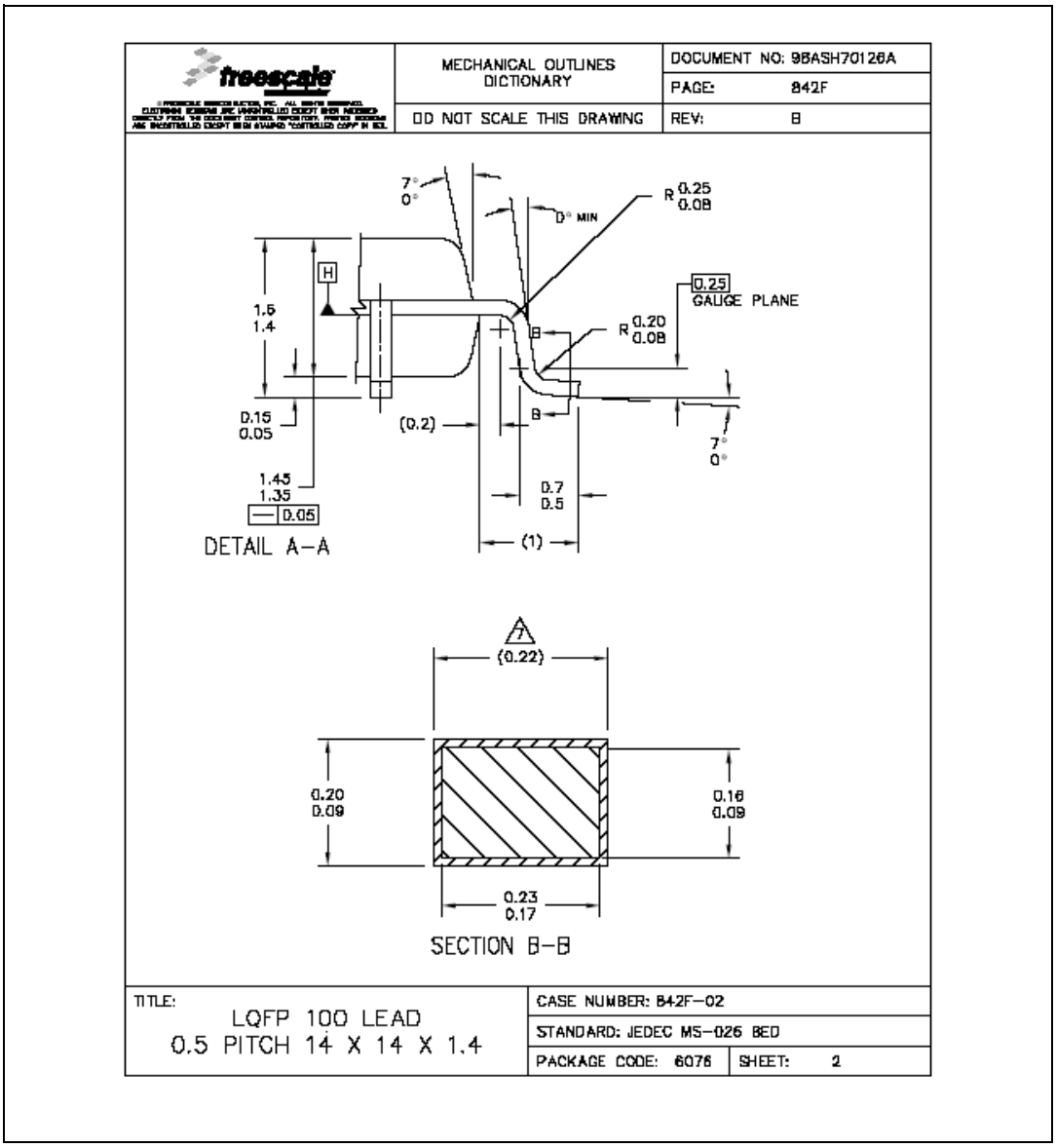


Figure 39. 100 LQFP package mechanical drawing (Part 2 of 3)

Table 46. Revision history (continued)

Revision	Date	Description of changes
2 (cont.)	15 May 2013	In Table 24 (Electrical characteristics in different application modes), — Changed I_{DDMAX} Typ to 81 mA and I_{DDMAX} Typ to 130 mA. — Changed I_{DDRUN} Typ for fCPU = 32 MHz to 40 mA. — Changed I_{DDRUN} Typ for fCPU = 48 MHz to 54 mA. Added I_{DDRUN} Max of 96 mA. — Changed I_{DDRUN} Typ for fCPU = 64 MHz to 67 mA. Added I_{DDRUN} Max of 120 mA. — Changed I_{DDHALT} at T_A = 25 °C Typ to 10 mA and I_{DDHALT} Max to 15 mA. — Changed I_{DDHALT} at T_A = 125 °C Typ to 15 mA and I_{DDHALT} Max to 28 mA. — Changed I_{DDSTOP} T_A temperature from –40 °C to 25 °C. — Changed I_{DDSTOP} at T_A = 25 °C Typ to 130 µA and I_{DDSTOP} Max to 500 µA. — Changed I_{DDSTOP} at T_A = 55 °C Typ to 180 µA. — Changed I_{DDSTOP} at T_A = 85 °C Typ to 1 mA and I_{DDSTOP} Max to 5 mA. — Changed I_{DDSTOP} at T_A = 105 °C Typ to 3 mA and I_{DDSTOP} Max to 9 mA. — Changed I_{DDSTOP} at T_A = 125 °C Typ to 5 mA and I_{DDSTOP} Max to 14 mA. — Changed $I_{DDSTDBY2}$ at T_A = 25 °C Typ to 17 µA and Max to 80 µA. — Changed $I_{DDSTDBY2}$ at T_A = 55 °C Typ to 30 µA. — Changed $I_{DDSTDBY2}$ at T_A = 85 °C Typ to 100 µA. — Changed $I_{DDSTDBY2}$ at T_A = 105 °C Typ to 280 µA and Max to 950 µA. — Changed $I_{DDSTDBY2}$ at T_A = 125 °C Typ to 460 µA and Max to 1700 µA. — Changed the parameter classification for $I_{DDSTANDBY2}$ (T_A = 125 °C) — Changed $I_{DDSTDBY1}$ at T_A = 25 °C Typ to 12 µA and Max to 50 µA. — Changed $I_{DDSTDBY1}$ at T_A = 55 °C Typ to 24 µA. — Changed $I_{DDSTDBY1}$ at T_A = 85 °C Typ to 48 µA. — Changed $I_{DDSTDBY1}$ at T_A = 105 °C Typ to 150 µA and Max to 500 µA. — Changed $I_{DDSTDBY1}$ at T_A = 125 °C Typ to 260 µA. — Changed the third sentence of Footnote 3 to begin with “The given value is thought to be a **worst case value** (64 MHz at 125 °C) with all peripherals running.” — Removed footnotes 8 and 9 regarding I_{DDHALT} and I_{DDSTOP}. — Corrected “C” characteristics to reflect testing status. In Section 3.10, Flash memory electrical characteristics, removed the "FLASH_BIU settings vs. frequency of operation" table. In Table 28 (Flash power supply DC electrical characteristics), corrected Footnote 2 to specify 125 °C. In Section 3.14, FMPLL electrical characteristics, changed the text “the main oscillator driver” to “the FXOSC or FIRC sources.” In Table 40 (ADC input leakage current), added specifications for 85 °C. In Table 44 (DSPI characteristics), added t_{SCK} specifications for MTFE=1. In Table 44 (DSPI characteristics), updated specifications 7 and 8 to 13 ns, all DSPIs. in ADC section, corrected Equation 11. In Figure 41 (Commercial product code structure), added “**Note:** Not all options are available on all devices.” Removed Section 6, Abbreviations.
3	11 Sep 2013	Updated the temperature in table note 2 in Table 1 (MPC5606BK family comparison) from 105 ^{o}C to 125 ^{o}C.
4	25 Nov2015	Updated the Max value current for $I_{ADC0run}$ from 40 mA to 5 mA in Table 41 (ADC_0 conversion characteristics (10-bit ADC_0)).
5	7 Nov 2017	In Table 9 (Recommended operating conditions (3.3 V)) added Min value for TV_{DD}. In Table 10 (Recommended operating conditions (5.0 V)) added Min value for TV_{DD}. In Table 44 (DSPI characteristics) changed the for DSPI 2 and 4, in MTFE=1 mode from 125 to 145.