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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	149
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 29x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0vlu6

1.3 Device comparison

Table 1 summarizes the functions of the blocks present on the MPC5606BK.

Table 1. MPC5606BK family comparison[1]

Feature	MPC5605BK			MPC5606BK		
Package	100 LQFP	144 LQFP	176 LQFP	100 LQFP	144 LQFP	176 LQFP
CPU	e200z0h					
Execution speed[2]	Up to 64 MHz					
Code flash memory	768 KB			1 MB		
Data flash memory	64 (4 x 16) KB					
SRAM	64 KB			80 KB		
MPU	8-entry					
eDMA	16 ch					
10-bit ADC	Yes					
dedicated[3]	7 ch	15 ch	29 ch	7 ch	15 ch	29 ch
shared with 12-bit ADC	19 ch					
12-bit ADC	Yes					
dedicated[4]	5 ch					
shared with 10-bit ADC	19 ch					
Total timer I/O[5] eMIOS	37 ch, 16-bit	64 ch, 16-bit		37 ch, 16-bit	64 ch, 16-bit	
Counter / OPWM / ICOC[6]	10 ch					
O(I)PWM / OPWFMB / OPWMCB / ICOC[7]	7 ch					
O(I)PWM / ICOC[8]	7 ch	14 ch				
OPWM / ICOC[9]	13 ch	33 ch				
SCI (LINFlex)	4	6	8	4	6	8
SPI (DSPI)	3	5	6	3	5	6
CAN (FlexCAN)	6					
I^2C	1					
32 KHz oscillator	Yes					
GPIO[10]	77	121	149	77	121	149
Debug	JTAG					

1 Feature set dependent on selected peripheral multiplexing; table shows example.

2 Based on 125 °C ambient operating temperature.

3 Not shared with 12-bit ADC, but possibly shared with other alternate functions.

4 Not shared with 10-bit ADC, but possibly shared with other alternate functions.

5 Refer to eMIOS section of device reference manual for information on the channel configuration and functions.

6 Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.

7 Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.

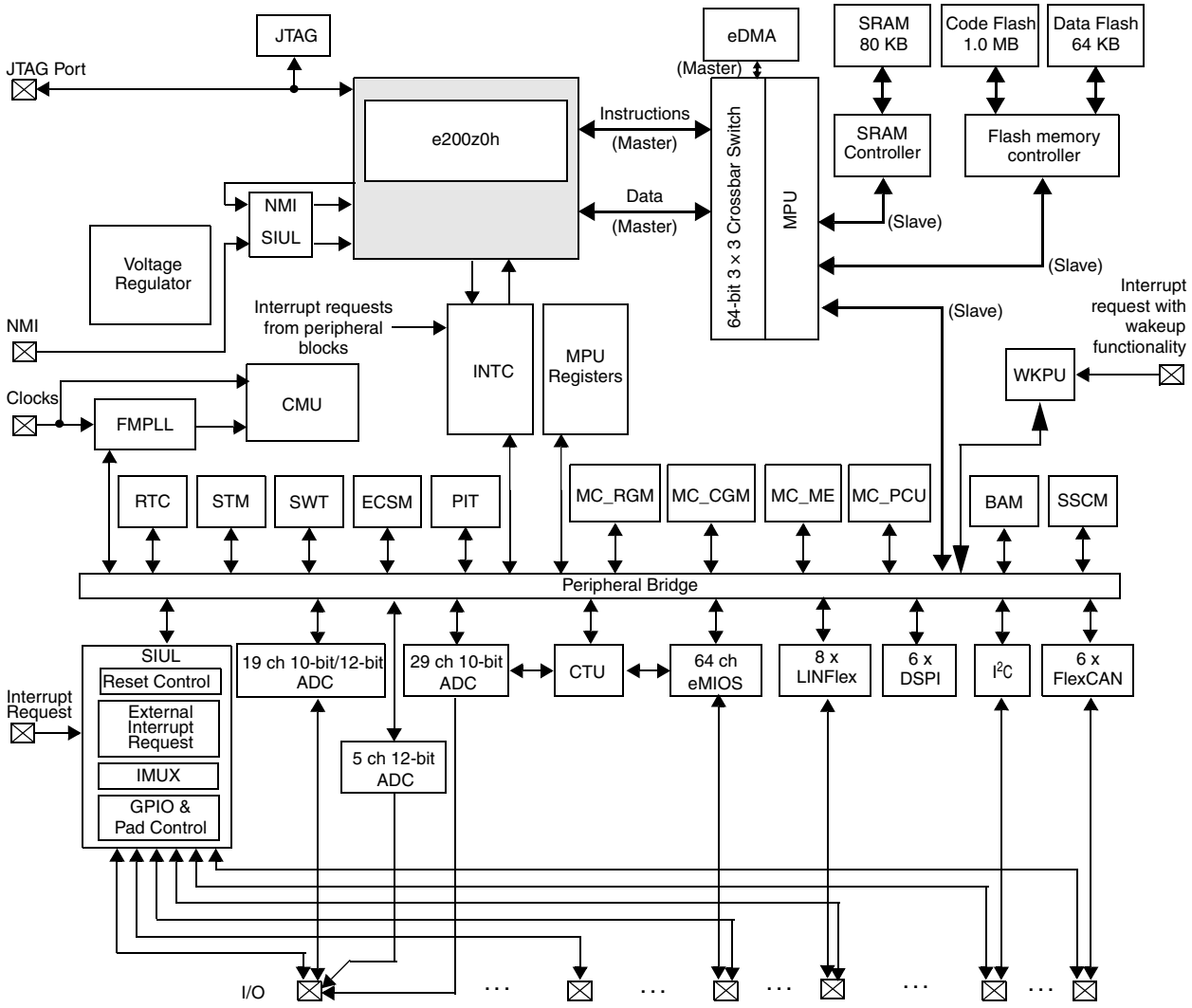
8 Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.

9 Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.

10 Maximum I/O count based on multiplexing with peripherals.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5606BK.



Legend:

ADC	Analog-to-Digital Converter
BAM	Boot Assist Module
FlexCAN	Controller Area Network
CFlash	Code flash memory
CMU	Clock Monitor Unit
CTU	Cross Triggering Unit
DFlash	Data flash memory
DSPI	Deserial Serial Peripheral Interface
eDMA	Enhanced Direct Memory Access
eMIOS	Enhanced Modular Input Output System
FMPLL	Frequency-Modulated Phase-Locked Loop
I^2C	Inter-integrated Circuit Bus
IMUX	Internal Multiplexer
INTC	Interrupt Controller
JTAG	JTAG controller
LINFlex	Serial Communication Interface (LIN support)
MC_CGM	Clock Generation Module
MC_ME	Mode Entry Module
MPU	Memory Protection Unit
NMI	Non-Maskable Interrupt
MC_PCU	Power Control Unit
MC_RGM	Reset Generation Module
PIT	Periodic Interrupt Timer
RTC	Real-Time Clock
SIUL	System Integration Unit Lite
SRAM	Static Random-Access Memory
SSCM	System Status Configuration Module
STM	System Timer Module
SWT	Software Watchdog Timer
WKPU	Wakeup Unit

Figure 1. MPC5606BK block diagram

2.2 Pin muxing

Table 2 defines the pin list and muxing for this device.

Each entry of Table 2 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 2. Functional port pins

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
Port A										
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][4]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKUP	I/O I/O O I/O I	M	Tristate	12	16	24
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[5] — WKUP[2][4]	SIUL eMIOS_0 WKUP — WKUP	I/O I/O I — I	S	Tristate	7	11	19
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKUP[3][4]	SIUL eMIOS_0 — ADC_0 WKUP	I/O I/O — O I	S	Tristate	5	9	17
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKUP[9][4]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKUP	I/O I/O — I/O I I	S	Tristate	29	43	51
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	118	146
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 LINFlex_3 — SIUL ADC_1	I/O I/O O — I I	J	Tristate	71	104	128
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[6] —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	105	129
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[6]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I^2C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I^2C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	108	132
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — E0UC[28] CS3_1 EIRQ[17] SIN_0	SIUL — eMIOS_0 DSPI_1 SIUL DSPI_0	I/O — I/O O I I	S	Tristate	31	45	53
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 E0UC[29] —	SIUL DSPI_0 eMIOS_0 —	I/O O I/O —	M	Tristate	30	44	52
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	28	42	50

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX DEBUG[3] EIRQ[7]	SIUL DSPI_1 FlexCAN_3 SSCM SIUL	I/O O O O I	M	Tristate	91	130	158
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] DEBUG[4]	SIUL LINFlex_1 eMIOS_1 SSCM	I/O O I/O O	S	Tristate	25	36	44
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] DEBUG[5] LIN1RX WKUP[12][4]	SIUL — eMIOS_1 SSCM LINFlex_1 WKUP	I/O — I/O O I I	S	Tristate	26	37	45
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] DEBUG[6]	SIUL LINFlex_2 eMIOS_0 SSCM	I/O O I/O O	S	Tristate	99	143	175
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] DEBUG[7] WKUP[13][4] LIN2RX	SIUL — eMIOS_0 SSCM WKUP LINFlex_2	I/O — I/O O I I	S	Tristate	2	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M	Tristate	22	28	36
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] WKUP[5][4] CAN1RX CAN4RX	SIUL — — ADC_0 WKUP FlexCAN_1 FlexCAN_4	I/O — — O I I I	S	Tristate	21	27	35
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] — WKUP[20][4] LIN6RX	SIUL eMIOS_1 eMIOS_1 — WKUP LINFlex_6	I/O I/O I/O — I I	S	Tristate	—	29	37
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15]	SIUL eMIOS_1 LINFlex_7 DSPI_2 SIUL	I/O I/O O I/O I	S	Tristate	—	26	34
PG[9]	PCR[105]	AF0 AF1 AF2 AF3 — —	GPIO[105] E1UC[18] — SCK_2 WKUP[21][4] LIN7RX	SIUL eMIOS_1 — DSPI_2 WKUP LINFlex_7	I/O I/O — I/O I I	S	Tristate	—	25	33
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	—	114	138
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	115	139
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] SOUT_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	92	116
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] SCK_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	91	115
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	110	134
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] — — —	SIUL eMIOS_1 — — —	I/O I/O — — —	M	Tristate	—	111	135
Port H										

Table 14. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[2] The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 15. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply V_{DD_LV} from the high voltage ballast supply V_{DD_BV}. The regulator itself is supplied by the common I/O supply V_{DD}. The following supplies are involved:

- HV: High voltage external power supply for voltage regulator module. This must be provided externally through V_{DD} power pin.
- BV: High voltage external power supply for internal ballast module. This must be provided externally through V_{DD_BV} power pin. Voltage values should be aligned with V_{DD}.
- LV: Low voltage internal power supply for core, FMPLL and Flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR: Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA: Low voltage supply for code Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA: Low voltage supply for data Flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

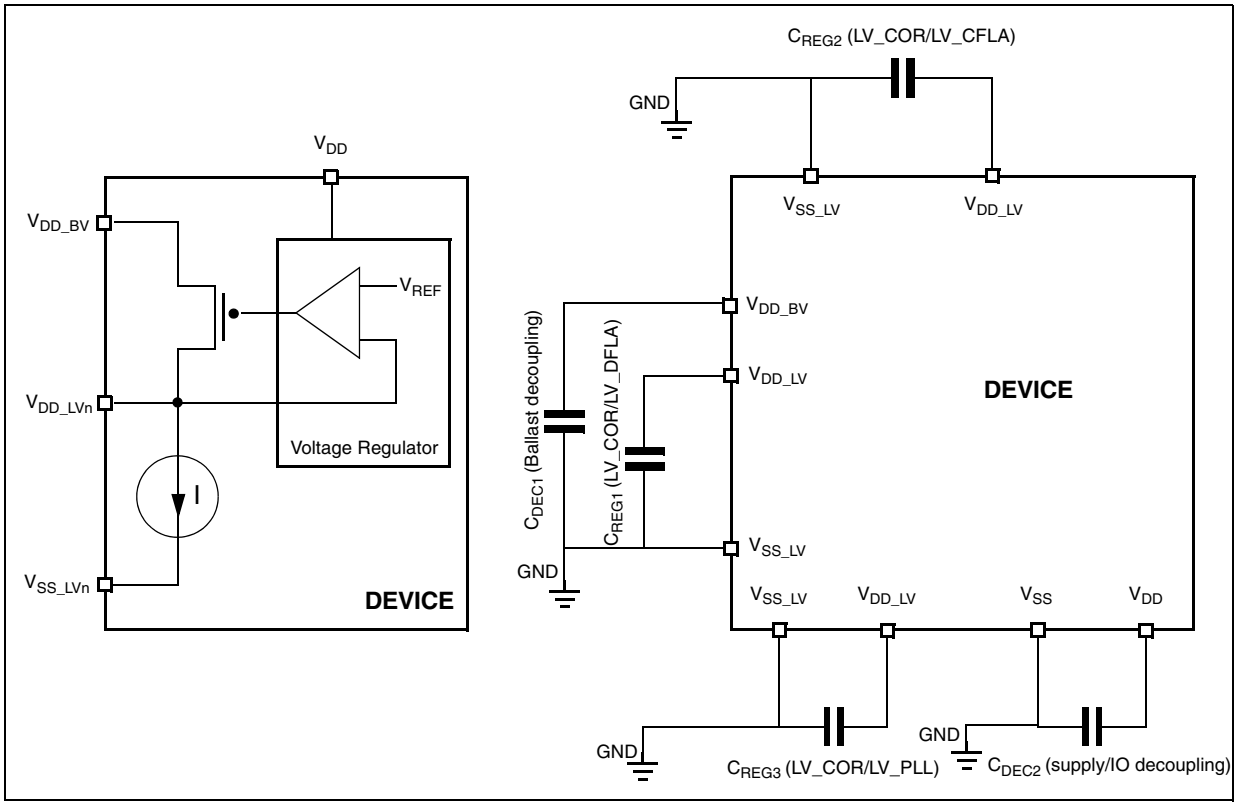


Figure 8. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors VDD_BV to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

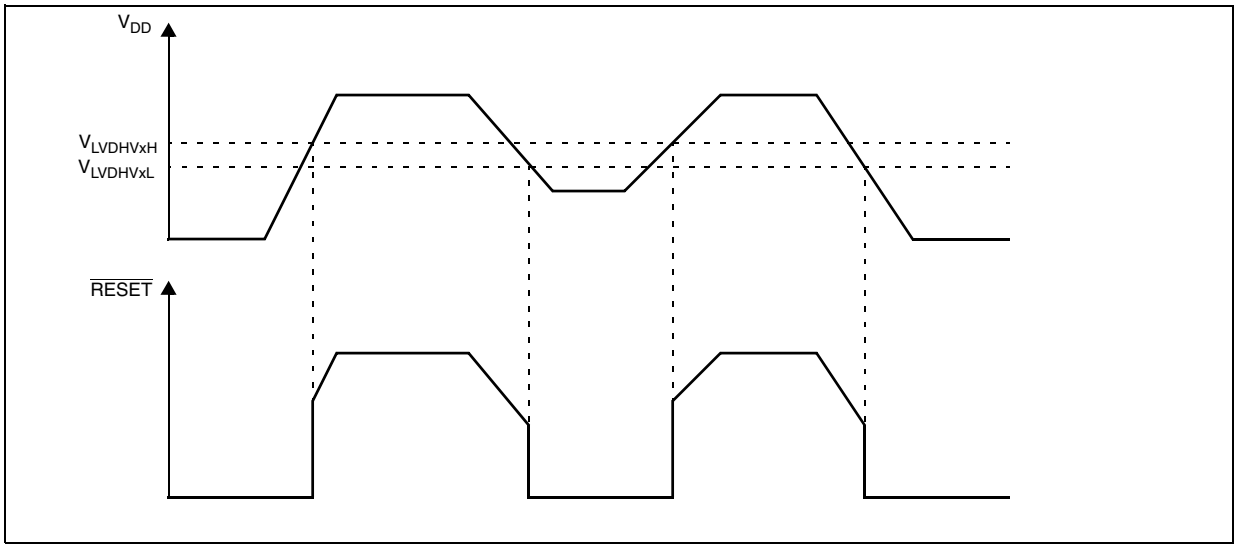


Figure 11. Low voltage monitor vs. reset

Table 23. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	D	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV3BH}$	CC	T	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3BL low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.14	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 26. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	—	years

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 27. Flash read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{READ}	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

3.10.2 Flash power supply DC characteristics

Table 28 shows the power supply DC characteristics on external supply.

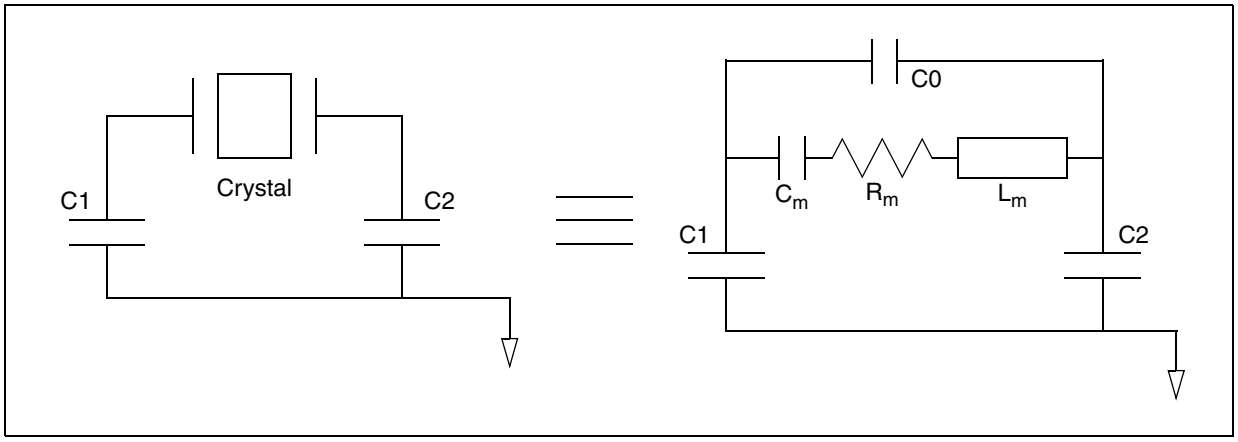


Figure 15. Equivalent circuit of a quartz crystal

Table 35. Crystal motional characteristics[1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
L_m	Motional inductance	—	—	11.796	—	KH
C_m	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2]	—	18	—	28	pF
R_m[3]	Motional resistance	AC coupled at C0 = 2.85 pF[4]	—	—	65	kΩ
		AC coupled at C0 = 4.9 pF[4]	—	—	50	
		AC coupled at C0 = 7.0 pF[4]	—	—	35	
		AC coupled at C0 = 9.0 pF[4]	—	—	30	

1 The crystal used is Epson Toyocom MC306.

2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR (R_m) of the crystal is 50 kΩ

4 C0 Includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins.

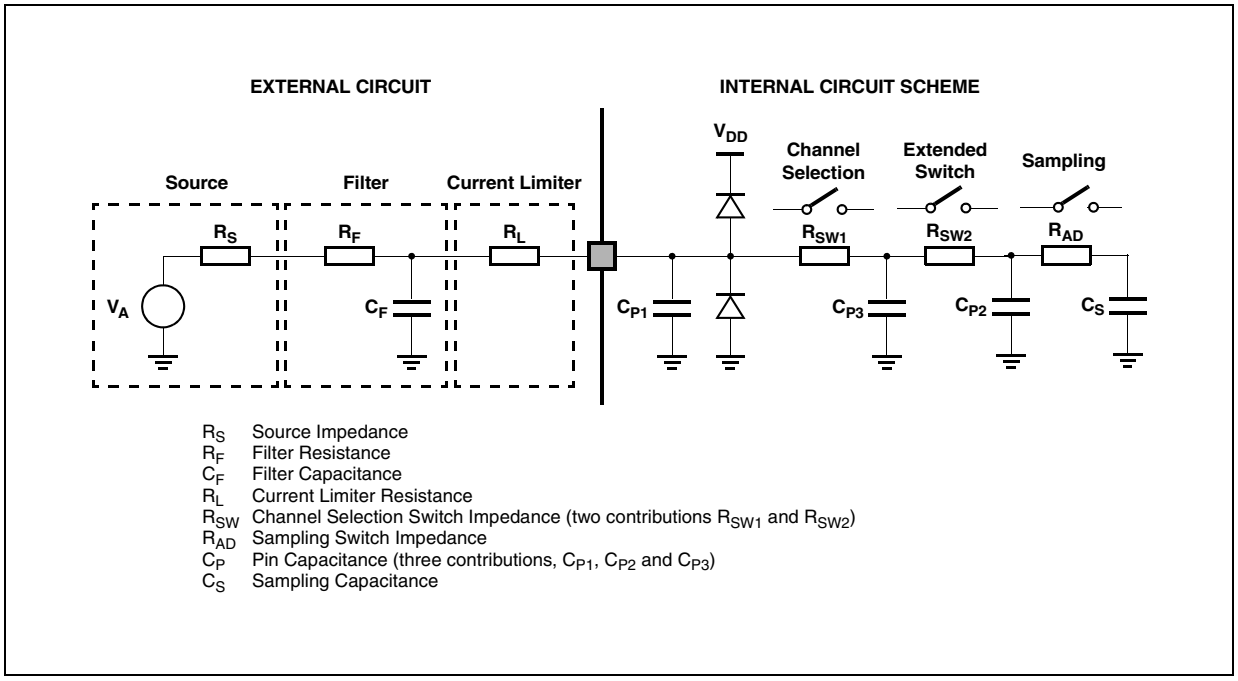


Figure 19. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

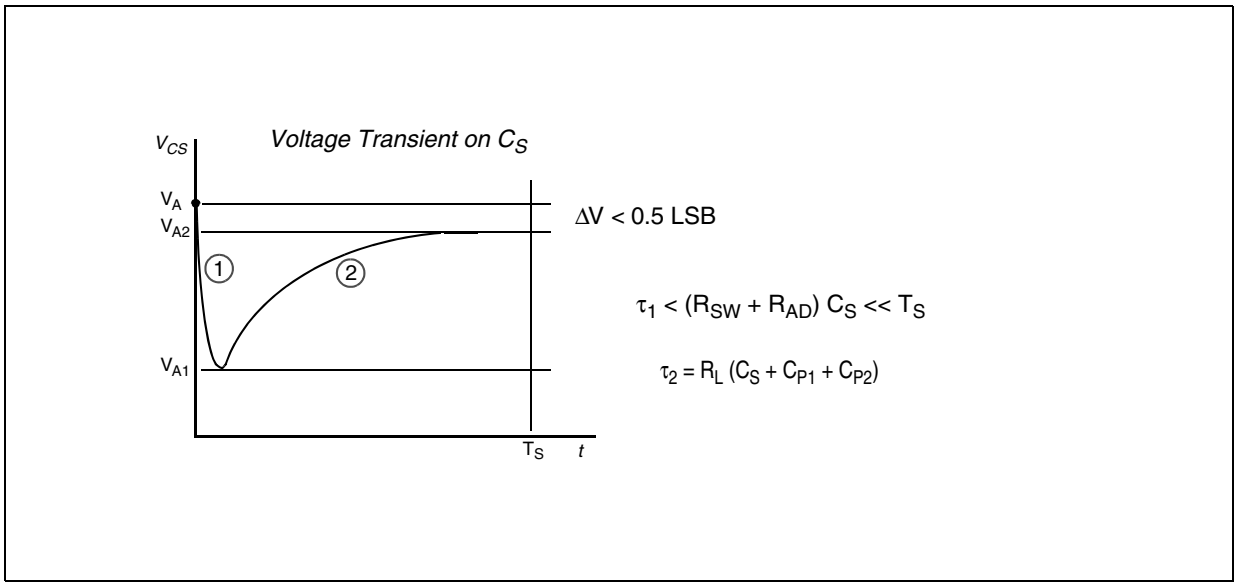


Figure 20. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

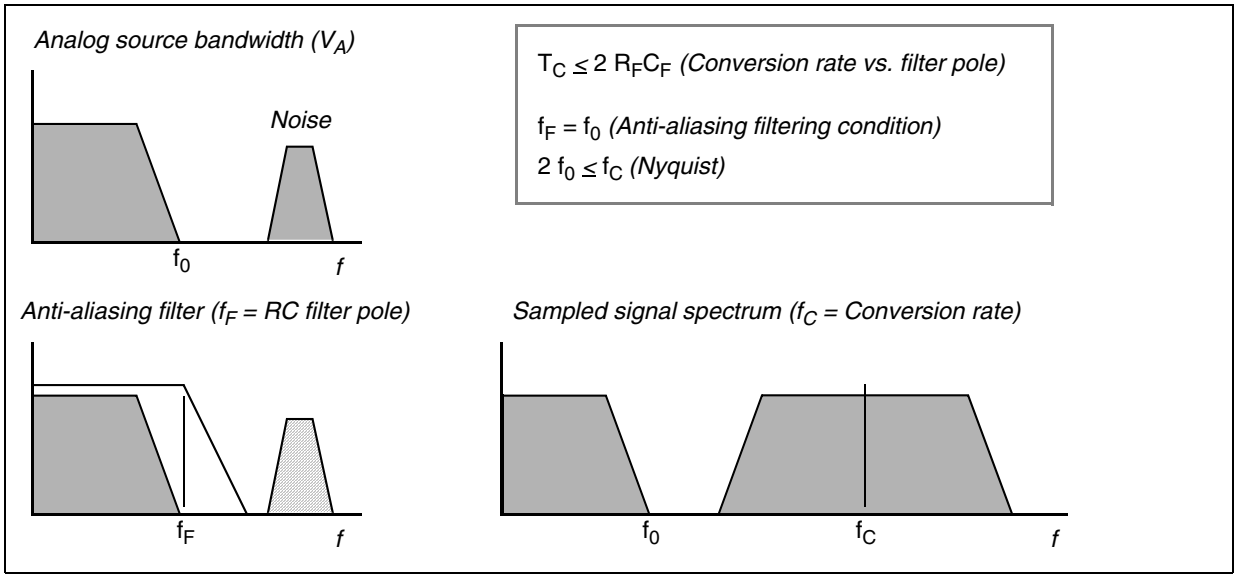


Figure 21. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

ADC_0 (10-bit) ***Eqn. 12***

$$C_F > 2048 \bullet C_S$$

ADC_1 (12-bit) ***Eqn. 13***

$$C_F > 8192 \bullet C_S$$

Table 42. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC_1 input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-Precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-Extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
OFS	CC	T	Absolute Offset error	—		—	2	—	LSB
GNE	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total Unadjusted Error for precise channels, input only pins	Without current injection		–6	—	6	LSB
		T		With current injection		–8	—	8	
TUEX[7]	CC	T	Total Unadjusted Error for extended channel	Without current injection		–10	—	10	LSB
		T		With current injection		–12	—	12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC1} and V_{DD_ADC1} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC1_S}. After the end of the sample time t_{ADC1_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC1_S} depend on programming.

5 This parameter does not include the sample time t_{ADC1_S}, but only the time for determining the digital result and the time to load the result's register with the conversion result.

6 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

1 Operating conditions: C_{out} = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

2 For DSPI4, if SOUT is mapped to a SLOW pad while SCK is mapped to a MEDIUM pad (or vice versa), the minimum cycle time for SCK should be calculated based on the rise and fall times of the SLOW pad. For MTFE=1, SOUT must not be mapped to a SLOW pad while SCK is mapped to a MEDIUM pad.

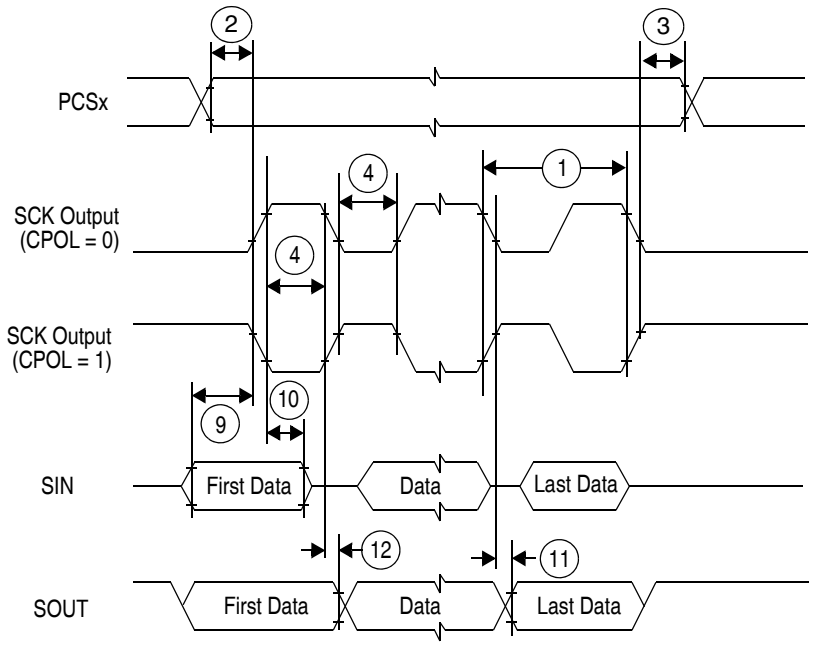
3 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTAR*x* registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

4 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTAR*x* registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

5 For DSPI*x*_CTAR*n*[PCSSCK] = 11.

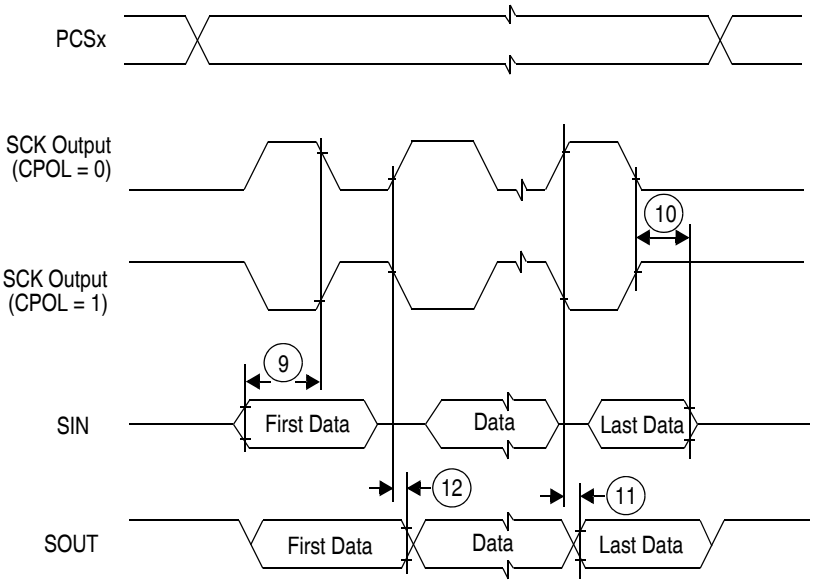
6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.

7 SCK and SOUT are configured as MEDIUM pad.



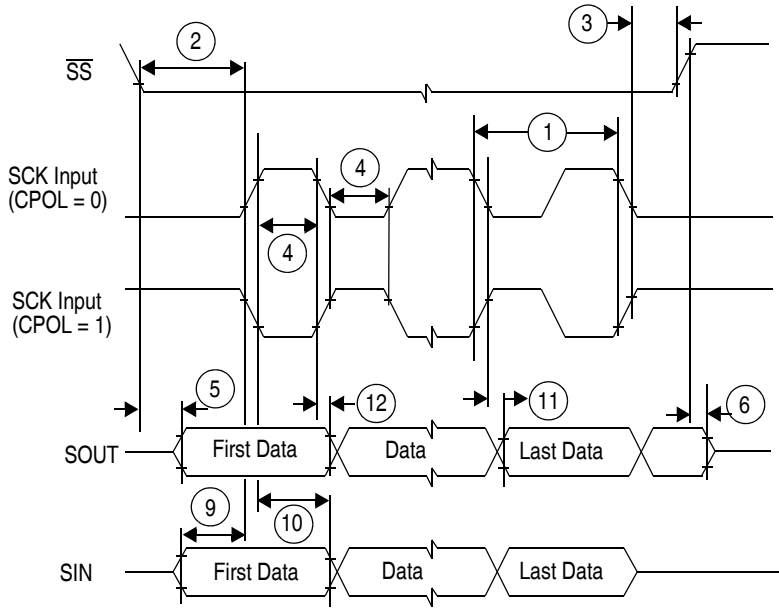
Note: Numbers shown reference Table 44.

Figure 23. DSPI classic SPI timing — master, CPHA = 0



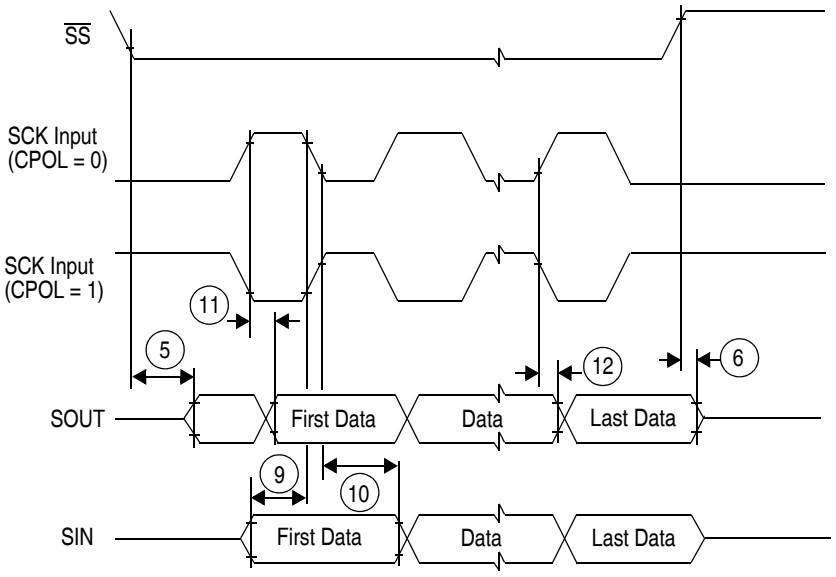
Note: Numbers shown reference Table 44.

Figure 24. DSPI classic SPI timing — master, CPHA = 1



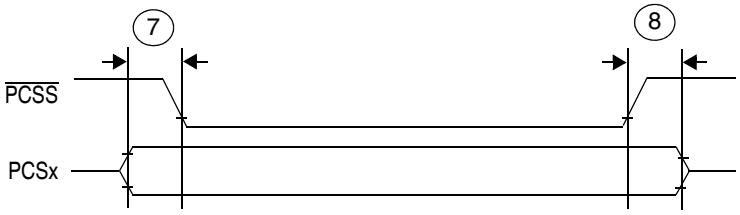
Note: Numbers shown reference Table 44.

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Numbers shown reference Table 44.

Figure 30. DSPI modified transfer format timing — slave, CPHA = 1



Note: Numbers shown reference Table 44.

Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

3.18.3 JTAG characteristics

Table 45. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{JCYC}	CC	D	TCK cycle time	64	—	—	ns
2	t_{TDIS}	CC	D	TDI setup time	15	—	—	ns
3	t_{TDIH}	CC	D	TDI hold time	5	—	—	ns

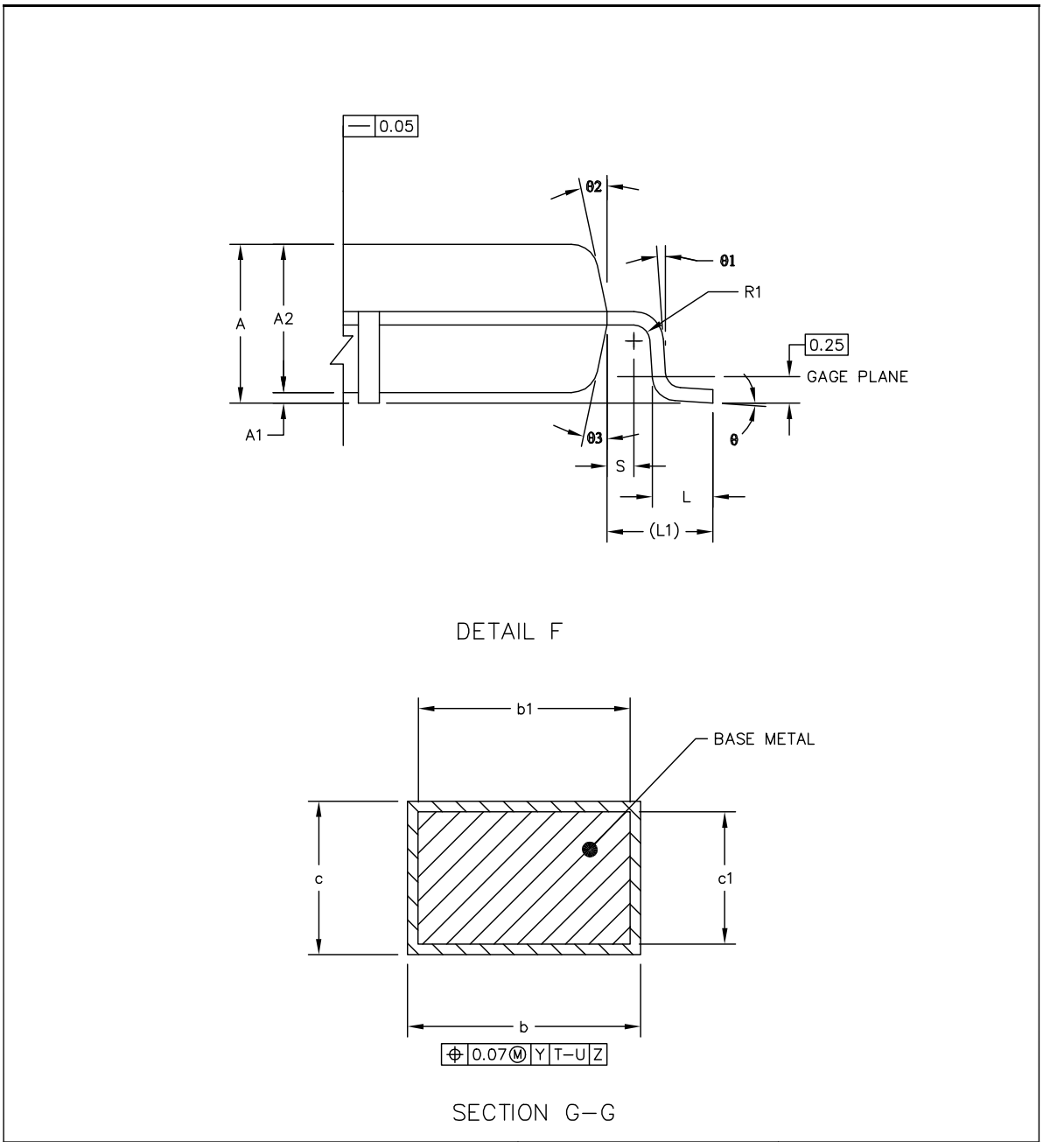


Figure 34. 176 LQFP package mechanical drawing (Part 2 of 3)

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX
A	---		1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D		26 BSC	
D1		24 BSC	
e		0.5 BSC	
E		26 BSC	
E1		24 BSC	
L	0.45	0.6	0.75

DIM	MIN	NOM	MAX
L1		1 REF	
R1	0.08		---
R2	0.08		0.2
S		0.2 REF	
θ	0°	3.5°	7°
θ1	0°		---
θ2	11°	12°	13°
θ3	11°	12°	13°

DIM	MIN	NOM	MAX

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

Figure 35. 176 LQFP package mechanical drawing (Part 3 of 3)

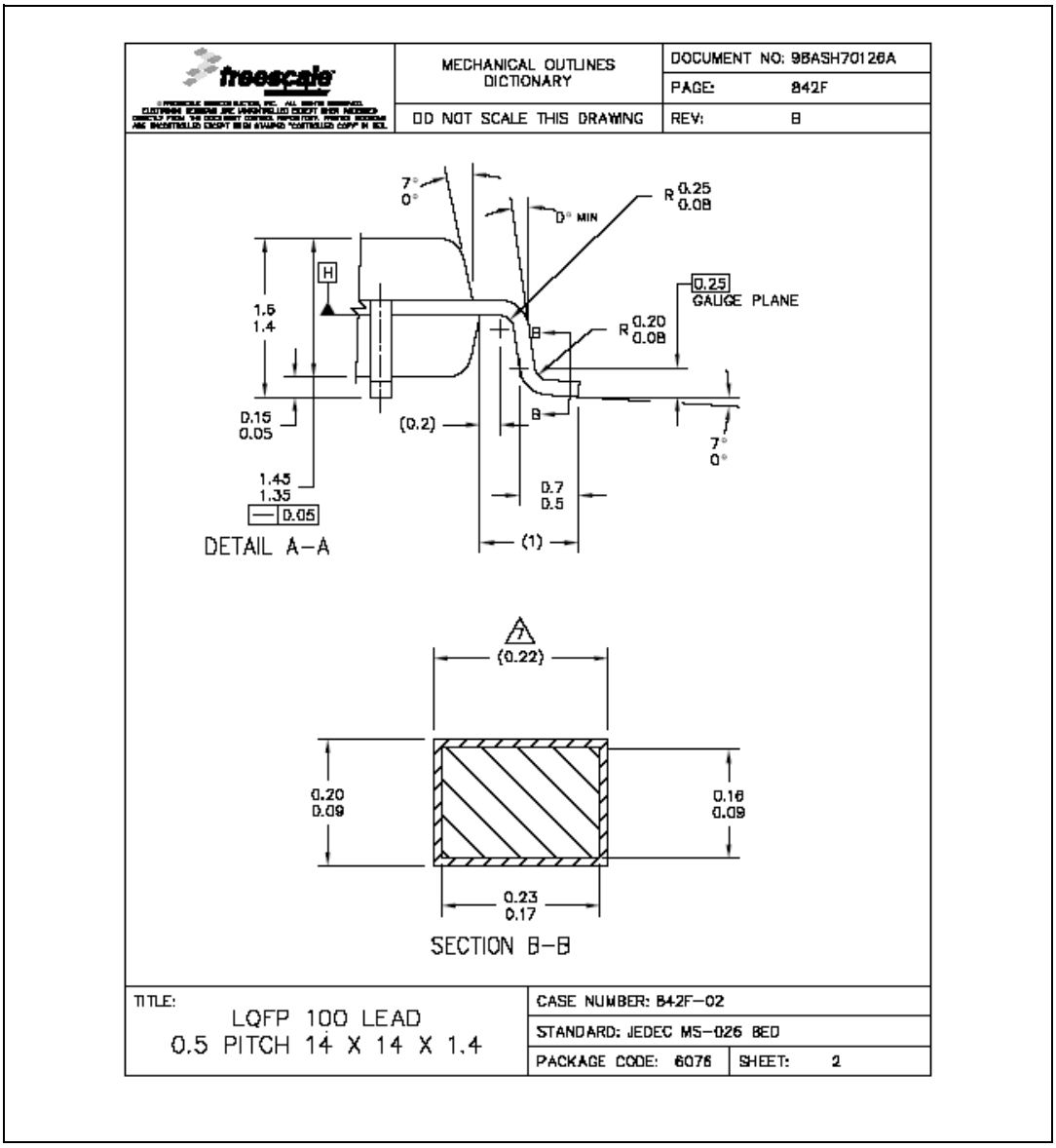


Figure 39. 100 LQFP package mechanical drawing (Part 2 of 3)