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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	149
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 29x10b, 5x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5606bk0vlu6r

2.2 Pin muxing

Table 2 defines the pin list and muxing for this device.

Each entry of Table 2 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

Table 2. Functional port pins

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
Port A										
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKUP[19][4]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKUP	I/O I/O O I/O I	M	Tristate	12	16	24
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[5] — WKUP[2][4]	SIUL eMIOS_0 WKUP — WKUP	I/O I/O I — I	S	Tristate	7	11	19
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKUP[3][4]	SIUL eMIOS_0 — ADC_0 WKUP	I/O I/O — O I	S	Tristate	5	9	17
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 — —	GPIO[4] E0UC[4] — CS0_1 LIN5RX WKUP[9][4]	SIUL eMIOS_0 — DSPI_1 LINFlex_5 WKUP	I/O I/O — I/O I I	S	Tristate	29	43	51
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] LIN4TX —	SIUL eMIOS_0 LINFlex_4 —	I/O I/O O —	M	Tristate	79	118	146
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 — —	GPIO[6] E0UC[6] — CS1_1 EIRQ[1] LIN4RX	SIUL eMIOS_0 — DSPI_1 SIUL LINFlex_4	I/O I/O — O I I	S	Tristate	80	119	147

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX DEBUG[3] EIRQ[7]	SIUL DSPI_1 FlexCAN_3 SSCM SIUL	I/O O O O I	M	Tristate	91	130	158
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX E1UC[28] DEBUG[4]	SIUL LINFlex_1 eMIOS_1 SSCM	I/O O I/O O	S	Tristate	25	36	44
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — E1UC[29] DEBUG[5] LIN1RX WKUP[12][4]	SIUL — eMIOS_1 SSCM LINFlex_1 WKUP	I/O — I/O O I I	S	Tristate	26	37	45
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] DEBUG[6]	SIUL LINFlex_2 eMIOS_0 SSCM	I/O O I/O O	S	Tristate	99	143	175
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] DEBUG[7] WKUP[13][4] LIN2RX	SIUL — eMIOS_0 SSCM WKUP LINFlex_2	I/O — I/O O I I	S	Tristate	2	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC_0	I/O O O O	M	Tristate	22	28	36
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — MA[2] WKUP[5][4] CAN1RX CAN4RX	SIUL — — ADC_0 WKUP FlexCAN_1 FlexCAN_4	I/O — — O I I I	S	Tristate	21	27	35
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PG[7]	PCR[103]	AF0 AF1 AF2 AF3 — —	GPIO[103] E1UC[16] E1UC[30] — WKUP[20][4] LIN6RX	SIUL eMIOS_1 eMIOS_1 — WKUP LINFlex_6	I/O I/O I/O — I I	S	Tristate	—	29	37
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] LIN7TX CS0_2 EIRQ[15]	SIUL eMIOS_1 LINFlex_7 DSPI_2 SIUL	I/O I/O O I/O I	S	Tristate	—	26	34
PG[9]	PCR[105]	AF0 AF1 AF2 AF3 — —	GPIO[105] E1UC[18] — SCK_2 WKUP[21][4] LIN7RX	SIUL eMIOS_1 — DSPI_2 WKUP LINFlex_7	I/O I/O — I/O I I	S	Tristate	—	25	33
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	—	114	138
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	115	139
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] SOUT_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	92	116
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] SCK_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	91	115
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	110	134
PG[15]	PCR[111]	AF0 AF1 AF2 AF3 —	GPIO[111] E1UC[1] — — —	SIUL eMIOS_1 — — —	I/O I/O — — —	M	Tristate	—	111	135
Port H										

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN_1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	93	117
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	94	118
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	95	119
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	96	120
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	134	162
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	135	163
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC_0	I/O I/O — O	M	Tristate	—	136	164
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	137	165
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	138	166
PH[9][8]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	88	127	155
PH[10][8]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	81	120	148

Table 2. Functional port pins (continued)

Port pin	PCR register	Alternate function[1]	Function	Peripheral	I/O direction	Pad type[2]	RESET config.[3]	Pin number		
								100 LQFP	144 LQFP	176 LQFP
PH[11]	PCR[123]	AF0 AF1 AF2 AF3	GPIO[123] SOUT_3 CS0_4 E1UC[5]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O O I/O I/O	M	Tristate	—	—	140
PH[12]	PCR[124]	AF0 AF1 AF2 AF3	GPIO[124] SCK_3 CS1_4 E1UC[25]	SIUL DSPI_3 DSPI_4 eMIOS_1	I/O I/O I/O —	M	Tristate	—	—	141
PH[13]	PCR[125]	AF0 AF1 AF2 AF3	GPIO[125] SOUT_4 CS0_3 E1UC[26]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O O I/O —	M	Tristate	—	—	9
PH[14]	PCR[126]	AF0 AF1 AF2 AF3	GPIO[126] SCK_4 CS1_3 E1UC[27]	SIUL DSPI_4 DSPI_3 eMIOS_1	I/O I/O I/O —	M	Tristate	—	—	10
PH[15]	PCR[127]	AF0 AF1 AF2 AF3	GPIO[127] SOUT_5 — E1UC[17]	SIUL DSPI_5 — eMIOS_1	I/O O — —	M	Tristate	—	—	8
Port I										
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	172
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKUP[24][4] —	SIUL eMIOS_0 — — WKUP —	I/O I/O — — I —	S	Tristate	—	—	171
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	170
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKUP[23][4] —	SIUL eMIOS_0 — — WKUP —	I/O I/O — — I —	S	Tristate	—	—	169
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	143

[4] All WKUP pins also support external interrupt capability. See the WKPU chapter of the *MPC5606BK Microcontroller Reference Manual* for further details.

[5] NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

[6] "Not applicable" because these functions are available only while the device is booting. See the BAM chapter of the *MPC5606BK Microcontroller Reference Manual* for details.

[7] Value of PCR.IBE bit must be 0.

[8] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
It is up to the user to configure these pins as GPIO when needed.

[9] PC[1] is a fast/medium pad but is in medium configuration by default. This pad is in Alternate Function 2 mode after reset which has TDO functionality. The reset value of PCR.OBE is 1, but this setting has no impact as long as this pad stays in AF2 mode. After configuring this pad as GPIO (PCR.PA = 0), output buffer is enabled as reset value of PCR.OBE = 1.

[10] Not available in 100LQFP package.

Table 3. Pad types

Type	Description
F	Fast
I	Input only with analog feature
J	Input/output with analog feature
M	Medium
S	Slow

3 Electrical characteristics

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 4 are used and the parameters are tagged accordingly in the tables where appropriate.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

3.4 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}[3]	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}[4]	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0[5]	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up[6]	—	3.0[7]	0.25 V/µs	V/s

Table 19. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 20 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below the 100%.

Table 20. I/O weight[1]

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
6	4	4	PB[3]	5%	—	6%	—	13%	—	15%	—
			PC[9]	4%	—	5%	—	13%	—	15%	—
			PC[14]	4%	—	4%	—	13%	—	15%	—
			PC[15]	3%	4%	4%	4%	12%	18%	15%	16%
	—	—	PJ[4]	3%	4%	3%	3%	—	—	—	—

Table 20. I/O weight[1] (continued)

Supply segment			Pad	176 LQFP				144/100 LQFP			
				Weight 5 V		Weight 3.3 V		Weight 5 V		Weight 3.3 V	
176 LQFP	144 LQFP	100 LQFP		SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1	SRC = 0	SRC = 1
3	2	2	PB[9]	1%	—	1%	—	1%	—	1%	—
			PB[8]	1%	—	1%	—	1%	—	1%	—
			PB[10]	5%	—	6%	—	6%	—	7%	—
		—	PF[0]	5%	—	6%	—	6%	—	8%	—
		—	PF[1]	5%	—	6%	—	7%	—	8%	—
		—	PF[2]	6%	—	7%	—	7%	—	9%	—
		—	PF[3]	6%	—	7%	—	8%	—	9%	—
		—	PF[4]	6%	—	7%	—	8%	—	10%	—
		—	PF[5]	6%	—	7%	—	9%	—	10%	—
		—	PF[6]	6%	—	7%	—	9%	—	11%	—
		—	PF[7]	6%	—	7%	—	9%	—	11%	—
	—	—	PJ[3]	6%	—	7%	—	—	—	—	—
	—	—	PJ[2]	6%	—	7%	—	—	—	—	—
	—	—	PJ[1]	6%	—	7%	—	—	—	—	—
	—	—	PJ[0]	6%	—	7%	—	—	—	—	—
	—	—	PI[15]	6%	—	7%	—	—	—	—	—
	—	—	PI[14]	6%	—	7%	—	—	—	—	—
	2	2	PD[0]	1%	—	1%	—	1%	—	1%	—
			PD[1]	1%	—	1%	—	1%	—	1%	—
			PD[2]	1%	—	1%	—	1%	—	1%	—
			PD[3]	1%	—	1%	—	1%	—	1%	—
			PD[4]	1%	—	1%	—	1%	—	1%	—
			PD[5]	1%	—	1%	—	1%	—	1%	—
			PD[6]	1%	—	1%	—	1%	—	2%	—
			PD[7]	1%	—	1%	—	1%	—	2%	—

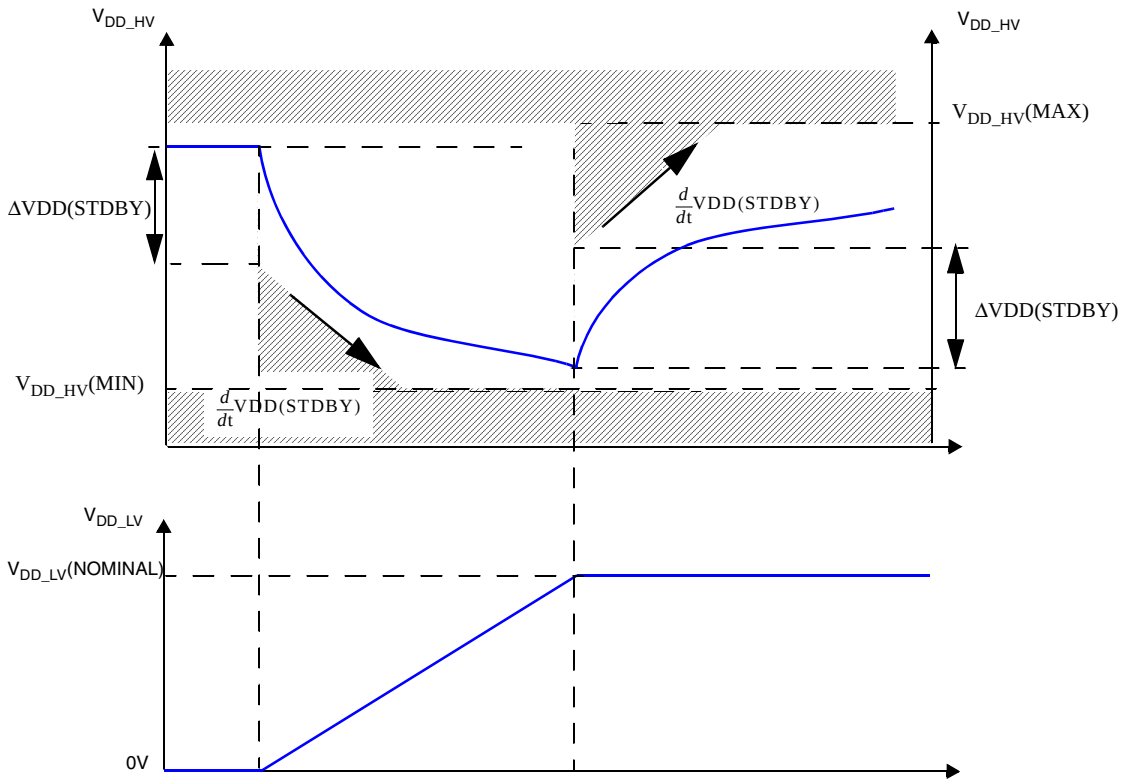


Figure 10. V_{DD} and V_{DD_BV} supply constraints during STANDBY mode exit

Table 22. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	Ω
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	P	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
				After trimming	1.15	1.28	1.32	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV3B monitors VDD_BV to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10% range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

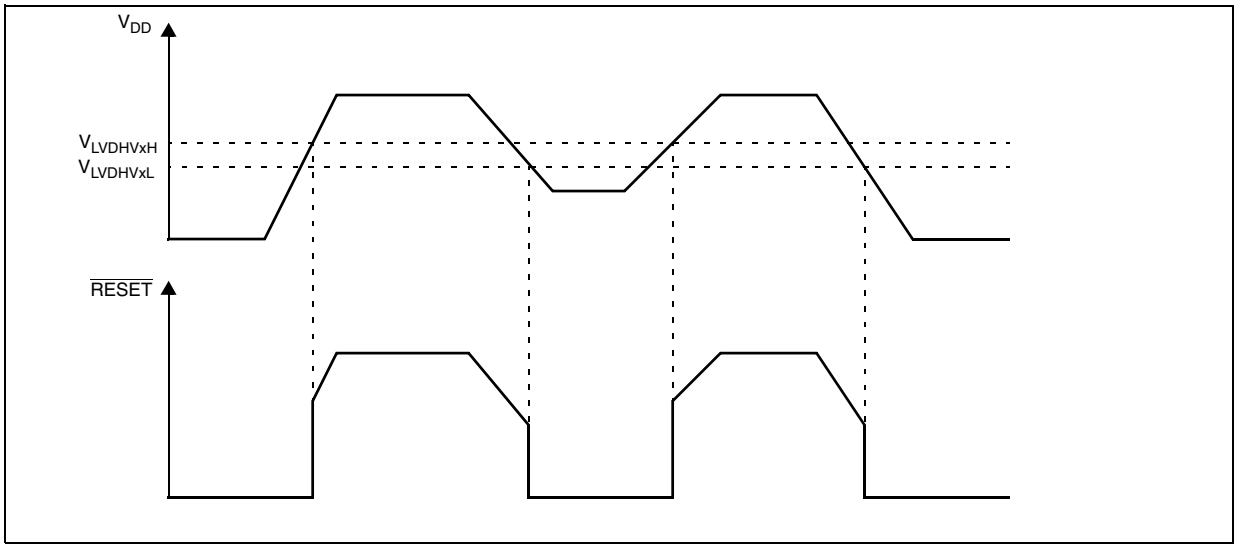


Figure 11. Low voltage monitor vs. reset

Table 23. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	D	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV3BH}$	CC	T	LVDHV3B low voltage detector high threshold		—	—	2.95	
$V_{LVDHV3BL}$	CC	P	LVDHV3BL low voltage detector low threshold		2.6	—	2.9	
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	—	
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.14	

[1] V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

[4] Higher current may be sunk by device during power-up and standby exit. Please refer to inrush current in Table 22.

[5] RUN current measured with typical application with accesses on both Flash and RAM.

[6] Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

[7] Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.

[8] Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

[9] Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

[10] ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

3.10 Flash memory electrical characteristics

3.10.1 Program/erase characteristics

Table 25 shows the program and erase characteristics.

Table 25. Program and erase specifications

Symbol		C	Parameter	Conditions	Value				Unit
					Min	Typ[1]	Initial max[2]	Max[3]	
$T_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	Code Flash	—	18	50	500	µs
				Data Flash		22			
$T_{16Kpperase}$			16 KB block preprogram and erase time	Code Flash	—	200	500	5000	ms
				Data Flash		300			
$T_{32Kpperase}$			32 KB block preprogram and erase time	Code Flash	—	300	600	5000	ms
				Data Flash		400			
$T_{32Kpperase}$			32 KB block preprogram and erase time for sector B0F4	Code Flash	—	600	1200	10000	ms
$T_{128Kpperase}$			128 KB block preprogram and erase time	Code Flash	—	600	1300	7500	ms
				Data Flash		800			
$T_{128Kpperase}$			128 KB block preprogram and erase time for sector B0F5	Code Flash	—	1200	2600	15000	ms
T_{eslat}		D	Erase Suspend Latency	—	—	—	30	30	µs
T_{ESRT}		C	Erase Suspend Request Rate	Code Flash	20	—	—	—	ms
				Data Flash	10	—	—	—	

Table 31. ESD absolute maximum ratings[1,2]

Symbol	Ratings	Conditions	Class	Max value[3]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	
				750 (corners)	

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production

3.11.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 32. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.12 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 12 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 33 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

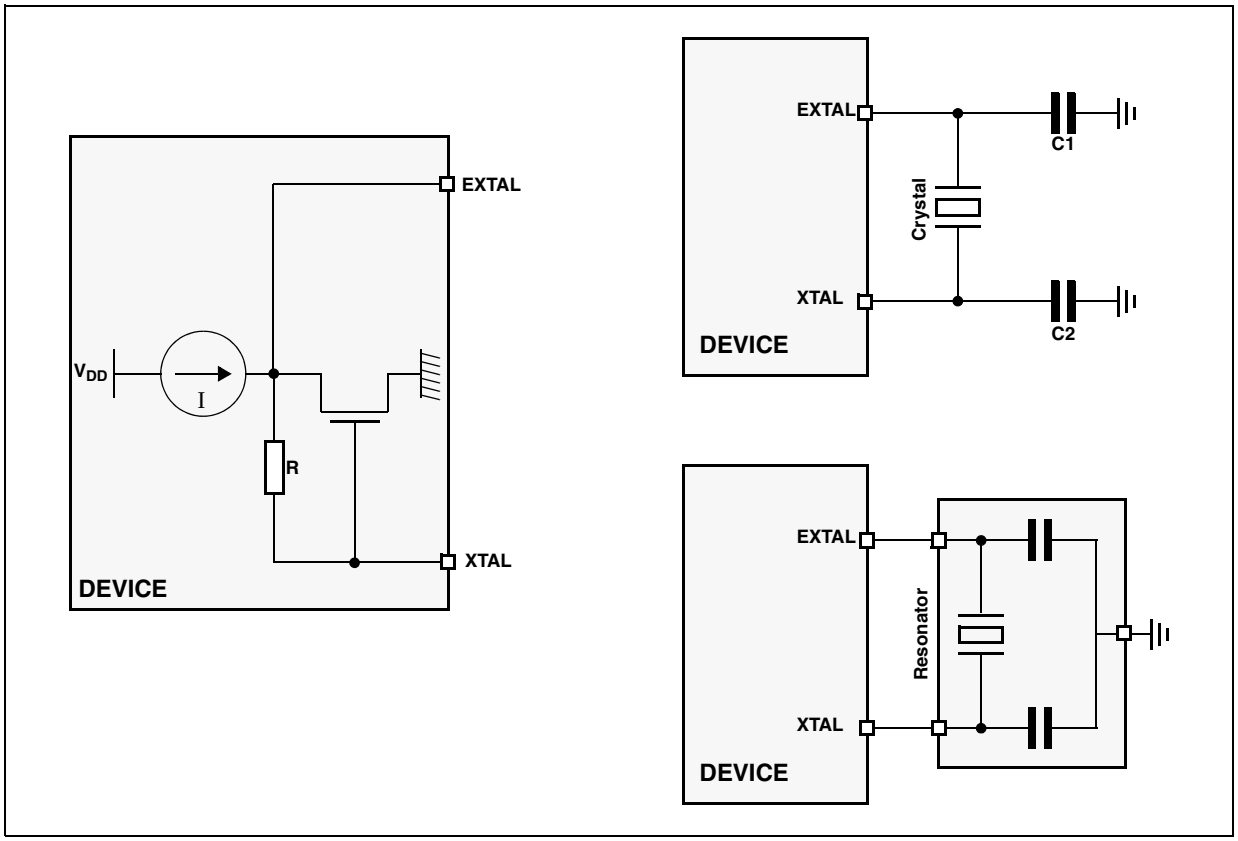


Figure 12. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 33. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout C1 = C2 (pF)[1]	Shunt capacitance between xtalout and xtalin C0[2] (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

[1] The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

[2] The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

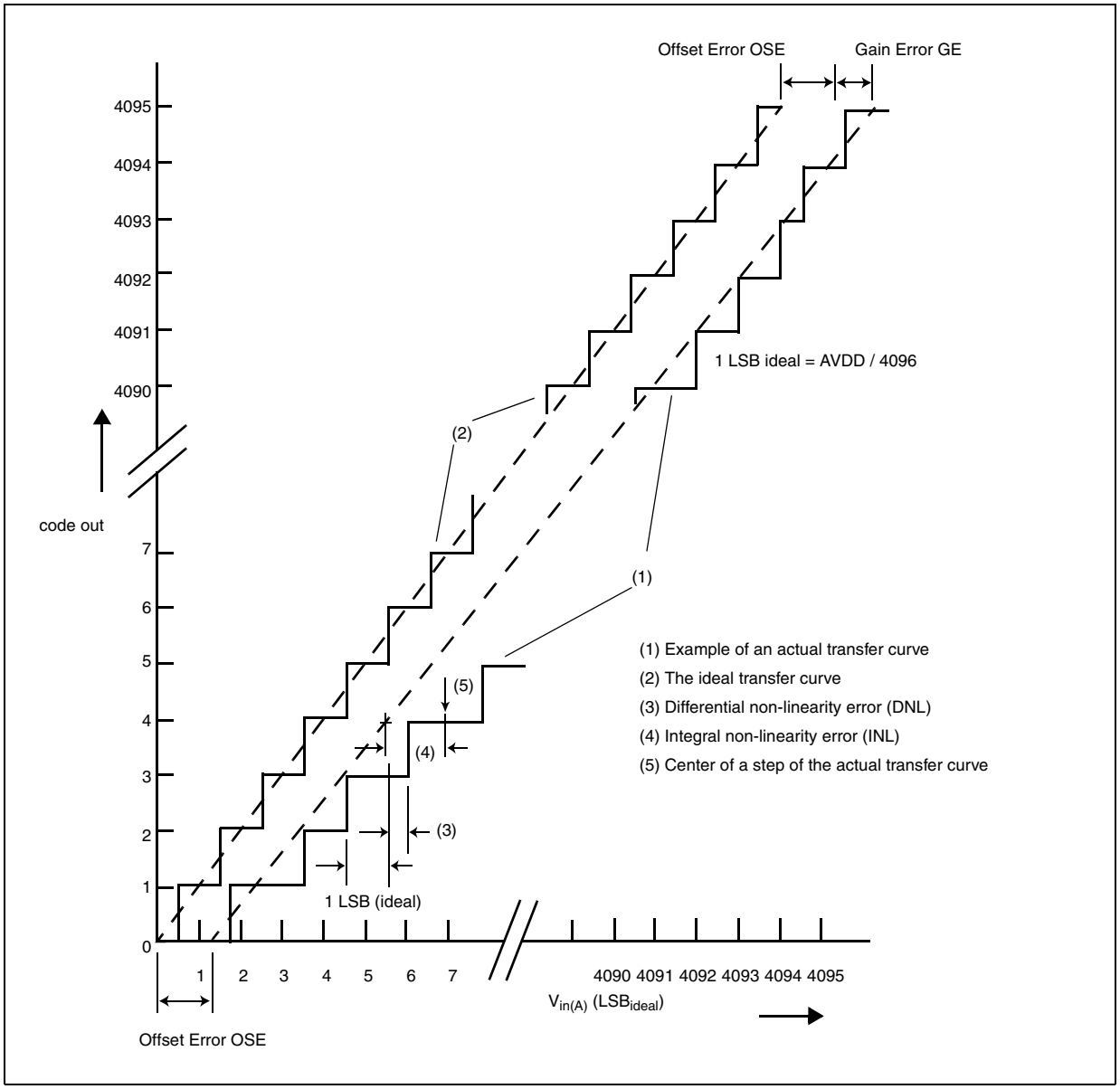


Figure 22. ADC_1 characteristic and error definitions

Table 42. ADC_1 conversion characteristics (12-bit ADC_1)

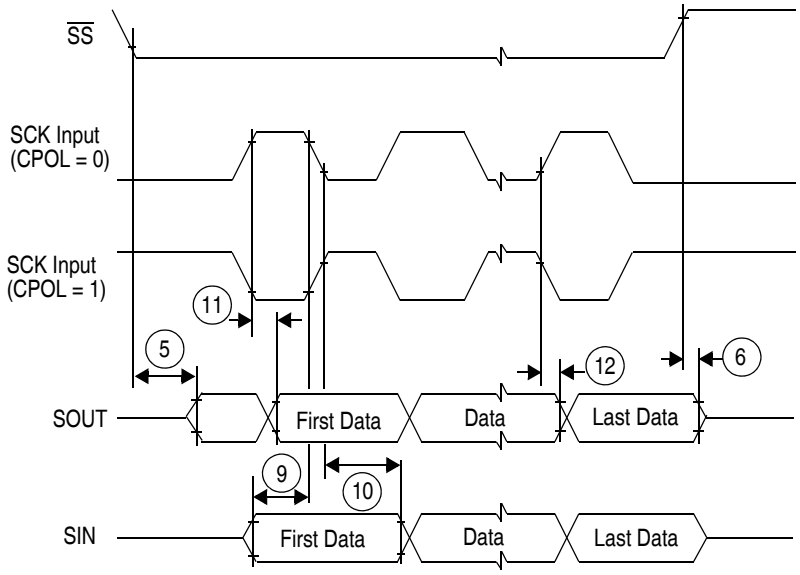
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC1}	SR	—	Voltage on VSS_HV_ADC1 (ADC_1 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC1}	SR	—	Voltage on VDD_HV_ADC1 pin (ADC_1 reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V

3.18 On-chip peripherals

3.18.1 Current consumption

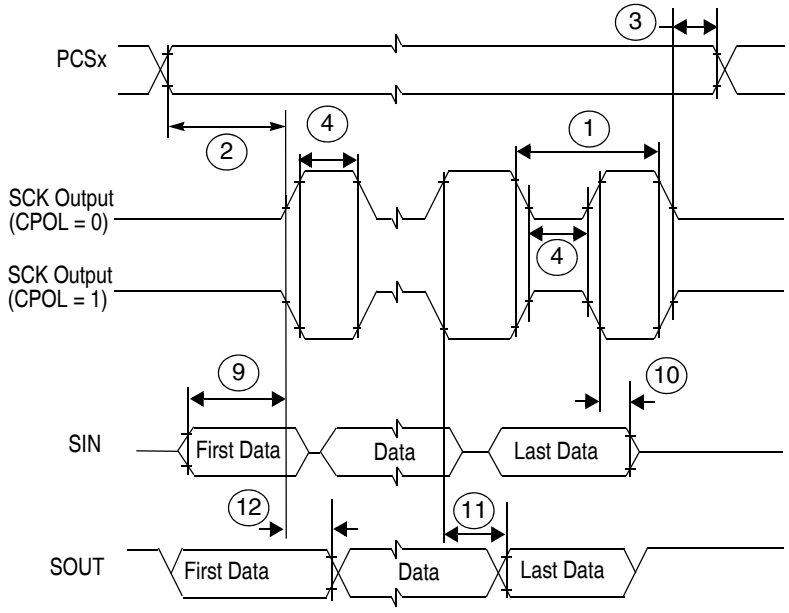
Table 43. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Value (Typ)	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	Bit rate = 500 KB/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 * f_{periph} + 85	µA
				Bit rate = 125 KB/s		8 * f_{periph} + 27	
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 * f_{periph}	
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baud rate: 20 KB/s		5 * f_{periph} + 31	
$I_{DD\_BV(SPI)}$	CC	T	SPI (DSPI) supply current on V_{DD_BV}	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): • Baud rate: 2 Mb/s • Transmission every 8 µs • Frame: 16 bits		16 * f_{periph}	
I_{DD_BV} (ADC_0/ADC_1)	CC	T	ADC_0/ADC_1 supply current on V_{DD_BV}	V_{DD} = 5.5 V	Ballast static consumption (no conversion)	41 * f_{periph}	µA
				V_{DD} = 5.5 V	Ballast dynamic consumption (continuous conversion)	46 * f_{periph}	
$I_{DD\_HV\_ADC0}$	CC	T	ADC_0 supply current on $V_{DD\_HV\_ADC0}$	V_{DD} = 5.5 V	Analog static consumption (no conversion)	200	
				V_{DD} = 5.5 V	Analog dynamic consumption (continuous conversion)	3	mA



Note: Numbers shown reference Table 44.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Numbers shown reference Table 44.

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

4.1.3 100 LQFP

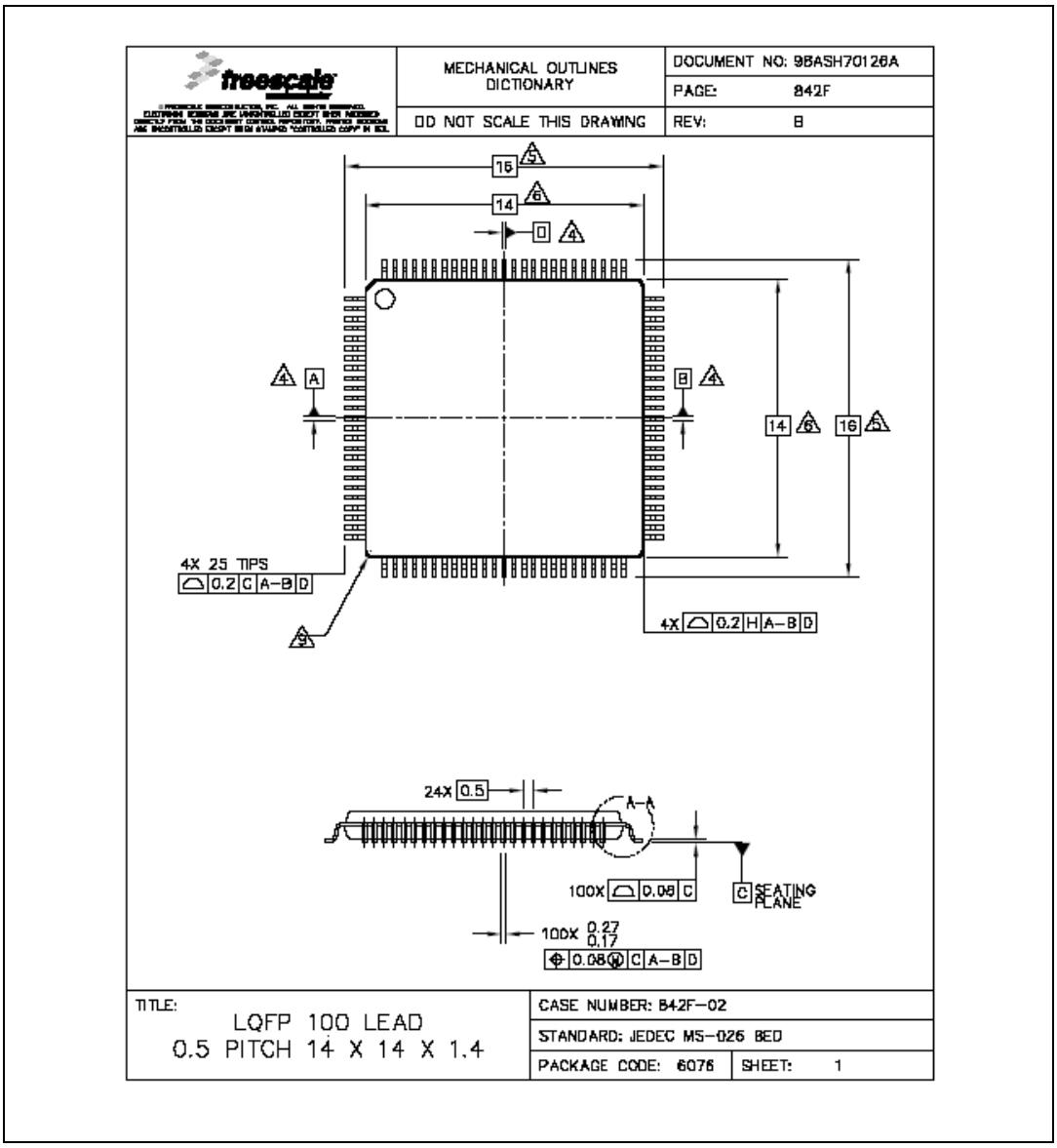


Figure 38. 100 LQFP package mechanical drawing (Part 1 of 3)

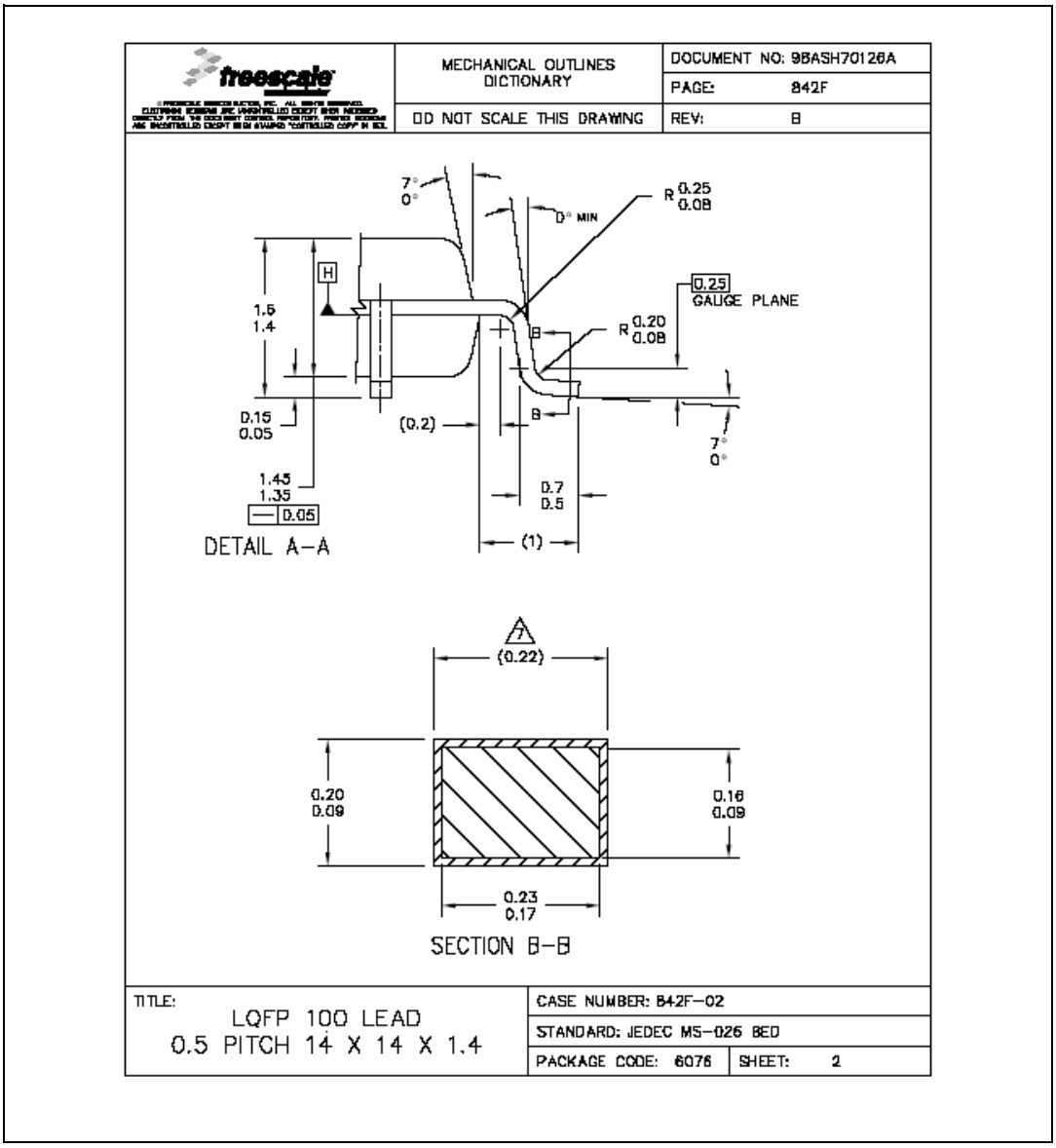
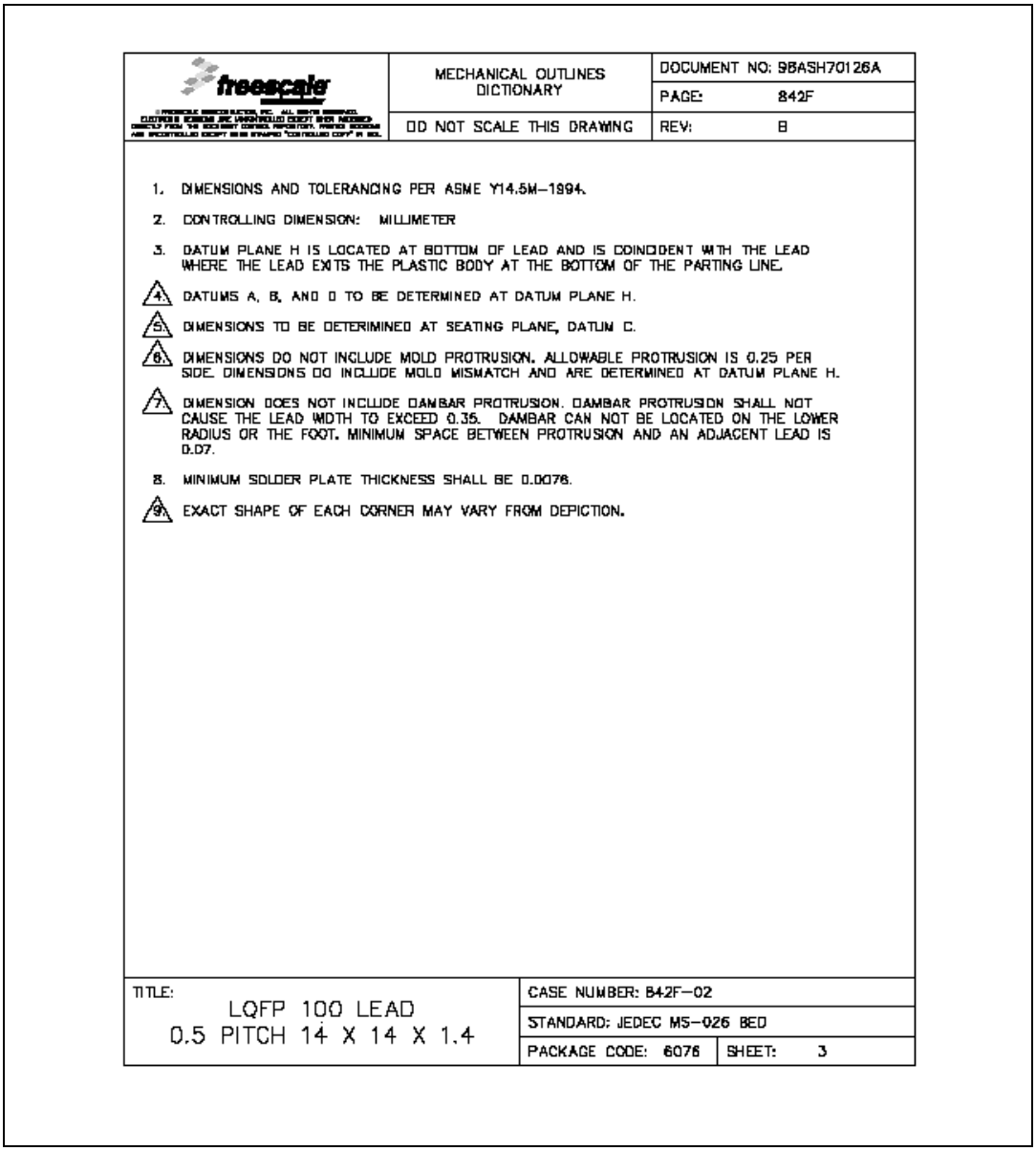


Figure 39. 100 LQFP package mechanical drawing (Part 2 of 3)



freescale	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH70126A
		PAGE: 842F
	DO NOT SCALE THIS DRAWING	REV: B

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERIMINED AT SEATING PLANE, DATUM C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

TITLE: LQFP 100 LEAD 0.5 PITCH 14 X 14 X 1.4	CASE NUMBER: 842F–02	
	STANDARD: JEDEC MS–026 BED	
	PACKAGE CODE: 6076	SHEET: 3

Figure 40. 100 LQFP package mechanical drawing (Part 3 of 3)