**Welcome to E-XFL.COM**

## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed Point |
| Interface | Synchronous Serial Port (SSP) |
| Clock Rate | 33.3MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 80kB |
| Voltage - I/O | 5.00V |
| Voltage - Core | 5.00V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-BQFP |
| Supplier Device Package | 128-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-2181bsz-133 |

# ADSP-2181* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- EZ-ICE® Serial Emulator for ADSP-218x Processor Family

## DOCUMENTATION

**Application Notes**

- AN-1: ADSP-21xx Legacy Application Notes
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-334: Digital Signal Processing Techniques
- AN-348: Avoiding Passive-Component Pitfalls
- AN-400: Considerations for Selecting a DSP Processor -- Why Buy the ADSP-2181?
- AN-415: ADSP-2181 IDMA Interface to Motorola MC68300 Family of Microprocessors
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- AN-543: High Quality, All-Digital RF Frequency Modulation Generation with the ADSP-2181 and the AD9850 DDS
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x

ADSP-2181 can fetch an operand from program memory and the next instruction in the same cycle.

In addition to the address and data bus for external memory connection, the ADSP-2181 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2181 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2181 can respond to 13 possible interrupts, eleven of which are accessible at any given time. There can be up to six external interrupts (one edge-sensitive, two level-sensitive and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port and the power-down circuitry. There is also a master $\overline{RESET}$ signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2181 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

**Serial Ports**

The ADSP-2181 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2181 SPORTs. Refer to the *ADSP-2100 Family User's Manual, Third Edition* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.

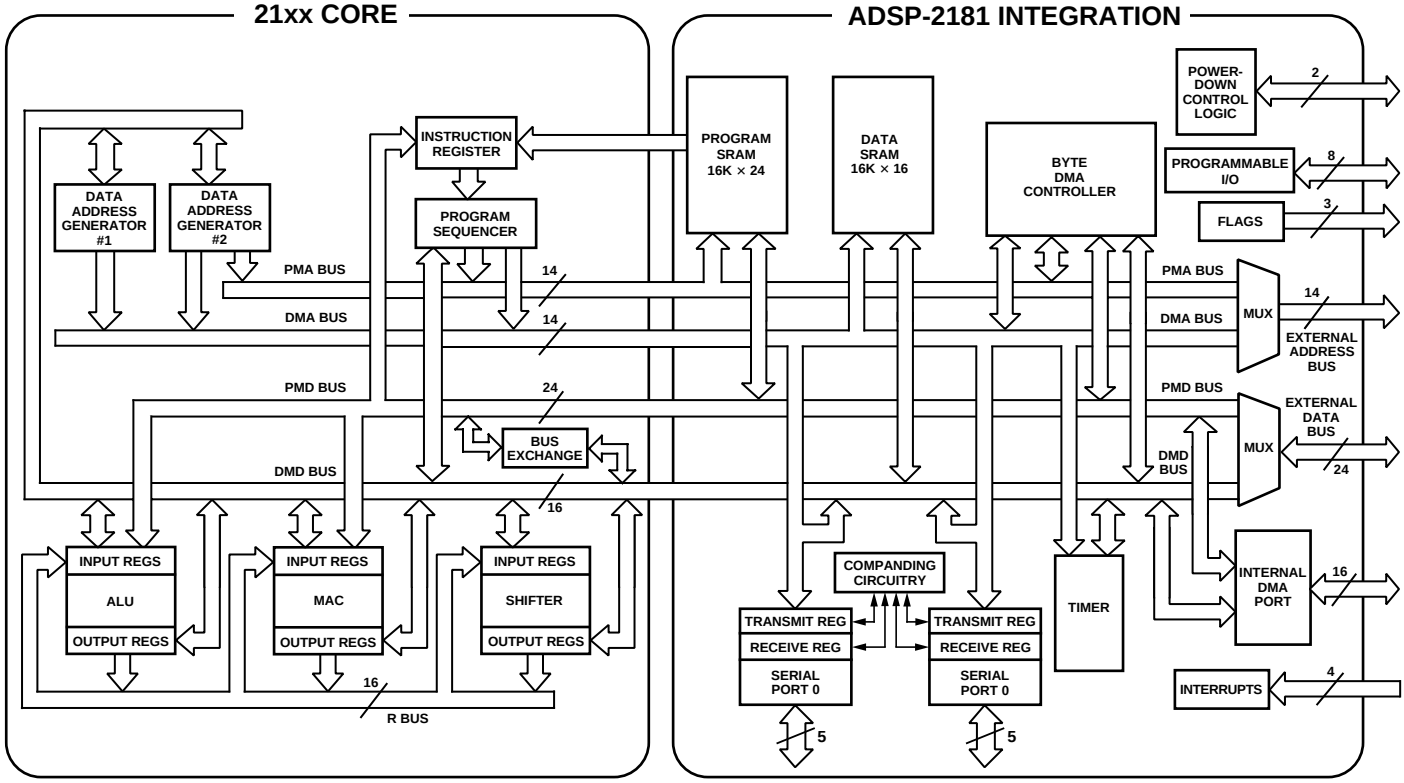



*Figure 1. ADSP-2181 Block Diagram*

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-2181 will remain in the idle state for up to a maximum of *n* processor cycles (*n* = 16, 32, 64 or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of *n* processor cycles).

**SYSTEM INTERFACE**

Figure 2 shows a typical basic system configuration with the ADSP-2181, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories. Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2181 also provides four external interrupts and two serial ports or six external interrupts and one serial port.

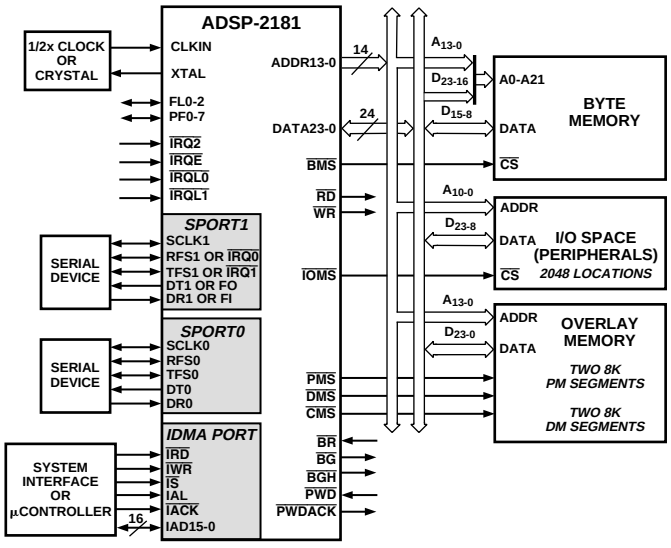



*Figure 2. ADSP-2181 Basic System Configuration*

**Clock Signals**

The ADSP-2181 can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual, Third Edition*, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-2181 uses an input clock with a frequency equal to half the instruction rate; a 20.00 MHz input clock yields a 25 ns processor cycle (which is equivalent to 40 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2181 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

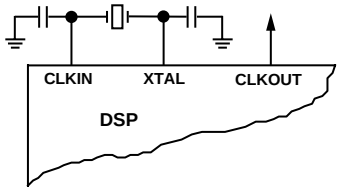



*Figure 3. External Crystal Connections*

**Reset**

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2181. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid $V_{DD}$ is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, $t_{RSP}$.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

**Memory Architecture**
The ADSP-2181 provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory and I/O.

**Program Memory** is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2181 has 16K words of Program Memory RAM on chip and the capability of accessing up to two 8K external memory overlay spaces using the external data bus. Both an instruction opcode and a data value can be read from on-chip program memory in a single cycle.

**Data Memory** is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2181 has 16K words on Data Memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

**Byte Memory** provides access to an 8-bit wide memory space through the Byte DMA (BDMA) port. The Byte Memory interface provides access to 4 MBytes of memory by utilizing eight data lines as additional address lines. This gives the BDMA Port an effective 22-bit address range. On power-up, the DSP can automatically load bootstrap code from byte memory.

**I/O Space** allows access to 2048 locations of 16-bit-wide data. It is intended to be used to communicate with parallel peripheral devices such as data converters and external registers or latches.

**Program Memory**
The ADSP-2181 contains a 16K × 24 on-chip program RAM. The on-chip program memory is designed to allow up to two accesses each cycle so that all operations can complete in a single cycle. In addition, the ADSP-2181 allows the use of 8K external memory overlays.

The program memory space organization is controlled by the MMAP pin and the PMOVLAY register. Normally, the ADSP-2181 is configured with MMAP = 0 and program memory organized as shown in Figure 4.

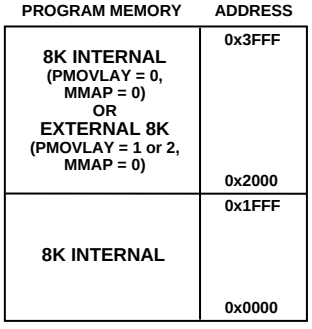



*Figure 4. Program Memory (MMAP = 0)*

There are 16K words of memory accessible internally when the PMOVLAY register is set to 0. When PMOVLAY is set to something other than 0, external accesses occur at addresses 0x2000 through 0x3FFF. The external address is generated as shown in Table II.

**Table II.**

| PMOVLAY | Memory | A13 | A12:0 |
|---|---|---|---|
| 0 | Internal | Not Applicable | Not Applicable |
| 1 | External Overlay 1 | 0 | 13 LSBs of Address Between 0x2000 and 0x3FFF |
| 2 | External Overlay 2 | 1 | 13 LSBs of Address Between 0x2000 and 0x3FFF |

This organization provides for two external 8K overlay segments using only the normal 14 address bits. This allows for simple program overlays using one of the two external segments in place of the on-chip memory. Care must be taken in using this overlay space in that the processor core (i.e., the sequencer) does not take into account the PMOVLAY register value. For example, if a loop operation was occurring on one of the external overlays and the program changes to another external overlay or internal memory, an incorrect loop operation could occur. In addition, care must be taken in interrupt service routines as the overlay registers are not automatically saved and restored on the processor mode stack.

For ADSP-2100 Family compatibility, MMAP = 1 is allowed. In this mode, booting is disabled and overlay memory is disabled (PMOVLAY must be 0). Figure 5 shows the memory map in this configuration.

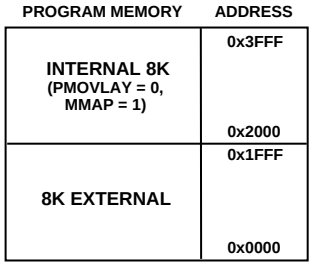



*Figure 5. Program Memory (MMAP = 1)*

**Data Memory**
The ADSP-2181 has 16,352 16-bit words of internal data memory. In addition, the ADSP-2181 allows the use of 8K external memory overlays. Figure 6 shows the organization of the data memory.

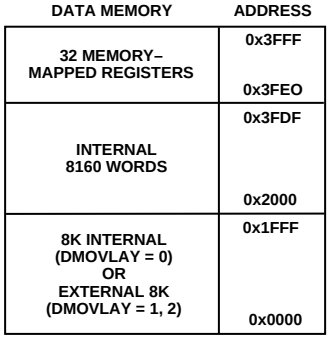



*Figure 6. Data Memory*

There are 16,352 words of memory accessible internally when the DMOVLAY register is set to 0. When DMOVLAY is set to something other than 0, external accesses occur at addresses 0x0000 through 0x1FFF. The external address is generated as shown in Table III.

**Table III.**

| DMOVLAY | Memory | A13 | A12:0 |
|---|---|---|---|
| 0 | Internal | Not Applicable | Not Applicable |
| 1 | External Overlay 1 | 0 | 13 LSBs of Address Between 0x0000 and 0x1FFF |
| 2 | External Overlay 2 | 1 | 13 LSBs of Address Between 0x0000 and 0x1FFF |

This organization allows for two external 8K overlays using only the normal 14 address bits.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

**I/O Space**

The ADSP-2181 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals or to bus interface ASIC data registers. I/O space supports 2048 locations. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0-3, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IV.

**Table IV.**

| Address Range | Wait State Register |
|---|---|
| 0x000–0x1FF | IOWAIT0 |
| 0x200–0x3FF | IOWAIT1 |
| 0x400–0x5FF | IOWAIT2 |
| 0x600–0x7FF | IOWAIT3 |

**Composite Memory Select ($\overline{\text{CMS}}$)**

The ADSP-2181 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

When set, each bit in the CMSSEL register, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the PMS and DMS bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory; use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits, except the $\overline{\text{BMS}}$ bit, default to 1 at reset.

**Byte Memory**

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2181 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

**Byte Memory DMA (BDMA)**

The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally, and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

The BDMA circuit supports four different data formats which are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table V shows the data formats supported by the BDMA circuit.

**Table V.**

| BTYPE | Internal Memory Space | Word Size | Alignment |
|---|---|---|---|
| 00 | Program Memory | 24 | Full Word |
| 01 | Data Memory | 16 | Full Word |
| 10 | Data Memory | 8 | MSBs |
| 11 | Data Memory | 8 | LSBs |

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register. The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory, regardless of the values of MMAP, PMOVLAY or DMOVLAY.

When the BWCOUNT register is written with a nonzero value, the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor and start execution at address 0 when the BDMA accesses have completed.

**Internal Memory DMA Port (IDMA Port)**

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2181. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-2181 is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location; the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can either be read from or written to the ADSP-2181's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-2181 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation.

**Bootstrap Loading (Booting)**

The ADSP-2181 has two mechanisms to allow automatic loading of the on-chip program memory after reset. The method for booting after reset is controlled by the MMAP and BMODE pins as shown in Table VI.

**Table VI. Boot Summary Table**

| MMAP | BMODE | Booting Method |
|---|---|---|
| 0 | 0 | BDMA feature is used in default mode to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. |
| 0 | 1 | IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. |
| 1 | X | Bootstrap features disabled. Program execution immediately starts from location 0. |

***BDMA Booting***

When the BMODE and MMAP pins specify BDMA booting (MMAP = 0, BMODE = 0), the ADSP-2181 initiates a BDMA boot sequence when reset is released. The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24 bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family Development Software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface.

***IDMA Booting***

The ADSP-2181 can also boot programs through its Internal DMA port. If BMODE = 1 and MMAP = 0, the ADSP-2181 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

The ADSP-2100 Family Development Software (Revision 5.02 and later) can generate IDMA compatible boot code.

**Bus Request and Bus Grant**

The ADSP-2181 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2181 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If Go Mode is enabled, the ADSP-2181 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2181 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2181 is ready to execute an instruction, but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2181 deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

**Flag I/O Pins**

The ADSP-2181 has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2181's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2181 has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1 and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

## INSTRUCTION SET DESCRIPTION

The ADSP-2181 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2181's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

## DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2181 has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

The ICE-Port interface consists of the following ADSP-2181 pins:

| | | |
|---|---|---|
| $\overline{EBR}$ | $\overline{EMS}$ | ELIN |
| $\overline{EBG}$ | $\overline{EINT}$ | ELOUT |
| $\overline{ERESET}$ | ECLK | EE |

These ADSP-2181 pins must be connected *only* to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2181 and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE:

| | |
|---|---|
| $\overline{BR}$ | $\overline{BG}$ |
| GND | $\overline{RESET}$ |

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2181 in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$ and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$ and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to the target system via a ribbon cable and a 14-pin female plug. The ribbon cable is 10 inches in length with one end fixed to the EZ-ICE. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

**Target Board Connector for EZ-ICE Probe**

The EZ-ICE connector (a standard pin strip header) is shown in Figure 7. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

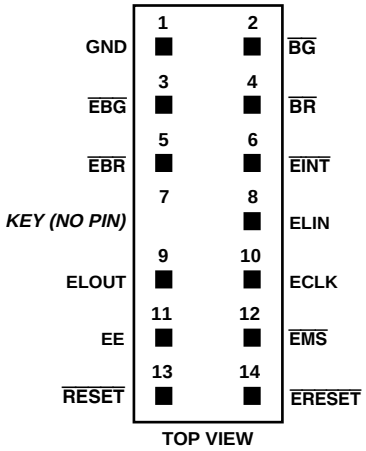



*Figure 7. Target Board Connector for EZ-ICE*

# ADSP-2181–SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

| Parameter | | K Grade Min | K Grade Max | B Grade Min | B Grade Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $T_{AMB}$ | Ambient Operating Temperature | 0 | +70 | –40 | +85 | °C |

## ELECTRICAL CHARACTERISTICS

| Parameter | | Test Conditions | K/B Grades Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Hi-Level Input Voltage[1, 2] | @ $V_{DD}$ = max | 2.0 | | | V |
| $V_{IH}$ | Hi-Level CLKIN Voltage | @ $V_{DD}$ = max | 2.2 | | | V |
| $V_{IL}$ | Lo-Level Input Voltage[1, 3] | @ $V_{DD}$ = min | | | 0.8 | V |
| $V_{OH}$ | Hi-Level Output Voltage[1, 4, 5] | @ $V_{DD}$ = min | | | | |
| | | $I_{OH}$ = –0.5 mA | 2.4 | | | V |
| | | @ $V_{DD}$ = min | | | | |
| | | $I_{OH}$ = –100 μA[6] | $V_{DD}$ – 0.3 | | | V |
| $V_{OL}$ | Lo-Level Output Voltage[1, 4, 5] | @ $V_{DD}$ = min | | | | |
| | | $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_{IH}$ | Hi-Level Input Current[3] | @ $V_{DD}$ = max | | | | |
| | | $V_{IN}$ = $V_{DD}$max | | | 10 | μA |
| $I_{IL}$ | Lo-Level Input Current[3] | @ $V_{DD}$ = max | | | | |
| | | $V_{IN}$ = 0 V | | | 10 | μA |
| $I_{OZH}$ | Three-State Leakage Current[7] | @ $V_{DD}$ = max | | | | |
| | | $V_{IN}$ = $V_{DD}$max[8] | | | 10 | μA |
| $I_{OZL}$ | Three-State Leakage Current[7] | @ $V_{DD}$ = max | | | | |
| | | $V_{IN}$ = 0 V[8] | | | 10 | μA |
| $I_{DD}$ | Supply Current (Idle)[9] | @ $V_{DD}$ = 5.0 | | | | |
| | | $T_{AMB}$ = +25°C | | | | |
| | | $t_{CK}$ = 34.7 ns | | 12 | | mA |
| | | $t_{CK}$ = 30 ns | | 13 | | mA |
| | | $t_{CK}$ = 25 ns | | 15 | | mA |
| $I_{DD}$ | Supply Current (Dynamic)[10] | @ $V_{DD}$ = 5.0 | | | | |
| | | $T_{AMB}$ = +25°C | | | | |
| | | $t_{CK}$ = 34.7 ns[11] | | 65 | | mA |
| | | $t_{CK}$ = 30 ns[11] | | 73 | | mA |
| | | $t_{CK}$ = 25 ns[11] | | 85 | | mA |
| $C_I$ | Input Pin Capacitance[3, 6, 12] | @ $V_{IN}$ = 2.5 V, | | | | |
| | | $f_{IN}$ = 1.0 MHz, | | | | |
| | | $T_{AMB}$ = +25°C | | | 8 | pF |
| $C_O$ | Output Pin Capacitance[6, 7, 12, 13] | @ $V_{IN}$ = 2.5 V, | | | | |
| | | $f_{IN}$ = 1.0 MHz, | | | | |
| | | $T_{AMB}$ = +25°C | | | 8 | pF |

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2-0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2186 outputs are CMOS-compatible and will drive to $V_{DD}$ and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RSF1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$, CLKIN Inactive.

[9]Idle refers to ADSP-2181 state of operation during execution of IDLE instruction. Deasserted pins are driven to either $V_{DD}$ or GND.

[10]$I_{DD}$ measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[11]$V_{IN}$ = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]Applies to TQFP and PQFP package types.

[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Interrupts and Flag** | | | | |
| *Timing Requirements*: | | | | |
| $t_{IFS}$ | $\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4] | $0.25t_{CK}$ + 15 | | ns |
| $t_{IFH}$ | $\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4] | $0.25t_{CK}$ | | ns |
| *Switching Characteristics:* | | | | |
| $t_{FOH}$ | Flag Output Hold after CLKOUT Low[5] | $0.5t_{CK}$ – 7 | | ns |
| $t_{FOD}$ | Flag Output Delay from CLKOUT Low[5] | | $0.5t_{CK}$ + 5 | ns |

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet $t_{IFS}$ and $t_{IFH}$ setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag outputs = PFx, FL0, FL1, FL2, Flag_out4.

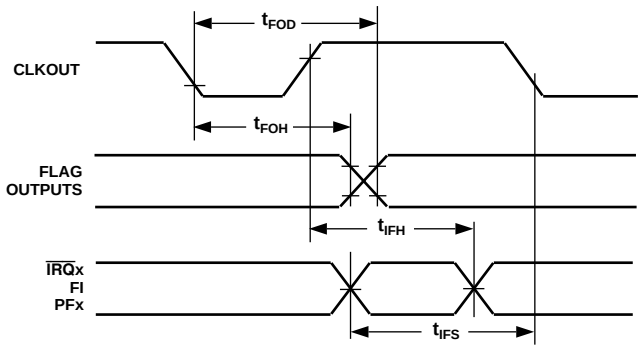



*Figure 9. Interrupts and Flags*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Bus Request/Grant** | | | | |
| *Timing Requirements*: | | | | |
| $t_{BH}$ | $\overline{BR}$ Hold after CLKOUT High[1] | $0.25t_{CK}$ + 2 | | ns |
| $t_{BS}$ | $\overline{BR}$ Setup before CLKOUT Low[1] | $0.25t_{CK}$ + 17 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{SD}$ | CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable | | $0.25t_{CK}$ + 10 | ns |
| $t_{SDB}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low | 0 | | ns |
| $t_{SE}$ | $\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable | 0 | | ns |
| $t_{SEC}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High | $0.25t_{CK}$ – 4 | | ns |
| $t_{SDBH}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2] | 0 | | ns |
| $t_{SEH}$ | $\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2] | 0 | | ns |

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual, Third Edition* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

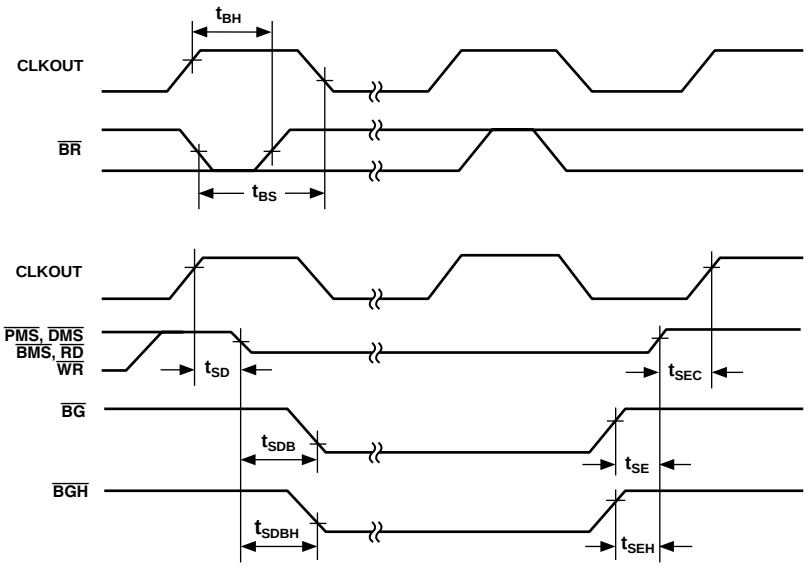



*Figure 10. Bus Request–Bus Grant*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Memory Read** | | | | |
| *Timing Requirements*: | | | | |
| $t_{RDD}$ | $\overline{RD}$ Low to Data Valid | | $0.5t_{CK} - 9 + w$ | ns |
| $t_{AA}$ | A0–A13, $\overline{xMS}$ to Data Valid | | $0.75t_{CK} - 10.5 + w$ | ns |
| $t_{RDH}$ | Data Hold from $\overline{RD}$ High | 0 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{RP}$ | $\overline{RD}$ Pulsewidth | $0.5t_{CK} - 5 + w$ | | ns |
| $t_{CRD}$ | CLKOUT High to $\overline{RD}$ Low | $0.25t_{CK} - 5$ | $0.25t_{CK} + 7$ | ns |
| $t_{ASR}$ | A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low | $0.25t_{CK} - 4$ | | ns |
| $t_{RDA}$ | A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted | $0.25t_{CK} - 3$ | | ns |
| $t_{RWR}$ | $\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low | $0.5t_{CK} - 5$ | | ns |

w = wait states × $t_{CK}$.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

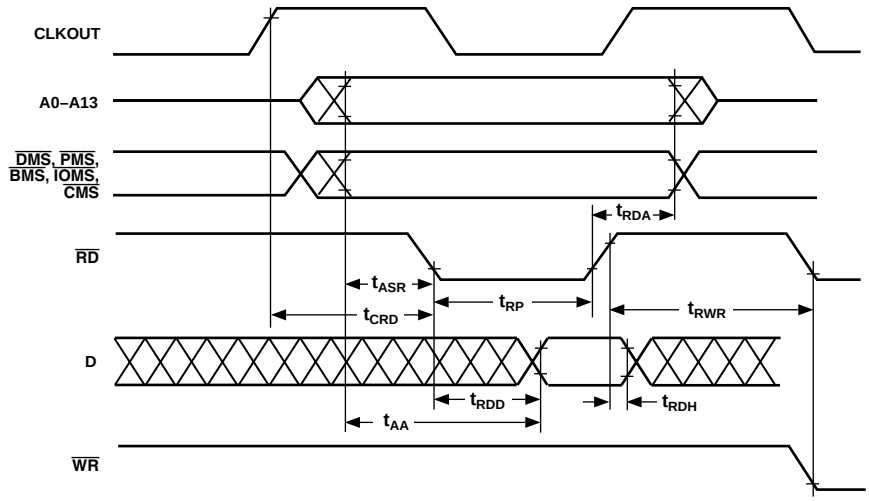



*Figure 11. Memory Read*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Memory Write** | | | | |
| *Switching Characteristics*: | | | | |
| $t_{DW}$ | Data Setup before $\overline{WR}$ High | $0.5t_{CK} - 7 + w$ | | ns |
| $t_{DH}$ | Data Hold after $\overline{WR}$ High | $0.25t_{CK} - 2$ | | ns |
| $t_{WP}$ | $\overline{WR}$ Pulsewidth | $0.5t_{CK} - 5 + w$ | | ns |
| $t_{WDE}$ | $\overline{WR}$ Low to Data Enabled | 0 | | ns |
| $t_{ASW}$ | A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low | $0.25t_{CK} - 4$ | | ns |
| $t_{DDR}$ | Data Disable before $\overline{WR}$ or $\overline{RD}$ Low | $0.25t_{CK} - 4$ | | ns |
| $t_{CWR}$ | CLKOUT High to $\overline{WR}$ Low | $0.25t_{CK} - 5$ | $0.25\ t_{CK} + 7$ | ns |
| $t_{AW}$ | A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted | $0.75t_{CK} - 9 + w$ | | ns |
| $t_{WRA}$ | A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted | $0.25t_{CK} - 3$ | | ns |
| $t_{WWR}$ | $\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low | $0.5t_{CK} - 5$ | | ns |

w = wait states × $t_{CK}$.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

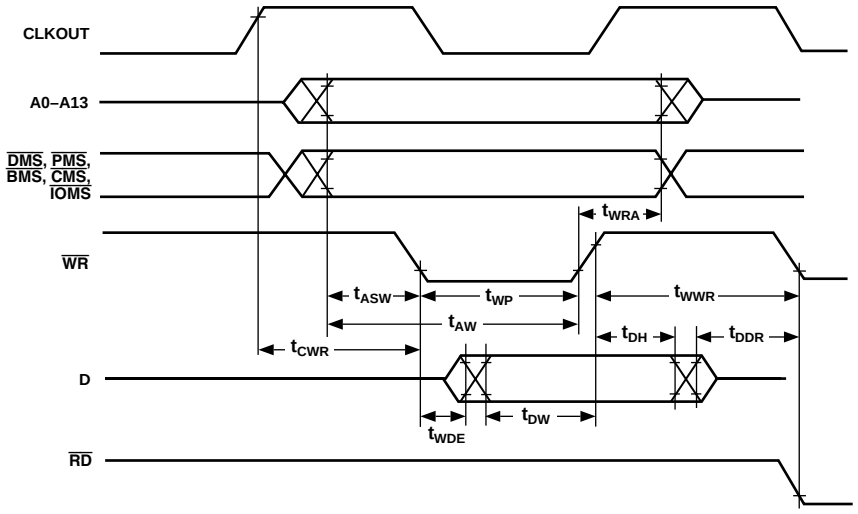



*Figure 12. Memory Write*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Serial Ports** | | | | |
| *Timing Requirements*: | | | | |
| $t_{SCK}$ | SCLK Period | 50 | | ns |
| $t_{SCS}$ | DR/TFS/RFS Setup before SCLK Low | 4 | | ns |
| $t_{SCH}$ | DR/TFS/RFS Hold after SCLK Low | 7 | | ns |
| $t_{SCP}$ | $SCLK_{IN}$ Width | 20 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{CC}$ | CLKOUT High to $SCLK_{OUT}$ | $0.25t_{CK}$ | $0.25t_{CK}$ + 10 | ns |
| $t_{SCDE}$ | SCLK High to DT Enable | 0 | | ns |
| $t_{SCDV}$ | SCLK High to DT Valid | | 15 | ns |
| $t_{RH}$ | $TFS/RFS_{OUT}$ Hold after SCLK High | 0 | | ns |
| $t_{RD}$ | $TFS/RFS_{OUT}$ Delay from SCLK High | | 15 | ns |
| $t_{SCDH}$ | DT Hold after SCLK High | 0 | | ns |
| $t_{TDE}$ | TFS (Alt) to DT Enable | 0 | | ns |
| $t_{TDV}$ | TFS (Alt) to DT Valid | | 14 | ns |
| $t_{SCDD}$ | SCLK High to DT Disable | | 15 | ns |
| $t_{RDV}$ | RFS (Multichannel, Frame Delay Zero) to DT Valid | | 15 | ns |

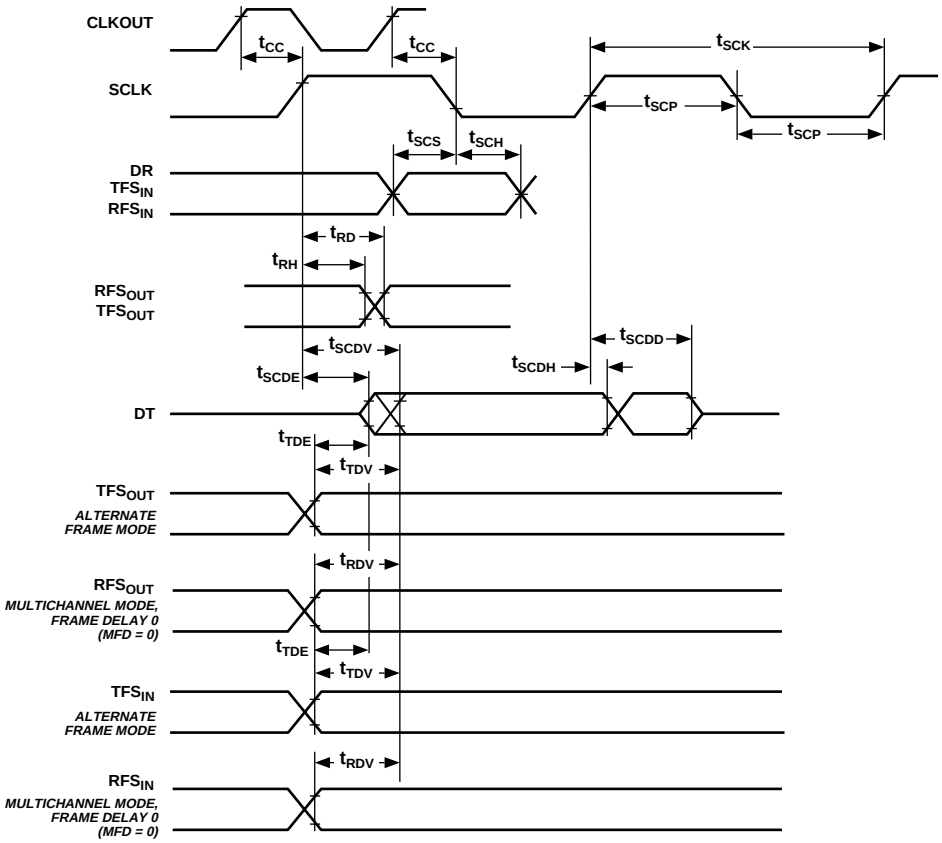



*Figure 13. Serial Ports*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Address Latch** | | | | |
| *Timing Requirements*: | | | | |
| $t_{IALP}$ | Duration of Address Latch[1, 2] | 10 | | ns |
| $t_{IASU}$ | IAD15–0 Address Setup before Address Latch End[2] | 5 | | ns |
| $t_{IAH}$ | IAD15–0 Address Hold after Address Latch End[2] | 2 | | ns |
| $t_{IKA}$ | $\overline{IACK}$ Low before Start of Address Latch[1] | 0 | | ns |
| $t_{IALS}$ | Start of Write or Read after Address Latch End[2, 3] | 3 | | ns |

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

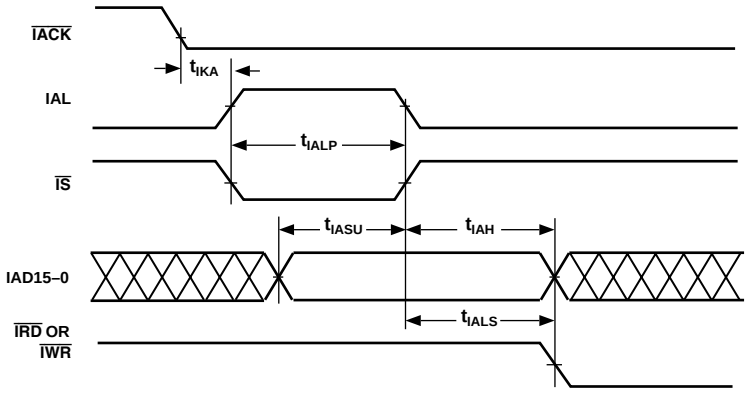



*Figure 14. IDMA Address Latch*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Read, Long Read Cycle** | | | | |
| *Timing Requirements*: | | | | |
| $t_{IKR}$ | $\overline{IACK}$ Low before Start of Read[1] | 0 | | ns |
| $t_{IRP}$ | Duration of Read | 15 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{IKHR}$ | $\overline{IACK}$ High after Start of Read[1] | | 15 | ns |
| $t_{IKDS}$ | IAD15–0 Data Setup before IACK Low | $0.5t_{CK} - 10$ | | ns |
| $t_{IKDH}$ | IAD15–0 Data Hold after End of Read[2] | 0 | | ns |
| $t_{IKDD}$ | IAD15–0 Data Disabled after End of Read[2] | | 12 | ns |
| $t_{IRDE}$ | IAD15–0 Previous Data Enabled after Start of Read | 0 | | ns |
| $t_{IRDV}$ | IAD15–0 Previous Data Valid after Start of Read | | 15 | ns |
| $t_{IRDH1}$ | IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3] | $2t_{CK} - 5$ | | ns |
| $t_{IRDH2}$ | IAD15–0 Previous Data Hold after Start of Read (PM2)[4] | $t_{CK} - 5$ | | ns |

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

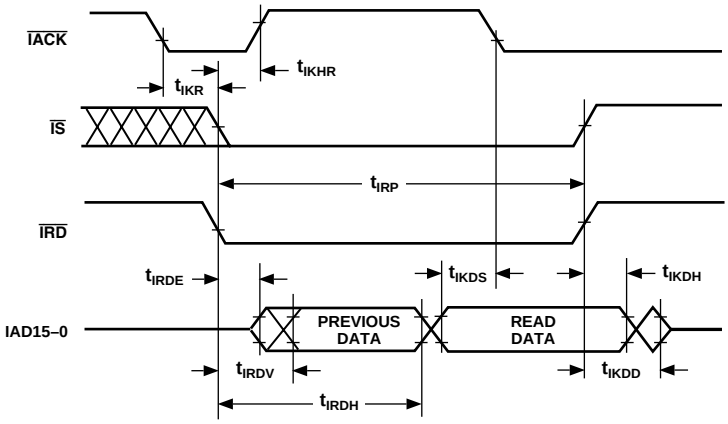



*Figure 17. IDMA Read, Long Read Cycle*

## CAPACITIVE LOADING

Figures 22 and 23 show the capacitive loading characteristics of the ADSP-2181.

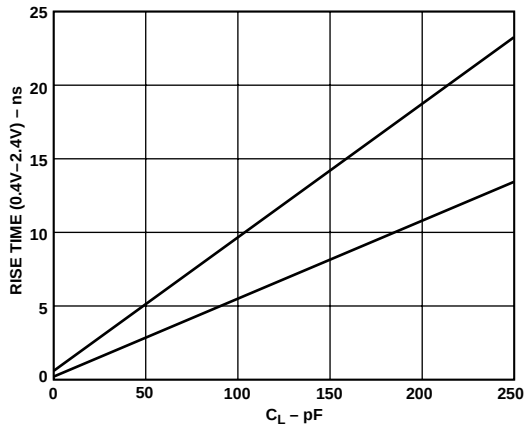



*Figure 22. Range of Output Rise Time vs. Load Capacitance, $C_L$ (at Maximum Ambient Operating Temperature)*

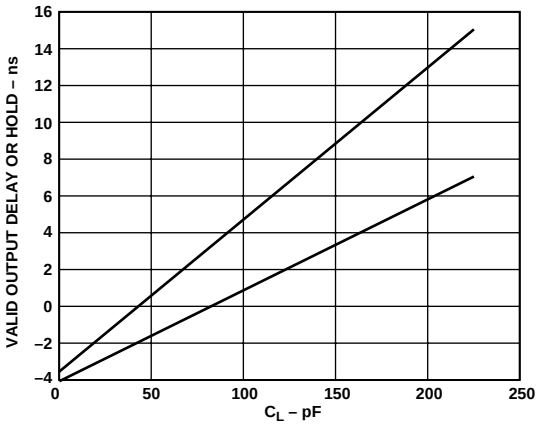



*Figure 23. Range of Output Valid Delay or Hold vs. Load Capacitance, $C_L$ (at Maximum Ambient Operating Temperature)*

## TEST CONDITIONS

### Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time ($t_{DIS}$) is the difference of $t_{MEASURED}$ and $t_{DECAY}$, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, $t_{DECAY}$, is dependent on the capacitive load, $C_L$, and the current load, $i_L$, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.


*Figure 24. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)*

### Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time ($t_{ENA}$) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

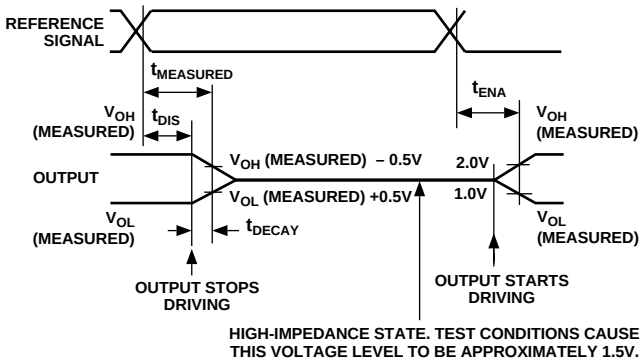



*Figure 25. Output Enable/Disable*

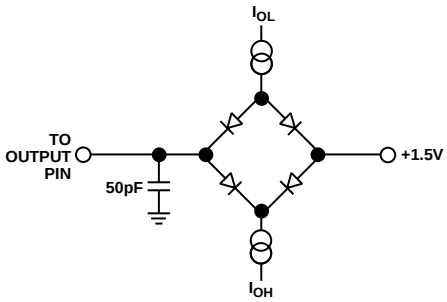



*Figure 26. Equivalent Device Loading for AC Measurements (Including All Fixtures)*

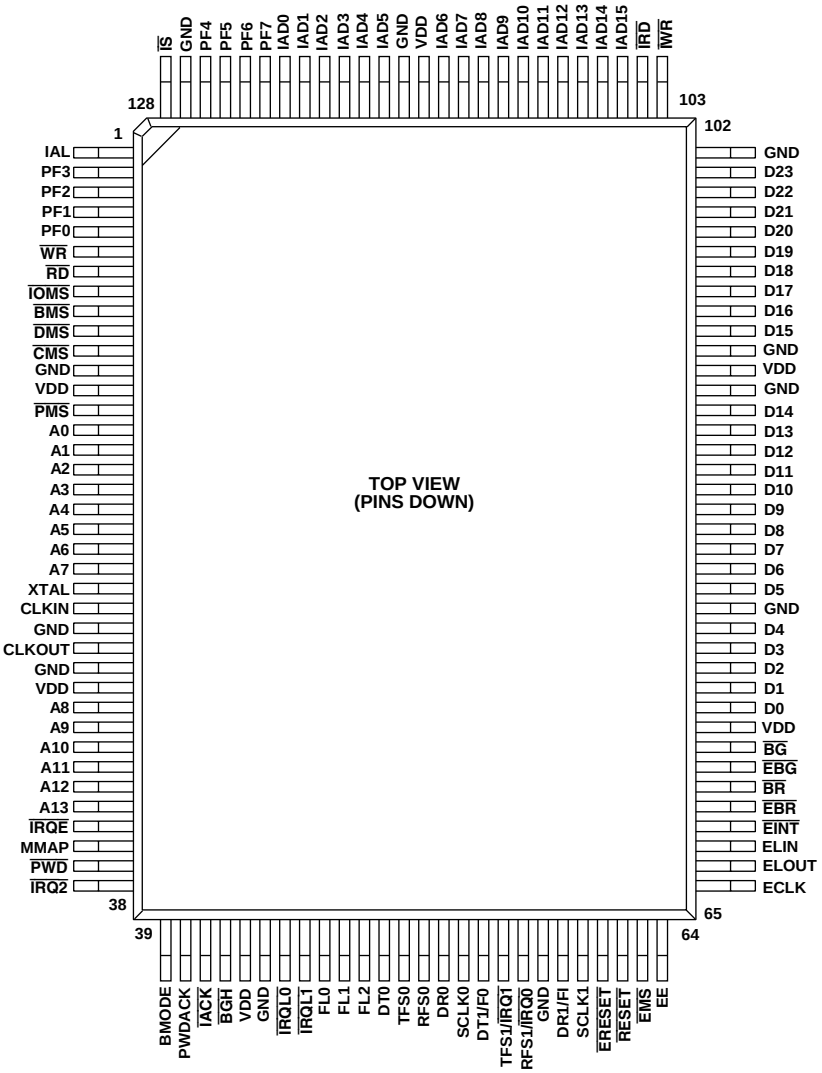
**ENVIRONMENTAL CONDITIONS**

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
$T_{CASE}$ = Case Temperature in °C
PD = Power Dissipation in W
$\theta_{CA}$ = Thermal Resistance (Case-to-Ambient)
$\theta_{JA}$ = Thermal Resistance (Junction-to-Ambient)
$\theta_{JC}$ = Thermal Resistance (Junction-to-Case)

| **Package** | $\theta_{JA}$ | $\theta_{JC}$ | $\theta_{CA}$ |
|---|---|---|---|
| TQFP | 50°C/W | 2°C/W | 48°C/W |
| PQFP | 41°C/W | 10°C/W | 31°C/W |

**128-Lead TQFP Package Pinout**



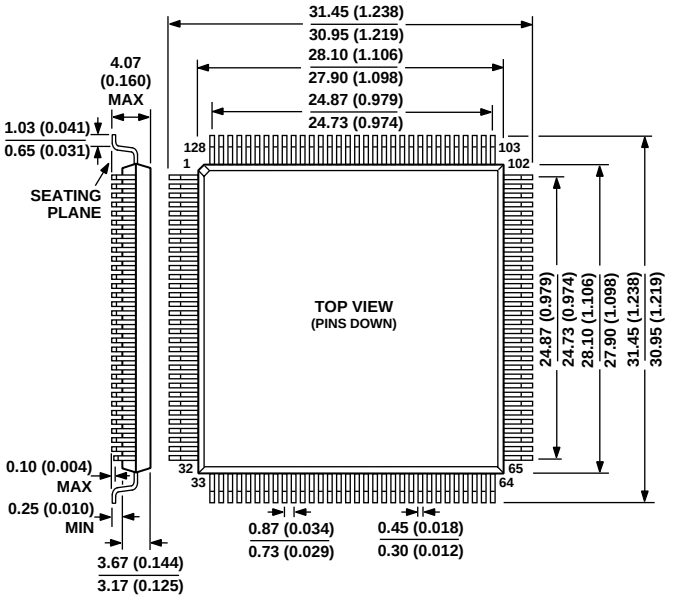
**TQFP Pin Configurations**

| TQFP Number | Pin Name | TQFP Number | Pin Name | TQFP Number | Pin Name | TQFP Number | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | IAL | 33 | A12 | 65 | ECLK | 97 | D19 |
| 2 | PF3 | 34 | A13 | 66 | ELOUT | 98 | D20 |
| 3 | PF2 | 35 | $\overline{\text{IRQE}}$ | 67 | ELIN | 99 | D21 |
| 4 | PF1 | 36 | MMAP | 68 | $\overline{\text{EINT}}$ | 100 | D22 |
| 5 | PF0 | 37 | $\overline{\text{PWD}}$ | 69 | $\overline{\text{EBR}}$ | 101 | D23 |
| 6 | $\overline{\text{WR}}$ | 38 | $\overline{\text{IRQ2}}$ | 70 | $\overline{\text{BR}}$ | 102 | GND |
| 7 | $\overline{\text{RD}}$ | 39 | BMODE | 71 | $\overline{\text{EBG}}$ | 103 | $\overline{\text{IWR}}$ |
| 8 | $\overline{\text{IOMS}}$ | 40 | PWDACK | 72 | $\overline{\text{BG}}$ | 104 | $\overline{\text{IRD}}$ |
| 9 | $\overline{\text{BMS}}$ | 41 | $\overline{\text{IACK}}$ | 73 | VDD | 105 | IAD15 |
| 10 | $\overline{\text{DMS}}$ | 42 | $\overline{\text{BGH}}$ | 74 | D0 | 106 | IAD14 |
| 11 | $\overline{\text{CMS}}$ | 43 | VDD | 75 | D1 | 107 | IAD13 |
| 12 | GND | 44 | GND | 76 | D2 | 108 | IAD12 |
| 13 | VDD | 45 | $\overline{\text{IRQL0}}$ | 77 | D3 | 109 | IAD11 |
| 14 | $\overline{\text{PMS}}$ | 46 | $\overline{\text{IRQL1}}$ | 78 | D4 | 110 | IAD10 |
| 15 | A0 | 47 | FL0 | 79 | GND | 111 | IAD9 |
| 16 | A1 | 48 | FL1 | 80 | D5 | 112 | IAD8 |
| 17 | A2 | 49 | FL2 | 81 | D6 | 113 | IAD7 |
| 18 | A3 | 50 | DT0 | 82 | D7 | 114 | IAD6 |
| 19 | A4 | 51 | TFS0 | 83 | D8 | 115 | VDD |
| 20 | A5 | 52 | RFS0 | 84 | D9 | 116 | GND |
| 21 | A6 | 53 | DR0 | 85 | D10 | 117 | IAD5 |
| 22 | A7 | 54 | SCLK0 | 86 | D11 | 118 | IAD4 |
| 23 | XTAL | 55 | DT1/F0 | 87 | D12 | 119 | IAD3 |
| 24 | CLKIN | 56 | TFS1/$\overline{\text{IRQ1}}$ | 88 | D13 | 120 | IAD2 |
| 25 | GND | 57 | RFS1/$\overline{\text{IRQ0}}$ | 89 | D14 | 121 | IAD1 |
| 26 | CLKOUT | 58 | GND | 90 | GND | 122 | IAD0 |
| 27 | GND | 59 | DR1/FI | 91 | VDD | 123 | PF7 |
| 28 | VDD | 60 | SCLK1 | 92 | GND | 124 | PF6 |
| 29 | A8 | 61 | $\overline{\text{ERESET}}$ | 93 | D15 | 125 | PF5 |
| 30 | A9 | 62 | $\overline{\text{RESET}}$ | 94 | D16 | 126 | PF4 |
| 31 | A10 | 63 | $\overline{\text{EMS}}$ | 95 | D17 | 127 | GND |
| 32 | A11 | 64 | EE | 96 | D18 | 128 | $\overline{\text{IS}}$ |

## OUTLINE DIMENSIONS

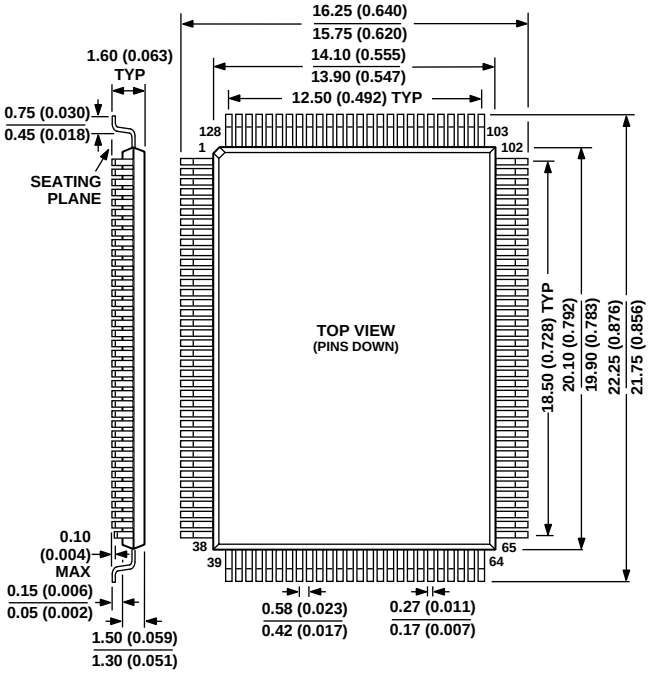
Dimensions shown in mm and (inches).

### 128-Lead Metric Plastic Quad Flatpack (PQFP) (S-128)




NOTE: THE ACTUAL POSITION OF EACH LEAD IS WITHIN .20 (.008) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION. UNLESS OTHERWISE NOTED.

### 128-Lead Metric Thin Plastic Quad Flatpack (TQFP) (ST-128)




NOTE: THE ACTUAL POSITION OF EACH LEAD IS WITHIN .08 (.0032) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION. UNLESS OTHERWISE NOTED.

## ORDERING GUIDE

| Part Number | Ambient Temperature Range | Instruction Rate (MHz) | Package Description | Package Options* |
|---|---|---|---|---|
| ADSP-2181KST-115 | 0°C to +70°C | 28.8 | 128-Lead TQFP | ST-128 |
| ADSP-2181BST-115 | –40°C to +85°C | 28.8 | 128-Lead TQFP | ST-128 |
| ADSP-2181KS-115 | 0°C to +70°C | 28.8 | 128-Lead PQFP | S-128 |
| ADSP-2181BS-115 | –40°C to +85°C | 28.8 | 128-Lead PQFP | S-128 |
| ADSP-2181KST-133 | 0°C to +70°C | 33.3 | 128-Lead TQFP | ST-128 |
| ADSP-2181BST-133 | –40°C to +85°C | 33.3 | 128-Lead TQFP | ST-128 |
| ADSP-2181KS-133 | 0°C to +70°C | 33.3 | 128-Lead PQFP | S-128 |
| ADSP-2181BS-133 | –40°C to +85°C | 33.3 | 128-Lead PQFP | S-128 |
| ADSP-2181KST-160 | 0°C to +70°C | 40 | 128-Lead TQFP | ST-128 |
| ADSP-2181KS-160 | 0°C to +70°C | 40 | 128-Lead PQFP | S-128 |

*S = Plastic Quad Flatpack (PQFP), ST = Plastic Thin Quad Flatpack (TQFP).

C2041c–3–3/98

PRINTED IN U.S.A.