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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	12MHz
Connectivity	SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-LQFP
Supplier Device Package	36-QFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87f2416au-eb-2e

■Ports

- Normal withstand voltage I/O ports
  - Ports I/O direction can be designated in 1 bit units — 16 (P1n, P20, P21, P30, P31, P70 to P73)
  - Ports I/O direction can be designated in 4 bit units — 8 (P0n)
- Dedicated oscillator ports/input ports — 2 (CF1/XT1, CF2/XT2)
- Reset pin — 1 ($\overline{RES}$)
- Power pins — 3 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$)

■Timers

- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + with an 8-bit prescaler 8-bit timer/counter (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes
  3) Base timer does not operate when selecting CF Oscillation circuit.

■High-speed clock counter

1) Capable of counting clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
2) Capable of generating real-time output.

■SIO

- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■UART
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD converter: 12 bits/8 bits × 10 channels
- 12 bits/8 bits AD converter resolution selectable

■PWM: Multifrequency 12-bit PWM × 2 channels

■Remote control receiver circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Clock output function
- Capable of outputting selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as system clock.
- Capable of outputting oscillation clock of sub clock.

■Watchdog timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Interrupts
- 20 sources, 10 vector addresses
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/PWM4, PWM5
10	0004BH	H or L	Port 0

• Priority levels X > H > L
• Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine stack levels: 256levels (the stack is allocated in RAM.)

■High-speed multiplication/division instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation circuits
- RC oscillation circuit (internal) : For system clock
- Frequency variable RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock, with internal Rf

1) CF and crystal oscillation circuit have a shared terminal, and it is software selectable.
2) When reset, CF and Crystal oscillators stop operation. After reset is released, CF oscillator starts operation.

■System clock divider function
- Capable of running with low current consumption.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Internal reset function
- Power-On-Reset (POR) function

1) POR resets the system when the power supply voltage is applied.
2) POR release level is selectable from 5 levels (1.55V, 1.72V, 2.00V, 2.37V, 2.65V) by option.

- Low Voltage Detection reset (LVD) function

1) LVD used with POR resets the system when the supply voltage is applied and when it is lowered.
2) LVD function is selectable from enable/disable and the reset level is selectable from 3 levels (1.90V, 2.25V, 2.50V) by option.

■Standby function
- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.

1) Oscillation is not halted automatically.
2) Canceled by a system reset or occurrence of an interrupt

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.

1) The CF, RC, and crystal oscillators automatically stop operation.
2) There are three ways of resetting the HOLD mode.
   (1) Setting the reset pin to the lower level.
   (2) Setting at least one of the INT0, INT1, INT2, and INT4 pins to the specified level
   (3) Having an interrupt source established at port 0

- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.

1) The CF and RC oscillators automatically stop operation.
2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
3) There are four ways of resetting the X'tal HOLD mode.
   (1) Setting the reset pin to the low level
   (2) Setting at least one of the INT0, INT1, INT2, and INT4 pins to the specified level
   (3) Having an interrupt source established at port
   (4) Having an interrupt source established in the base timer circuit

Note: X'tal HOLD mode can be used only when crystal oscillation is selected.

■Onchip-Debugger
- Supports software debugging with the IC mounted on the target board.
- For a small pin package, two-channel Onchip-Debugger port ((DBGP0(P0), DBGP1(P1)) are equipped.

■Flash data security
- Protects from illegal access to data in flash memory.
  Note: Flash data security cannot guarantee perfect security.

■Package form
- QFP36 (7 × 7): Lead-free type

■Development tools
- Onchip Debugger : TCB87 TypeB + LC87F2416A

■Flash ROM programming boards

Package	Programming boards
QFP36 (7×7)	W87F24Q

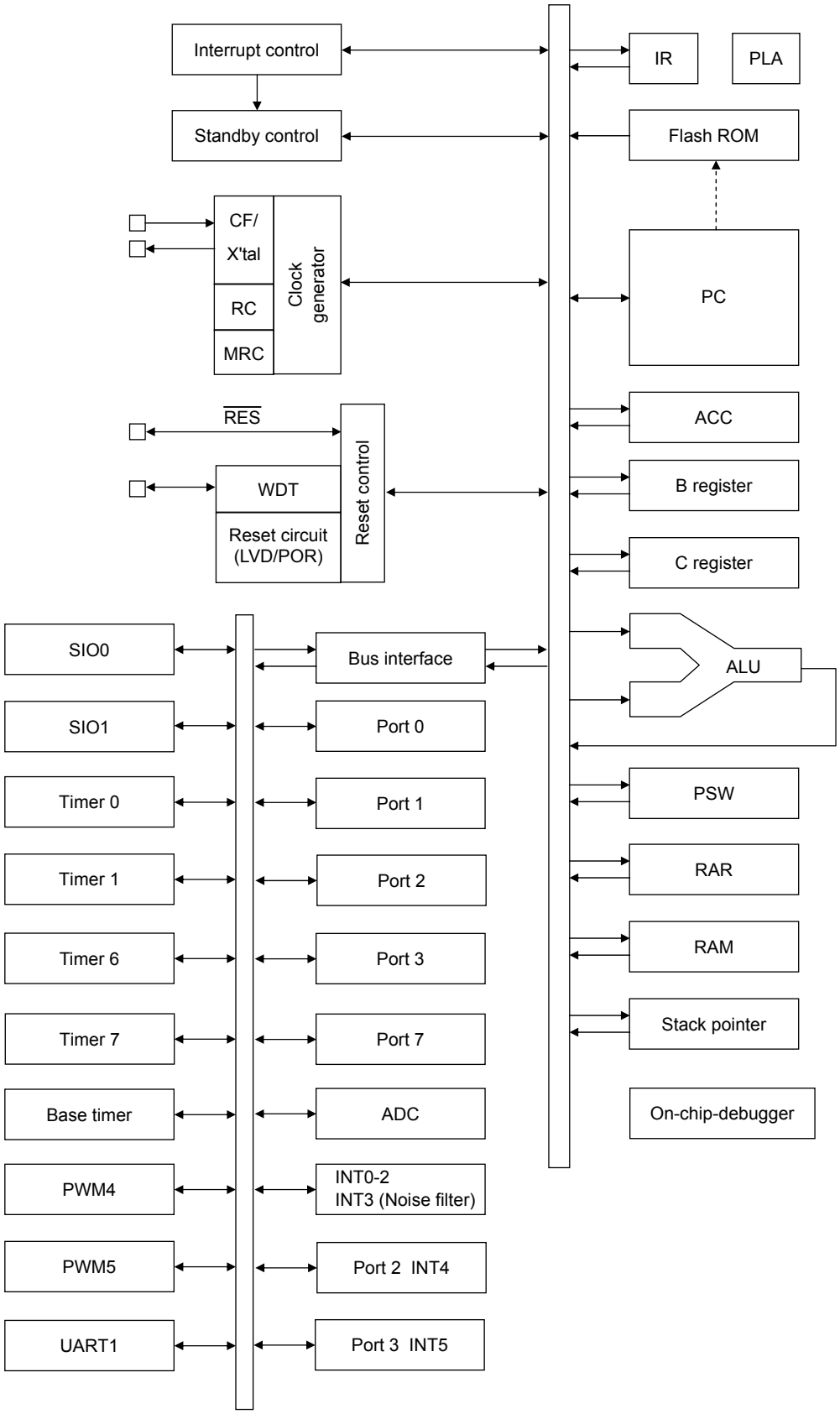
■Flash ROM programmer

Maker	Model		Supported version (Note)	Device
Flash Support Group, Inc.	Single	AF9708/AF9709/AF9709B (including product of Ando Electric Co.,Ltd)	Revision : After 02.60	LC87F2416A
	Gang	AF9723 (Main body) (including product of Ando Electric Co.,Ltd)		
		AF9833 (Unit) (including product of Ando Electric Co.,Ltd)		
Our Company	SKK Type-B(SANYOFWS)		Application Version : 1.03 or later Chip Data Version : 2.03 or later	LC87F2416A

For information about AF series, please contact the following:
Flash Support Group, Inc.
TEL: 053-459-1030
E-mail: sales@j-fsg.co.jp

■Same package and pin assignment as mask ROM version.
1) LC872400 series options can be set by using flash ROM data. Thus the board used for mass production can be used for debugging and evaluation without modifications.
2) If the program for the mask ROM version is used, the usable ROM/RAM capacity is the same as the mask ROM version.

System Block Diagram



Pin Function Chart

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$</td><td>-</td><td>-power supply pins</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4 bit units
• Pull-up resistors can be turned on and off in 4 bit units.
• HOLD reset input
• Port 0 interrupt input
• Pin functions
P05: System clock output
P06: Timer 6 toggle output
P07: Timer 7 toggle output
P00 (AN0) to P07 (AN7): AD converter input
P05 (DBGP00) to P07 (DBGP02): On-chip-debugger 0 port</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1PWML output
P17: Timer 1PWMH output/beeper output
P15 (DBGP10) to P13 (DBGP12): On-chip-debugger 1 port</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P21</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P20: UART transmit
P21: UART receive
P20 to P21: INT4 input/HOLD reset input/timer 1 event input
/timer 0L capture input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P31</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1 bit units
• Pull-up resistors can be turned on and off in 1 bit units.
• Pin functions
P30:PWM4 output
P31:PWM5 output
P30 to P31: INT5 input/HOLD reset input/timer 1 event input
/timer 0L capture input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT5</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
</table>

Continued on next page.

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P21	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P31	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable

Note1: Programmable pull-up resistors and selection of low-impedance-pull-up/high-impedance-pull-up for port 0 are controlled on lower four bits and upper four bits (P00 to P03, P04 to P07).

Note: $V_{SS}1$ and $V_{SS}2$ should connect to each other and they should also be grounded.

Onchip Debugger pin connection requirements

Refer to the separate documents, "RD87 Onchip Debugger Installation Manual" and "LC87200series pin connection requirements Manual", for the requirements on Onchip Debugger pin connections.

2. Allowable Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	max.	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1$	0.245µs ≤ tCYC ≤ 200µs		2.7		5.5	V
	$V_{DD}(2)$		0.294µs ≤ tCYC ≤ 200µs		2.2		5.5	
	$V_{DD}(3)$		0.735µs ≤ tCYC ≤ 200µs		1.8		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.		1.6			
High level input voltage	$V_{IH}(1)$	Ports 1, 2, 3 P71 to P73 P70 port input /interrupt side		1.8 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Ports 0		1.8 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 70 watchdog timer side		1.8 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	CF1, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3 P71 to P73 P70 port input /interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
				1.8 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		1.8 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(4)$	CF1, $\overline{RES}$		1.8 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	µs
				2.2 to 5.5	0.294		200	
				1.8 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio = 1/1 • External system clock duty = 50±5%	2.7 to 5.5	0.1		12	MHz
				1.8 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio = 1/2 • External system clock duty = 50±5%	3.0 to 5.5	0.2		24.4	
				2.0 to 5.5	0.1		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	2.7 to 5.5		12		
	FmCF(2)	CF1, CF2	10MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		10		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	1.8 to 5.5		4		
	FmRC		Internal RC oscillation	1.8 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation source oscillation	2.7 to 5.5		16		
	FsX'tal(1)	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	1.8 to 5.5		32.768		kHz

Note 2-1: V_{DD} must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Serial I/O Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

4-1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min.	typ.	max.	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 5. (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2			
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 5.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode (Note 4-1-3)	1.8 to 5.5			(1/3)tCYC +0.08	
			tdD0(2)		• Synchronous 8-bit mode (Note 4-1-3)				1tCYC +0.08	
	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.08	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 5.

4-2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min.	typ.	max.	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	• See Fig. 5.	1.8 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 5.	1.8 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 5.	1.8 to 5.5	0.05			µs
	Data hold time		thDI(2)				0.05			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5.	1.8 to 5.5			(1/3)tCYC +0.08	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

5. Pulse Input Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P21), INT5(P30 to P31)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	1.8 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	256			
	tPIL(5)	$\overline{RES}$	• External reset input mode. • Resetting is enabled.	1.8 to 5.5	200			μs

7. Power-on reset (POR) Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
POR release voltage	PORR		• Select from option. (Note 7-1)	1.55V	1.38	1.55	1.72	V
				1.72V	1.54	1.72	1.90	
				2.00V	1.81	2.00	2.19	
				2.37V	2.12	2.37	2.62	
				2.65V	2.39	2.65	2.91	
Detection voltage unknown state	POUKS		• See Fig. 7. (Note 7-2)			0.7	0.95	
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.4V.				100	ms

Note 7-1: The POR release level can be selected out of 5 levels only when the LVD reset function is disabled.
Note 7-2: POR is in an unknown state before transistors start operation.

8. Low voltage detection reset (LVD) Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	Specification min.	typ.	max.	unit
LVD reset Voltage • See Fig. 8. (Note 8-2)	LVDET		• Select from option. (Note 8-1) (Note 8-3)	1.90V	1.72	1.90	2.08	V
				2.25V	2.03	2.25	2.47	
				2.50V	2.26	2.50	2.74	
LVD hysteresys width	LVHYS			1.90V		LVDET ×0.054		
				2.25V		LVDET ×0.062		
				2.50V		LVDET ×0.065		
Detection voltage unknown state	LVUKS		• See Fig. 8. (Note 8-4)			0.7	0.95	
Low voltage detection minimum Width (Reply sensitivity)	TLVDW		• See Fig. 9.		0.2			ms

Note 8-1: The LVD reset level can be selected out of 3 levels only when the LVD reset function is enabled.
Note 8-2: LVD reset voltage specification values do not include hysteresis voltage.
Note 8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.
Note 8-4: LVD is in an unknown state before transistors start operation.

9. Consumption Current Characteristics at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	Max.	unit
Normal mode consumption current (Note 9-1) (Note 9-2)	IDDOP(1)	$V_{DD}1$	• FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		8.3	15.1	mA
				2.7 to 3.6		4.8	8.7	
	IDDOP(2)		• CF1=24MHz external clock • System clock set to CF1 side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		9	16.2	
				3.0 to 3.6		5.2	8.7	
	IDDOP(3)		• FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		7.3	13.8	
				2.2 to 3.6		4.3	8.3	
	IDDOP(4)		• FmCF=4 MHz ceramic oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		3.6	7.8	
				1.8 to 3.6		2.5	4.9	
	IDDOP(5)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.7	2.4	
				1.8 to 3.6		0.4	1.2	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 1MHz with Frequency variable RC oscillation • 1/2 frequency division ratio	1.8 to 5.5		1.3	2.8	
				1.8 to 3.6		0.8	1.6	
	IDDOP(7)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		39	139	μA
				1.8 to 3.6		17	66	
	IDDOP(8)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		39	101	
				3.3		17	47	
				2.5		10	29	

Note 9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/remarks	Conditions	V_{DD}[V]	Specification min.	typ.	max.	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(1)	V_{DD}1	• HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.7 to 5.5		3.4	6.2	mA
				2.7 to 3.6		1.8	3.1	
	IDDHALT(2)		• HALT mode • CF1=24MHz external clock • System clock set to CF1 side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	3.0 to 5.5		4.9	8.6	
				3.0 to 3.6		2.3	3.8	
	IDDHALT(3)		• HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	2.2 to 5.5		2.9	5.6	
				2.2 to 3.6		1.5	2.8	
	IDDHALT(4)		• HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	1.8 to 5.5		1.5	3.7	
				1.8 to 3.6		0.7	1.6	
	IDDHALT(5)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		0.5	1.4	
				1.8 to 3.6		0.2	0.6	
	IDDHALT(6)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 1MHz with Frequency variable RC oscillation • 1/2 frequency division ratio	1.8 to 5.5		T.B.D	T.B.D	
				1.8 to 3.6		T.B.D	T.B.D	
	IDDHALT(7)		• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	1.8 to 5.5		25	112	µA
				1.8 to 3.6		8.5	56	

Note 9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2: The consumption current values do not include operational current of LVD function if not specified.

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Parameter	Symbol	Pin/remarks	Conditions	V_{DD}[V]	Specification min.	typ.	max.	unit
HALT mode consumption current (Note 9-1) (Note 9-2)	IDDHALT(8)	V_{DD}1	• HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio • Ta=-10 to +50°C	5.0		25	69	μA
				3.3		8.5	29	
				2.5		4.2	15	
HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(1)		HOLD mode • CF1=V_{DD} or open (External clock mode)	1.8 to 5.5		0.04	30	
				1.8 to 3.6		0.02	21	
	IDDHOLD(2)		HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to 50°C	5.0		0.04	2.3	
				3.3		0.02	1.5	
				2.5		0.017	1.2	
	IDDHOLD(3)		HOLD mode • CF1=V_{DD} or open (External clock mode) • LVD option selected	1.8 to 5.5		2.2	34	
				1.8 to 3.6		1.7	24	
	IDDHOLD(4)		HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to 50°C • LVD option selected	5.0		2.2	5.4	
				3.3		1.7	3.8	
				2.5		1.5	3.3	
Timer HOLD mode consumption current (Note 9-1) (Note 9-2)	IDDHOLD(5)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	1.8 to 5.5		22	106	
				1.8 to 3.6		7.5	45	
	IDDHOLD(6)		Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode • Ta=-10 to 50°C	5.0		22	62	
				3.3		7.5	23	
				2.5		2.9	12	

Note 9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note 9-2: The consumption current values do not include operational current of LVD function if not specified.

10. F-ROM Programming Characteristics at Ta = +10 to +55°C, $V_{SS}1 = V_{SS}2 = 0V$

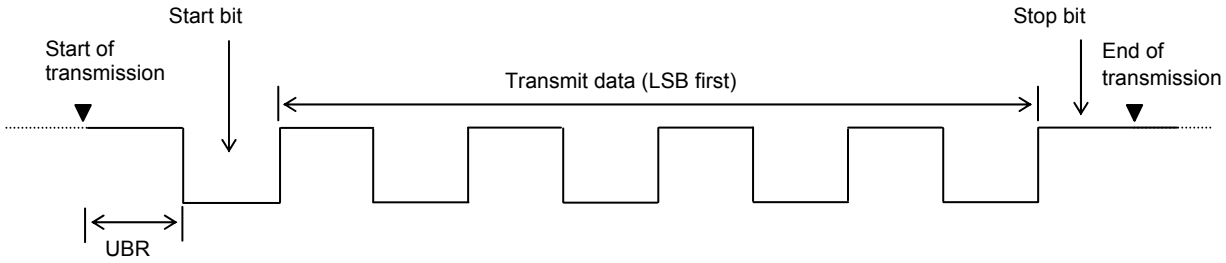
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	max.	unit
Onboard programming current	IDDFW	$V_{DD}1$	• Only current of the Flash block.	2.2 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5		20	30	ms
	tFW(2)		• Programming time			40	60	µs

11. UART (Full Duplex) Operating Conditions at Ta = -40 to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

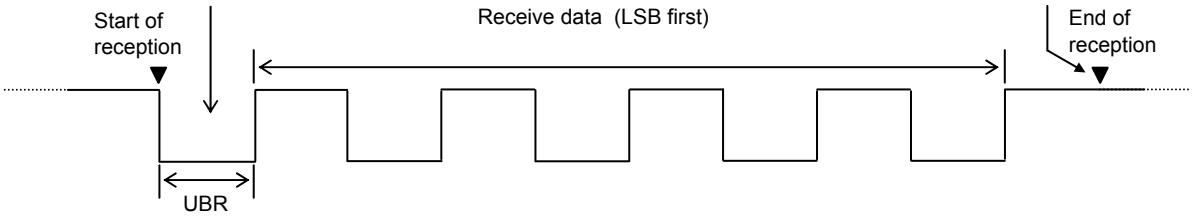
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min.	typ.	max.	unit
Transfer rate	UBR	P20, P21		1.8 to 5.5	16/3		8192/3	tCYC

Data length : 7/8/9 bits (LSB first)
Stop bits : 1 bit(2-bit in continuous data transmission)
Parity bits : None

Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using our company-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [ms]	Max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	2.7 to 3.6	0.1	0.5	Internal C1, C2
			(10)	(10)	Open	680	3.6 to 5.5	0.1	0.5	
10MHz		CSTCE10M0G52-R0	(10)	(10)	Open	680	2.2 to 3.6	0.1	0.5	
			(10)	(10)	Open	1.0k	3.6 to 5.5	0.1	0.5	
		CSTLS10M0G53-B0	(15)	(15)	Open	680	2.2 to 3.6	0.1	0.5	
			(15)	(15)	Open	680	3.6 to 5.5	0.1	0.5	
4MHz		CSTCR4M00G53-R0	(15)	(15)	Open	2.2k	1.8 to 2.7	0.2	0.6	
			(15)	(15)	Open	3.3k	2.7 to 5.5	0.2	0.6	
		CSTLS4M00G53-B0	(15)	(15)	Open	2.2k	1.8 to 2.7	0.2	0.6	
			(15)	(15)	Open	3.3k	2.7 to 5.5	0.2	0.6	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using our company-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		Typ [s]	Max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	Open	330k	1.8 to 5.5	1.4	4.0	Applicable CL value = 7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

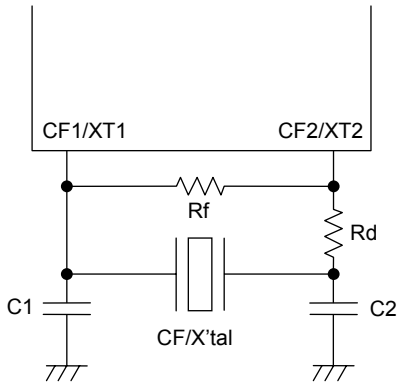


Figure 1 CF and XT Oscillator Circuit

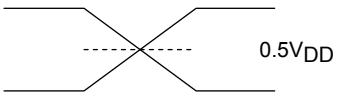
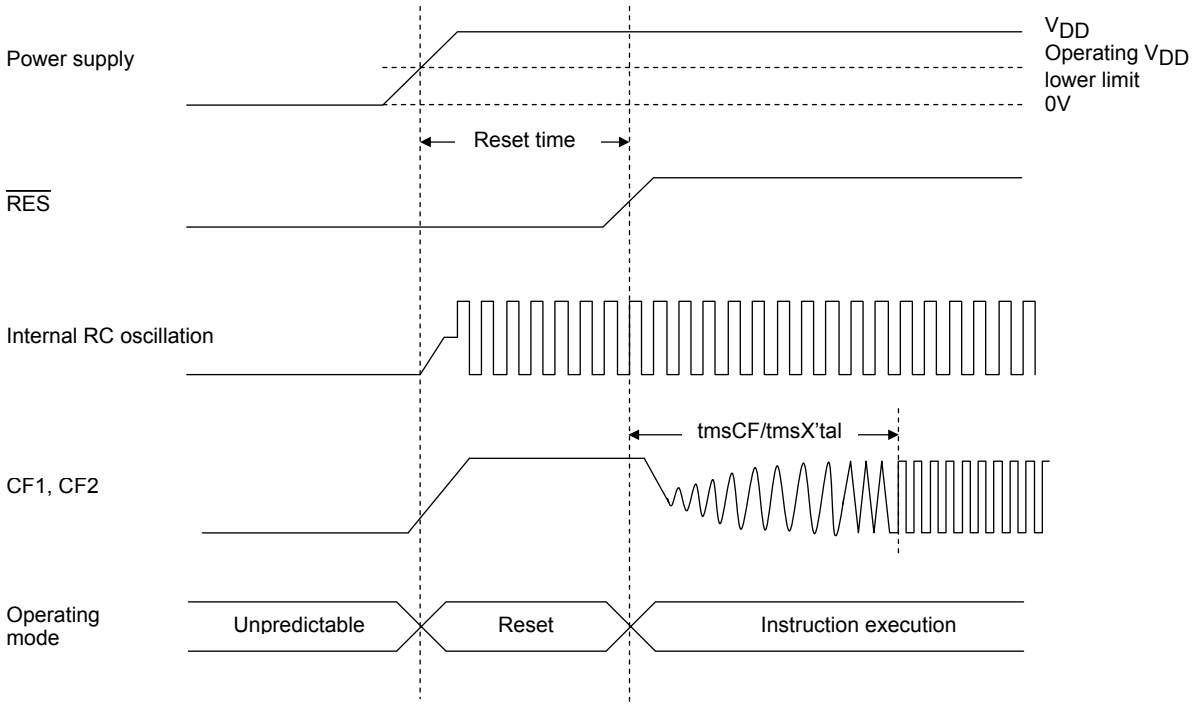
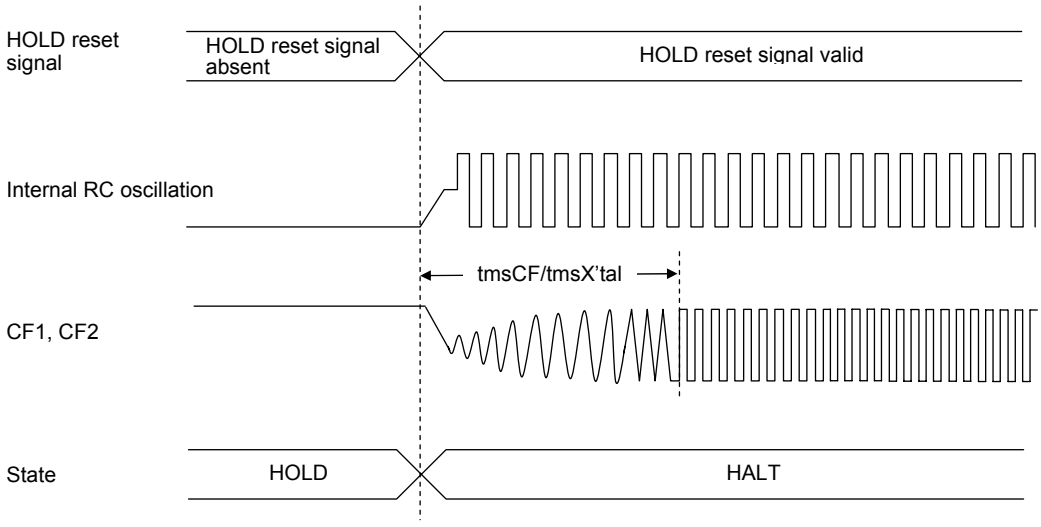


Figure 2 AC Timing Measurement Point

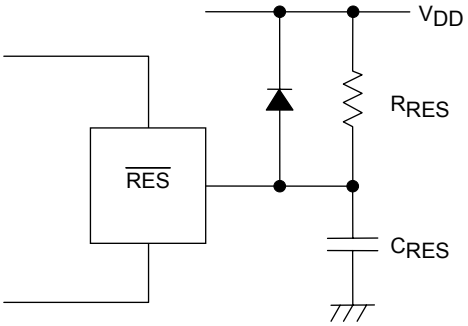


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 3 Oscillation Stabilization Times



Note: External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information.

Figure 4 Reset Circuit

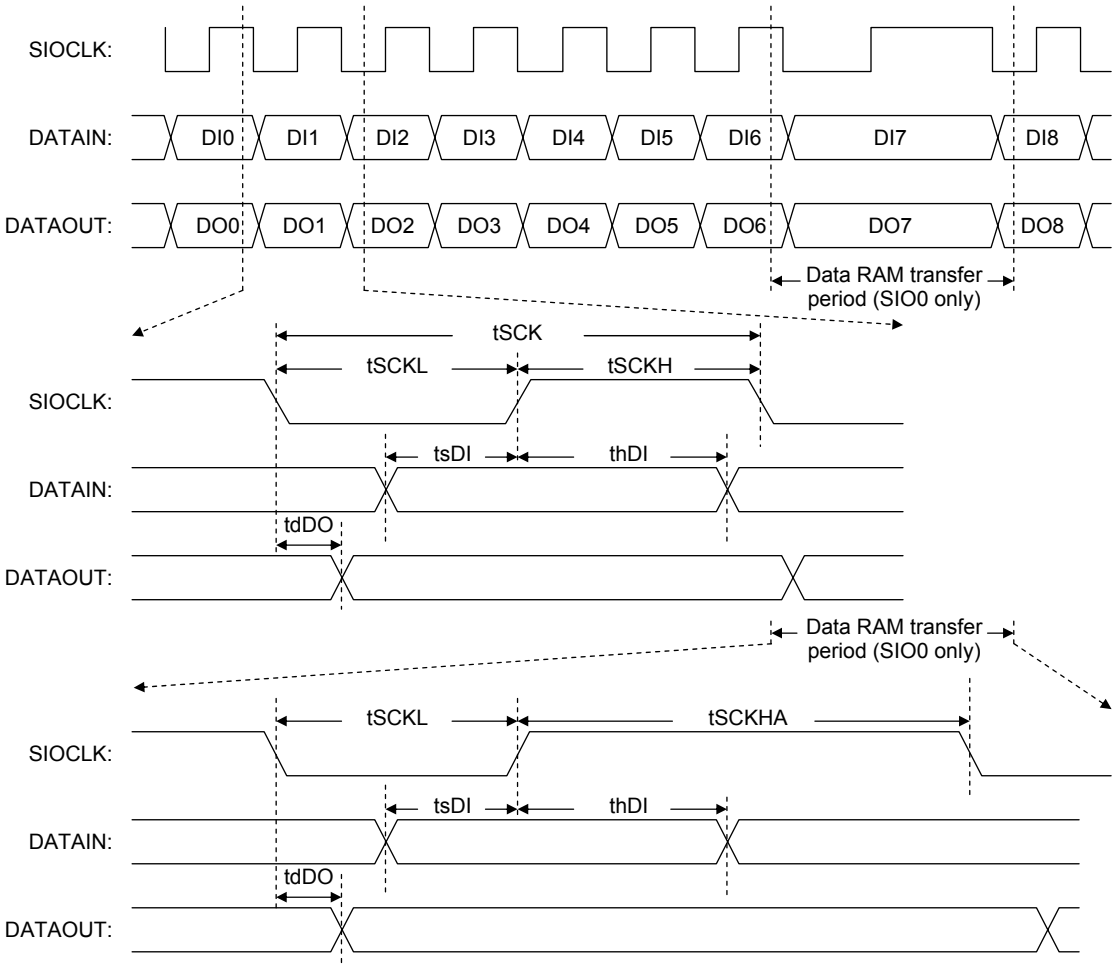


Figure 5 Serial I/O Output Waveforms

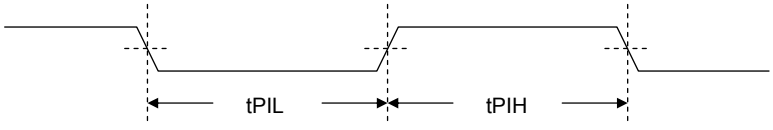


Figure 6 Pulse Input Timing Signal Waveform

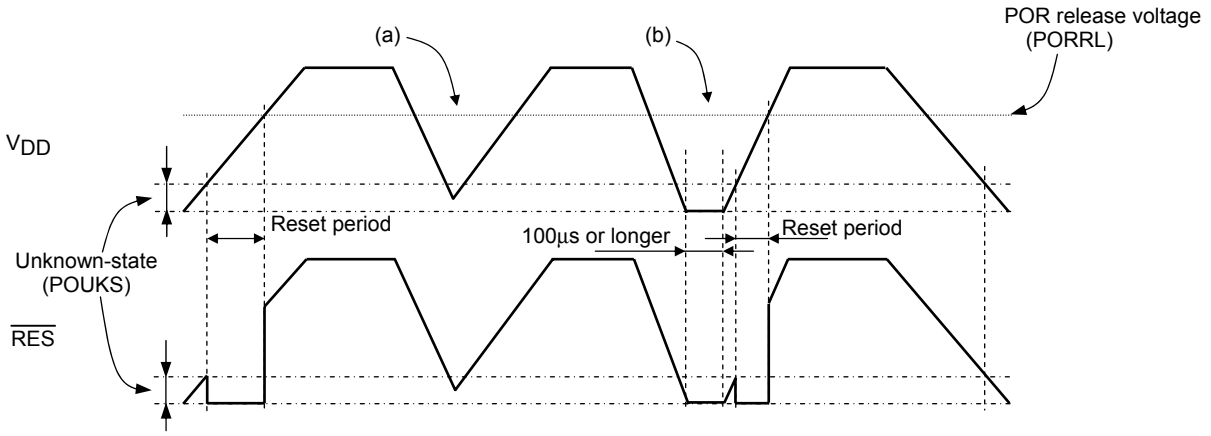


Figure 7 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor R_{RES} only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

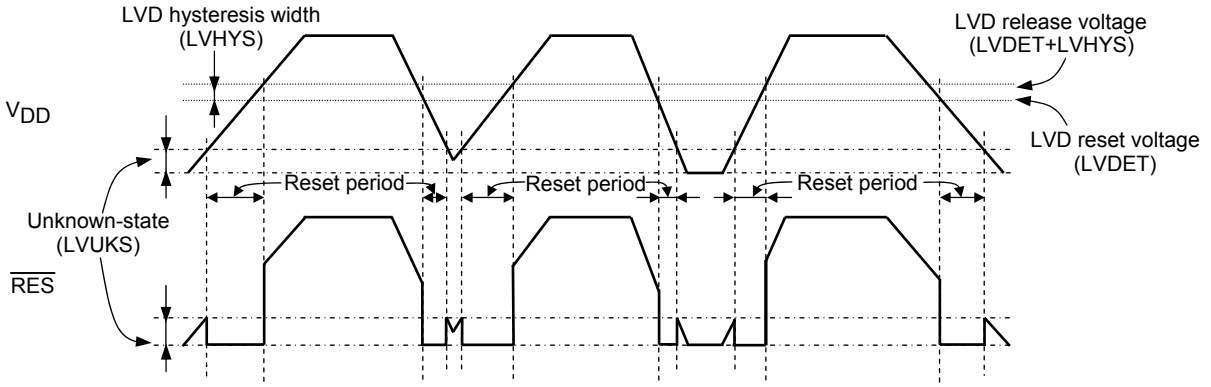


Figure 8 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor R_{RES} only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.