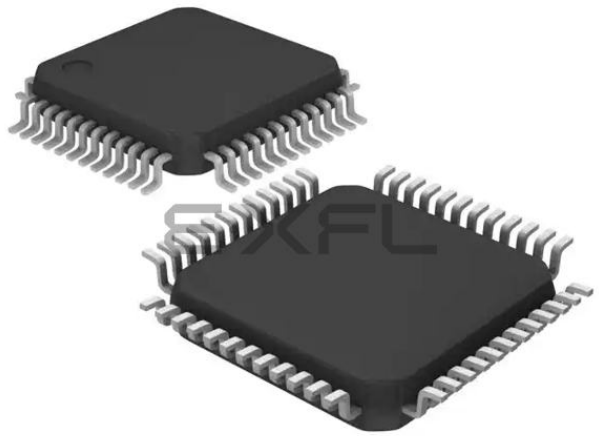

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0519ld3ae

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface

4.2 Pin Configuration

4.2.1 LQFP 100-pin

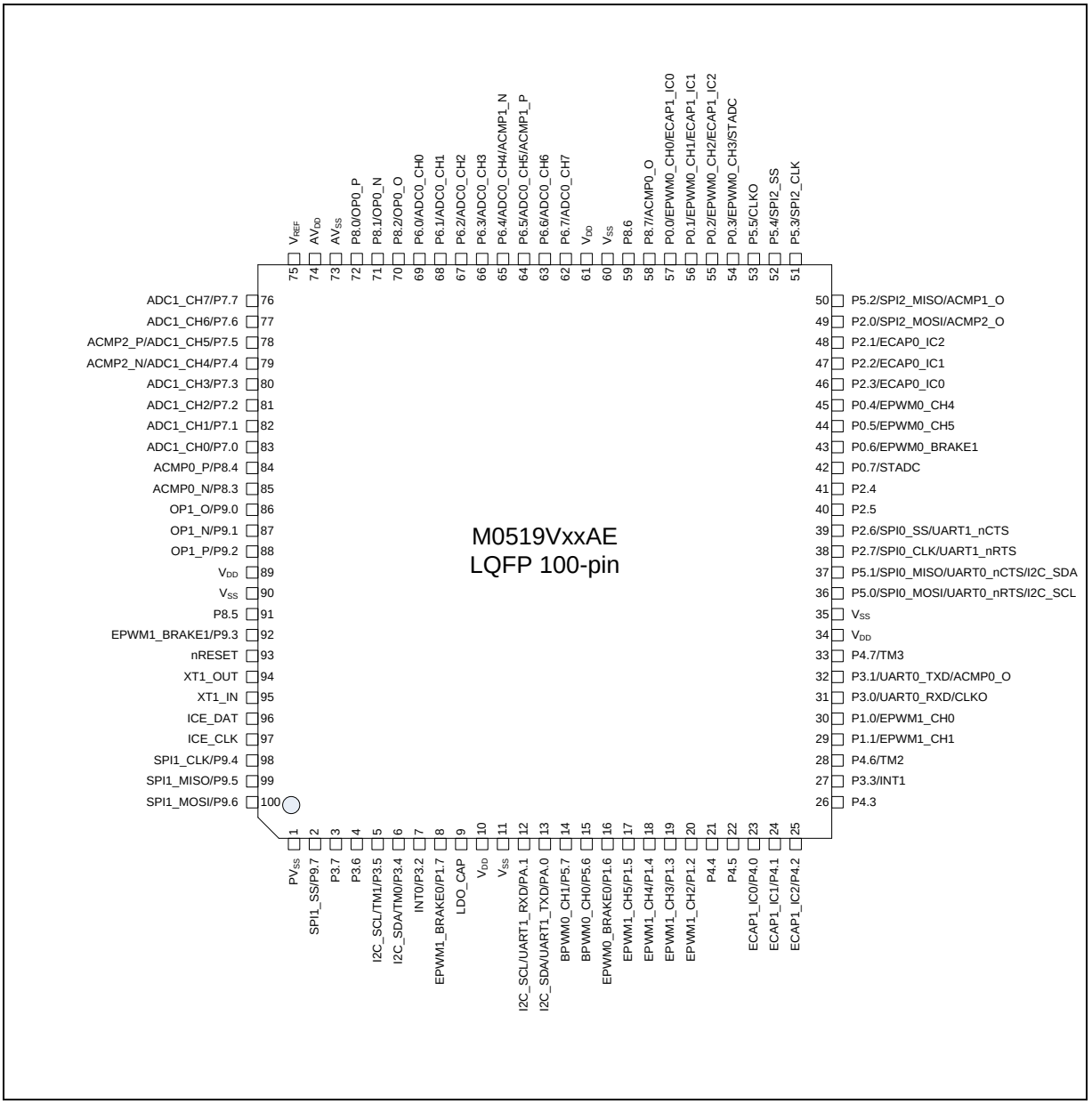


Figure 4-2 NuMicro® M0519VxxAE Series LQFP-100 Pin Diagram

4.2.2 LQFP 64-pin

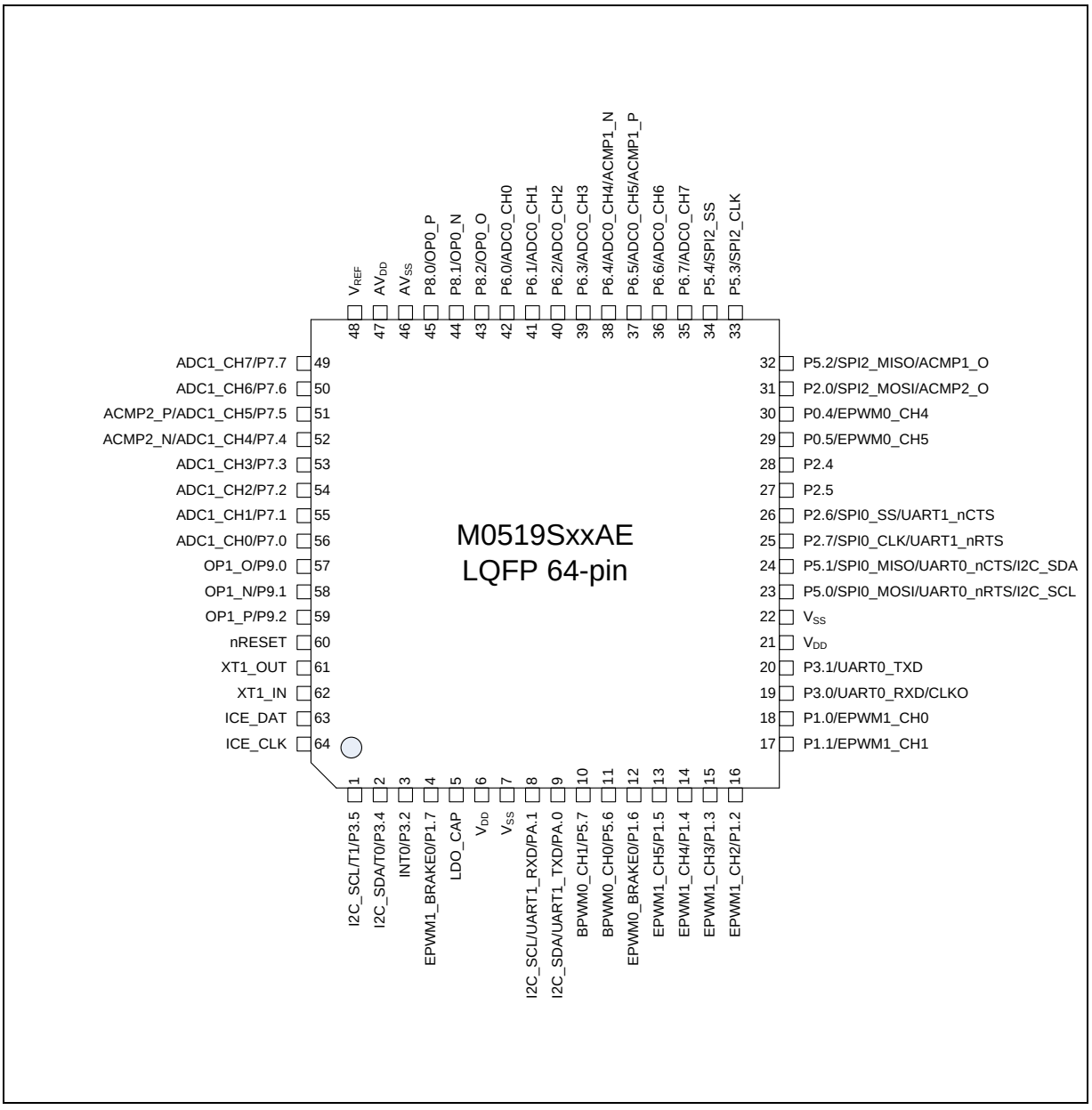


Figure 4-3 NuMicro® M0519SxxAE Series LQFP-64 Pin Diagram

4.2.3 LQFP 48-pin

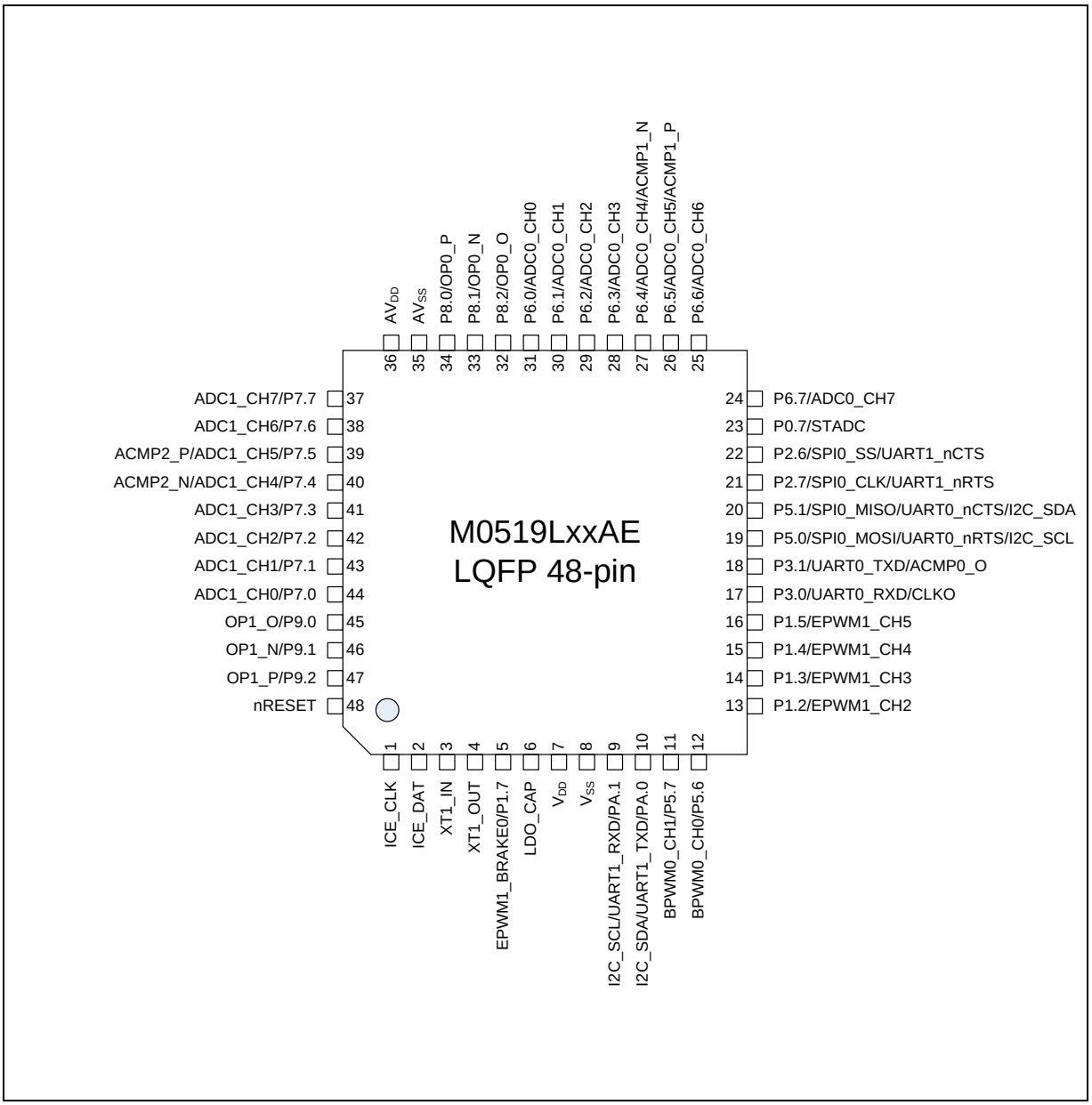


Figure 4-4 NuMicro® M0519LxxAE Series LQFP-48 Pin Diagram

4.3 Pin Description

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
10	6	7	V_{DD}	**P**	**POWER SUPPLY:** Supply voltage **Digital** V_{DD} for operation.
34					
61	21				
89					
11	7	8	V_{SS}	**P**	**GROUND:** Digital Ground potential.
35					
60	22				
90					
9	5	6	LDO_CAP	**P**	**LDO:** LDO output pin **Note: It needs to be connected with a 1uF capacitor.**
1	-	-	PV_{SS}	**P**	**PLL GROUND: PLL** Ground potential.
74	47	36	AV_{DD}	**AP**	Power supply for internal analog circuit
73	46	35	AV_{SS}	**AP**	Ground Pin for analog circuit
75	48	-	V_{REF}	**AP**	Voltage reference input for ADC **Note: It needs to be connected with a 1uF capacitor.**
93	60	48	nRESET	**I (ST)**	**RESET:** nRESET pin is a Schmitt trigger input pin for hardware device reset. A "**Low"** on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
94	61	4	XT1_OUT	**O**	**CRYSTAL OUT:** This is the output pin from the internal inverting amplifier. It emits the inverted signal of XT1_IN.
95	62	3	XT1_IN	**I (ST)**	**CRYSTAL IN:** This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
96	63	2	ICE_DAT	**I/O**	Serial Wired Debugger Data pin
97	64	1	ICE_CLK	**I**	Serial Wired Debugger Clock pin
57	-	-	P0.0	**I/O**	General purpose digital I/O pin
			PWM0_CH0	**O**	PWM0 output of PWM Unit 0
			ECAP1_IC0	**I**	Input 0 of Enhanced Input Capture Unit 1
56	-	-	P0.1	**I/O**	General purpose digital I/O pin
			PWM0_CH1	**O**	PWM1 output of PWM Unit 0
			ECAP1_IC1	**I**	Input 1 of Enhanced Input Capture Unit 1
55	-	-	P0.2	**I/O**	General purpose digital I/O pin
			PWM0_CH2	**O**	PWM2 output of PWM Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
54	-	-	P0.3	I/O	General purpose digital I/O pin
			PWM0_CH3	O	PWM3 output of PWM Unit 0
			STADC	I	ADC external trigger input
45	30	-	P0.4	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM Unit 0
44	29	-	P0.5	I/O	General purpose digital I/O pin
			PWM0_CH5	O	PWM5 output of PWM Unit 0
43	-	-	P0.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE1	I	Brake input pin 1 of PWM Unit 0
42	-	23	P0.7	I/O	General purpose digital I/O pin
			STADC	I	ADC external trigger input
30	18	-	P1.0	I/O	General purpose digital I/O pin
			PWM1_CH0	O	PWM0 output of PWM Unit 1
29	17	-	P1.1	I/O	General purpose digital I/O pin
			PWM1_CH1	O	PWM1 output of PWM Unit 1
20	16	13	P1.2	I/O	General purpose digital I/O pin
			PWM1_CH2	O	PWM2 output of PWM Unit 1
19	15	14	P1.3	I/O	General purpose digital I/O pin
			PWM1_CH3	O	PWM3 output of PWM Unit 1
18	14	15	P1.4	I/O	General purpose digital I/O pin
			PWM1_CH4	O	PWM4 output of PWM Unit 1
17	13	16	P1.5	I/O	General purpose digital I/O pin
			PWM1_CH5	O	PWM5 output of PWM Unit 1
16	12	-	P1.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE0	I	Brake input pin 0 of PWM Unit 0
8	4	5	P1.7	I/O	General purpose digital I/O pin
			PWM1_BRAKE0	I	Brake input pin0 of PWM Unit 1
49	31	-	P2.0	I/O	General purpose digital I/O pin
			SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin
			ACMP2_O	AO	Analog comparator 2 output pin
48	-	-	P2.1	I/O	General purpose digital I/O pin
			ECAP0_IC2	I	Input 2 of Enhanced Input Capture Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
25	-	-	P4.2	I/O	General purpose digital I/O pin
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
26	-	-	P4.3	I/O	General purpose digital I/O pin
21	-	-	P4.4	I/O	General purpose digital I/O pin
22	-	-	P4.5	I/O	General purpose digital I/O pin
28	-	-	P4.6	I/O	General purpose digital I/O pin
			TM2	I/O	Timer2 external clock
33	-	-	P4.7	I/O	General purpose digital I/O pin
			TM3	I/O	Timer3 external clock
36	23	19	P5.0	I/O	General purpose digital I/O pin
			SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin
			UART0_nRTS	O	UART0 RTS pin
37	24	20	P5.1	I/O	General purpose digital I/O pin
			SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin
			UART0_nCTS	I	UART0 CTS pin
50	32	-	P5.2	I/O	General purpose digital I/O pin
			SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin
			ACMP1_O	AO	Analog comparator 1 output pin
51	33	-	P5.3	I/O	General purpose digital I/O pin
			SPI2_CLK	I/O	SPI2 serial clock pin
52	34	-	P5.4	I/O	General purpose digital I/O pin
			SPI2_SS	I/O	SPI2 slave select pin
53	-	-	P5.5	I/O	General purpose digital I/O pin
			CLKO	O	Frequency Divider output pin
15	11	12	P5.6	I/O	General purpose digital I/O pin
			PWM2_CH0	I/O	PWM0 output of PWM unit 2
14	10	11	P5.7	I/O	General purpose digital I/O pin
			PWM2_CH1	I/O	PWM1 output of PWM unit 2
69	42	31	P6.0	I/O	General purpose digital I/O pin
			ADC0_CH0	AI	ADC analog input 0 for sample-and-hold A
68	41	30	P6.1	I/O	General purpose digital I/O pin
			ADC0_CH1	AI	ADC analog input 1 for sample-and-hold A
67	40	29	P6.2	I/O	General purpose digital I/O pin

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ADC0_CH2	AI	ADC analog input 2 for sample-and-hold A
66	39	28	P6.3	I/O	General purpose digital I/O pin
			ADC0_CH3	AI	ADC analog input 3 for sample-and-hold A
65	38	27	P6.4	I/O	General purpose digital I/O pin
			ADC0_CH4	AI	ADC analog input 4 for sample-and-hold A
			ACMP1_N	AI	Analog comparator 1 negative input
64	37	26	P6.5	I/O	General purpose digital I/O pin
			ADC0_CH5	AI	ADC analog input 5 for sample-and-hold A
			ACMP1_P	AI	Analog comparator 1 positive input
63	36	25	P6.6	I/O	General purpose digital I/O pin
			ADC0_CH6	AI	ADC analog input 6 for sample-and-hold A
62	35	24	P6.7	I/O	General purpose digital I/O pin
			ADC0_CH7	AI	ADC analog input 7 for sample-and-hold A
83	56	44	P7.0	I/O	General purpose digital I/O pin
			ADC1_CH0	AI	ADC analog input 0 for sample-and-hold B
82	55	43	P7.1	I/O	General purpose digital I/O pin
			ADC1_CH1	AI	ADC analog input 1 for sample-and-hold B
81	54	42	P7.2	I/O	General purpose digital I/O pin
			ADC1_CH2	AI	ADC analog input 2 for sample-and-hold B
80	53	41	P7.3	I/O	General purpose digital I/O pin
			ADC1_CH3	AI	ADC analog input 3 for sample-and-hold B
79	52	40	P7.4	I/O	General purpose digital I/O pin
			ADC1_CH4	AI	ADC analog input 4 for sample-and-hold B
			ACMP2_N	AI	Analog comparator 2 negative input
78	51	39	P7.5	I/O	General purpose digital I/O pin
			ADC1_CH5	AI	ADC analog input 5 for sample-and-hold B
			ACMP2_P	AI	Analog comparator 2 positive input
77	50	38	P7.6	I/O	General purpose digital I/O pin
			ADC1_CH6	AI	ADC analog input 6 for sample-and-hold B
76	49	37	P7.7	I/O	General purpose digital I/O pin
			ADC1_CH7	AI	ADC analog input 7 for sample-and-hold B
72	45	34	P8.0	I/O	General purpose digital I/O pin
			OP0_P	AI	OP Amplifier 0 positive input

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			I2C0_SCL	**I/O**	I2C0 clock output pin

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

Address Space	Token	Controllers
0x401B_0000 – 0x401B_3FFF	ECAP0_BA	Enhanced Input Capture 0 Control Registers
0x401B_4000 – 0x401B_7FFF	ECAP1_BA	Enhanced Input Capture 1 Control Registers
Reserved	Reserved	Reserved
Reserved	Reserved	Reserved
Reserved	Reserved	Reserved
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E01F	SYST_BA	System Timer Control Registers
0xE000_E100 – 0xE000_E4EF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED3F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® M0519 Series is equipped with 128/64 KB on-chip embedded flash for application program memory (APROM) and data flash, and with 8K bytes for ISP loader program memory (LDROM) that could be programmed boot loader to update APROM and data flash through In System Programming (ISP) procedure. ISP function enables user to update embedded flash when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select CBS (Config0[7:6]). By the way, the NuMicro® M0519 Series also provides data flash for user to store some application dependent data before chip power off. For 128 KB APROM device, the data flash is shared with original 128 KB program memory and its start address is configurable in Config1. For 64 KB APROM device, the data flash is fixed at 4K bytes.

6.4.2 Features

- Runs up to 72 MHz and optional up to 50 MHz with zero wait state for continuous address read access
- Supports 512 bytes page erase for all embedded flash
- Supports 128/64 Kbytes application program ROM (APROM)
- Supports 8 KB loader ROM (LDROM)
- Supports 4KB data flash for 64 Kbytes APROM device
- Supports configurable data flash size for 128KB APROM device
- Supports 8 bytes User Configuration block to control system initiation
- Support In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory

6.8 Enhanced PWM Generator (EPWM)

6.8.1 Overview

This device has two built-in PWM units with the same architecture whose function is specially designed for driving motor control applications.

6.8.2 Features

Each unit supports the features below:

- Three independent 16-bit PWM duty control units with maximum 6 port pins:
  - 3 independent PWM output:
    EPWM0_CH0, EPWM0_CH2 and EPWM0_CH4 for Unit 0
    EPWM1_CH0, EPWM1_CH2 and EPWM1_CH4 for Unit 1
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-time insertion:
    (EPWMx_CH0, EPWMx_CH1), (PWMx_CH2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1.
  - 3 synchronous PWM pairs, with each pin in a pair in-phase:
    (EPWMx_CH0, EPWMx_CH1), (EPWMx_CH2, EPWMx_CH3) and (EPWMx_CH4, EPWMx_CH5) where x=0~1
- Group control bits:
  EPWMx_CH2 and EPWMx_CH4 are synchronized with EPWMx_CH0
- Supports Edge aligned mode and Center aligned mode
- Programmable dead-time insertion between complementary paired PWMs
- Each pin of EPWMx_CH0 to EPWMx_CH5 has independent polarity setting control
- Mask output control for Electrically Commutated Motor operation
- Tri-state output at reset and brake state
- Hardware brake protection
- Two Interrupt Sources:
  - Interrupt is synchronously requested at PWM frequency when up/down counter comparison matched (edge and center aligned modes) or underflow (center aligned mode).
  - Interrupt is requested when external brake pins asserted
- PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.
- High Source/Sink current.
- Supports trigger EADC

6.15 Hardware Divider (HDIV)

6.15.1 Overview

The hardware divider is useful to the high performance application. The hardware divider is a signed, integer divider with quotient and remainder outputs.

6.15.2 Features

- Supports Signed (two's complement) integer calculation.
- Supports 32-bit dividend with 16-bit divisor calculation capacity.
- Supports 32-bit quotient and 16-bit remainder outputs.
- Supports divided by 0 warning flag.
- 7 HCLK clocks taken for one cycle calculation.
- Software triggered with finish flag.

7.2 DC Electrical Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation voltage	V_{DD}	2.5	-	5.5	V	V_{DD} =2.5V ~ 5.5V				
Power Ground	V_{SS}/ AV_{SS}	-0.3	-	-	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} >= 2.5V				
Analog Operating Voltage	AV_{DD}	2.5	-	V_{DD}	V					
Analog Reference Voltage	V_{REF}	1.2	-	AV_{DD}	V					
Operating Current Normal Run Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD1}		38.7		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{DD2}		17.9		mA	5.5V	12MHz	X	✓	X
	I_{DD3}		37.2		mA	3.3V	12MHz	X	✓	✓
	I_{DD4}		16.4		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD5}		32.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD6}		15.5		mA	5.5V	12MHz	X	✓	X
	I_{DD7}		31.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD8}		14.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD9}		29.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD10}		14.5		mA	5.5V	12MHz	X	✓	X
	I_{DD11}		27.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD12}		13.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD13}		28.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD14}		14.0		mA	5.5V	12MHz	X	✓	X
	I_{DD15}		26.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD16}		12.5		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD17}		19.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD18}		10.4		mA	5.5V	12MHz	X	✓	X
	I_{DD19}		18.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD20}		8.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD6}		-		μA	3.3V	X	X	✓	X
Logic 0 Input Current (Quasi-bidirectional mode)	I_{IL}	-	-	-75	μA					
Input Leakage Current (input only)	I_{LK}	-	-	2	μA					
Logic 1 to 0 Transition Current (Quasi-bidirectional mode)	I_{TL}[3]	-	-	-660	μA	V_{DD} = 5.5V, V_{IN}<2.0V				
Internal Pull-High Resistor of /RESET[1]	R_{RST}	15	-	-	kΩ					
Input Low Voltage (TTL input)	V_{IL}	-0.3	-	$0.2V_{DD}$-0.1	V					
Input Low Voltage (Schmitt input)	V_{IL1}	-0.3		$0.3V_{DD}$	V					
Input Low Voltage (/RESET, XTAL in)	V_{IL2}	-0.3		$0.15V_{DD}$	V					
Input High Voltage (TTL input)	V_{IH}	$0.2V_{DD}$+0.9	-	V_{DD} +0.3	V					
Input High Voltage (Schmitt input, /RESET, XTAL in)	V_{IH1}	$0.7V_{DD}$	-	V_{DD} +0.3	V					
Hysteresis voltage of (Schmitt input)	V_{HY}	-	$0.2V_{DD}$	-	V					
Source Current (Quasi-bidirectional Mode)	I_{OH}	-360	-	-	μA	V_{DD} = 4.5V, V_S = 2.4V				
		-60	-	-	μA	V_{DD} = 2.7V, V_S = 2.2V				
		-50	-	-	μA	V_{DD} = 2.5V, V_S = 2.0V				
Source Current (Push-pull Mode)	I_{OH1}	-25	-	-	mA	V_{DD} = 4.5V, V_S = 2.4V				
		-4	-	-	mA	V_{DD} = 2.7V, V_S = 2.2V				
		-3	-	-	mA	V_{DD} = 2.5V, V_S = 2.0V				
Sink Current (Quasi-bidirectional and Push-pull Mode)	I_{OL}	16	-	-	mA	V_{DD} = 4.5V, V_S = 0.45V				
		10	-	-	mA	V_{DD} = 2.7V, V_S = 0.45V				
		9	-	-	mA	V_{DD} = 2.5V, V_S = 0.45V				

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. I/O pin can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.4.6 Temperature Sensor

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operation Voltage[1]		2.5	-	5.5	V
Operation Temperature		-40	-	105	℃
Current Consumption		6.4	-	10.5	μA
Gain			-1.76		mV/℃
Offset Voltage	Temp=0 ℃		720		mV

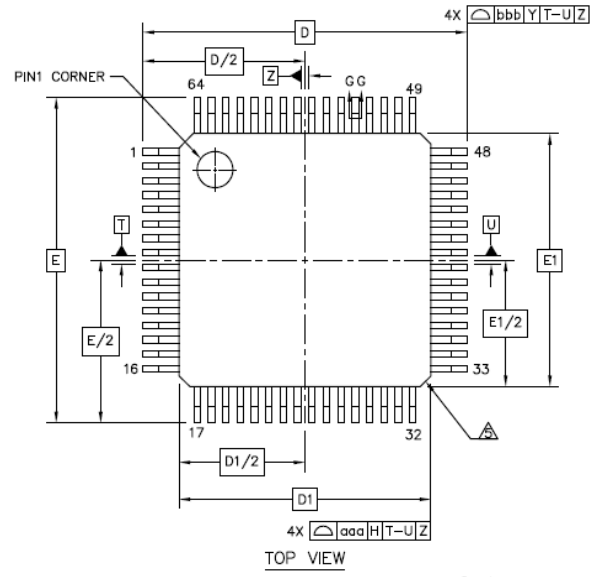
7.4.7 Comparator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage AV_{DD}	-	2.5		5.5	V
Operation Temperature	-	-40	25	85	℃
Operation Current	V_{DD}=3.0 V	-	20	40	μA
Input Offset Voltage	-	-	5	15	mV
Output Swing	-	0.1	-	V_{DD}-0.1	V
Input Common Mode Range	-	0.1	-	V_{DD}-1.2	V
DC Gain	-	-	70	-	dB
Propagation Delay	VCM=1.2 V and VDIFF=0.1 V	-	200	-	ns
Comparison Voltage	20 mV at VCM=1 V 50 mV at VCM=0.1 V 50 mV at VCM=V_{DD}-1.2 10 mV for non-hysteresis	10	20	-	mV
Hysteresis	VCM=0.4 V ~ V_{DD}-1.2 V	-	±10	-	mV
Wake-up Time	CINP=1.3 V CINN=1.2 V	-	-	2	μs

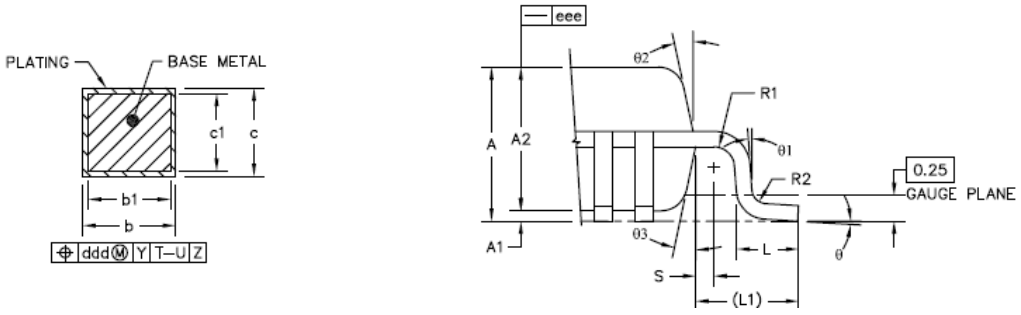
7.4.8 OP Amplifier

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AVDD	-	3.0	3.3	5.5	V
Input offset voltage	-	-	2	5	mV
Input offset average drift		-	-	1	uV/℃
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	80	-	dB
Unity gain freq.	AVDD=5V	-	-	5	MHz
Phase margin		-	50°	-	°
PSRR+	AVDD=5V	-	90	-	dB
CMRR	AVDD=5V	-	90	-	dB
Slew rate	AVDD=5V, RLOAD=33K, CLOAD=50p	6.0	-	-	V/us
Wake up time		-	-	1	us
Quiescent current		-	-	2	mA

8.2 LQFP 64S (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



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