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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0519sd3ae

Table of Contents

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Memory
  - 128K/64K bytes Flash for program memory (APROM)
  - 4KB Flash for data memory (Data Flash)
  - 8KB Flash for loader (LDROM)
  - Supports In-system program (ISP) and In-application program (IAP) application code update
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
  - 16K bytes embedded SRAM
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Supports one PLL up to 72 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock output
- Hardware divider
  - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
  - Four I/O modes:
  - TTL/Schmitt trigger input selectable
  - Bit control available
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high driver and high sink current I/O (up to 16 mA at 5V)
  - INT0 and INT1 pins with individual interrupt vectors
  - Supports up to 82/51/38 GPIOs for LQFP100/64/48 respectively
- Timers
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
  - Supports event counting function to count the event from external pin
- Watchdog Timer
  - Supports multiple clock sources from LIRC(default selection) and HCLK/2048
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Time-out reset delay period time can be selected
- Window Watchdog Timer

4.2 Pin Configuration

4.2.1 LQFP 100-pin

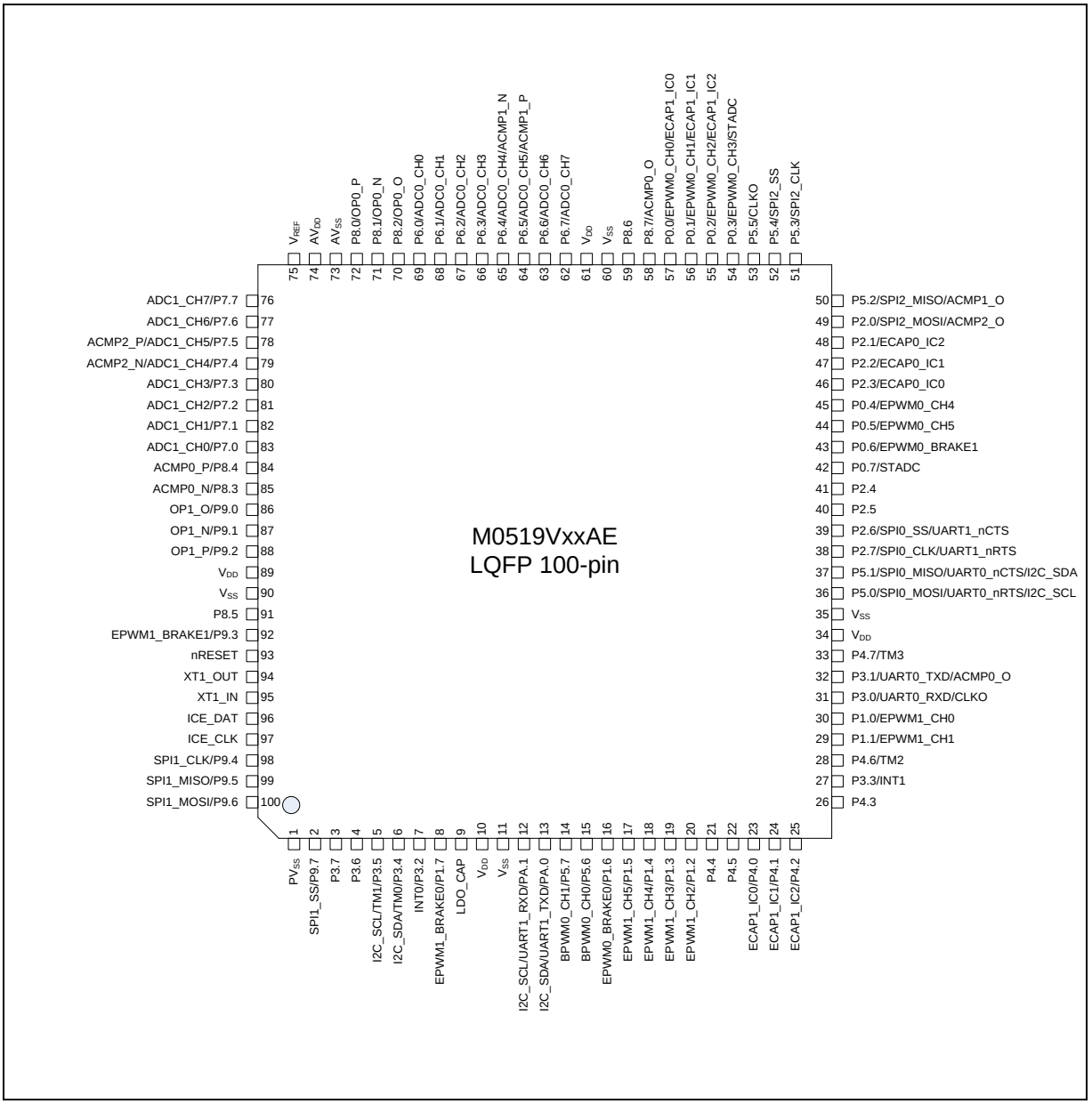


Figure 4-2 NuMicro® M0519VxxAE Series LQFP-100 Pin Diagram

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
			ECAP1_IC2	I	Input 2 of Enhanced Input Capture Unit 1
54	-	-	P0.3	I/O	General purpose digital I/O pin
			PWM0_CH3	O	PWM3 output of PWM Unit 0
			STADC	I	ADC external trigger input
45	30	-	P0.4	I/O	General purpose digital I/O pin
			PWM0_CH4	O	PWM4 output of PWM Unit 0
44	29	-	P0.5	I/O	General purpose digital I/O pin
			PWM0_CH5	O	PWM5 output of PWM Unit 0
43	-	-	P0.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE1	I	Brake input pin 1 of PWM Unit 0
42	-	23	P0.7	I/O	General purpose digital I/O pin
			STADC	I	ADC external trigger input
30	18	-	P1.0	I/O	General purpose digital I/O pin
			PWM1_CH0	O	PWM0 output of PWM Unit 1
29	17	-	P1.1	I/O	General purpose digital I/O pin
			PWM1_CH1	O	PWM1 output of PWM Unit 1
20	16	13	P1.2	I/O	General purpose digital I/O pin
			PWM1_CH2	O	PWM2 output of PWM Unit 1
19	15	14	P1.3	I/O	General purpose digital I/O pin
			PWM1_CH3	O	PWM3 output of PWM Unit 1
18	14	15	P1.4	I/O	General purpose digital I/O pin
			PWM1_CH4	O	PWM4 output of PWM Unit 1
17	13	16	P1.5	I/O	General purpose digital I/O pin
			PWM1_CH5	O	PWM5 output of PWM Unit 1
16	12	-	P1.6	I/O	General purpose digital I/O pin
			PWM0_BRAKE0	I	Brake input pin 0 of PWM Unit 0
8	4	5	P1.7	I/O	General purpose digital I/O pin
			PWM1_BRAKE0	I	Brake input pin0 of PWM Unit 1
49	31	-	P2.0	I/O	General purpose digital I/O pin
			SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin
			ACMP2_O	AO	Analog comparator 2 output pin
48	-	-	P2.1	I/O	General purpose digital I/O pin
			ECAP0_IC2	I	Input 2 of Enhanced Input Capture Unit 0

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
71	44	33	P8.1	**I/O**	General purpose digital I/O pin
			OP0_N	**AI**	OP Amplifier 0 negative input
70	43	32	P8.2	**I/O**	General purpose digital I/O pin
			OP0_O	**AO**	OP Amplifier 0 output
85	-	-	P8.3	**I/O**	General purpose digital I/O pin
			ACMP0_N	**AI**	Analog comparator negative input pin
84	-	-	P8.4	**I/O**	General purpose digital I/O pin
			ACMP0_P	**AI**	Analog comparator positive input pin
91	-	-	P8.5	**I/O**	General purpose digital I/O pin
59	-	-	P8.6	**I/O**	General purpose digital I/O pin
58	-	-	P8.7	**I/O**	General purpose digital I/O pin
			ACMP0_O	**O**	Analog comparator output pin
86	57	45	P9.0	**I/O**	General purpose digital I/O pin
			OP1_O	**AO**	OP Amplifier 1 output
87	58	46	P9.1	**I/O**	General purpose digital I/O pin
			OP1_N	**AI**	OP Amplifier 1 negative input
88	59	47	P9.2	**I/O**	General purpose digital I/O pin
			OP1_P	**AI**	OP Amplifier 1 positive input
92	-	-	P9.3	**I/O**	General purpose digital I/O pin
			PWM1_BRAKE1	**I**	Brake input pin 1 of PWM Unit 1
98	-	-	P9.4	**I/O**	General purpose digital I/O pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
99	-	-	P9.5	**I/O**	General purpose digital I/O pin
			SPI1_MISO	**I/O**	SPI1 MISO (Master In, Slave Out) pin
100	-	-	P9.6	**I/O**	General purpose digital I/O pin
			SPI1_MOSI	**I/O**	SPI1 MOSI (Master Out, Slave In) pin
2	-	-	P9.7	**I/O**	General purpose digital I/O pin
			SPI1_SS	**I/O**	SPI1 slave select pin
13	9	10	PA.0	**I/O**	General purpose digital I/O pin
			UART1_TXD	**O**	Data transmitter output pin for UART1
			I2C0_SDA	**I/O**	I2C0 data input/output pin
12	8	9	PA.1	**I/O**	General purpose digital I/O pin
			UART1_RXD	**I**	Data Receiver input pin for UART1

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

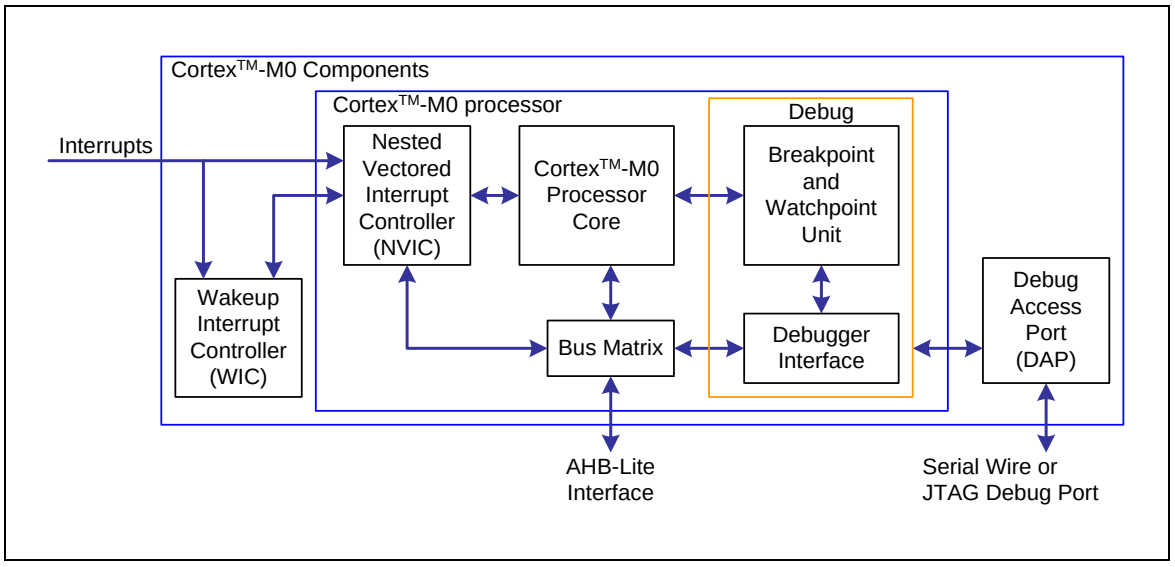


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Distribution
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset pin (nRESET)
  - Watchdog Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - SYS Reset - SYSRESETREQ (AIRCR[2])
  - Cortex®-M0 Core One-shot Reset - CPU_RST (IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST (IPRSTC1[0])

Power-on Reset or CHIP_RST (IPRST1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into two segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.

The output of internal voltage regulators, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}).

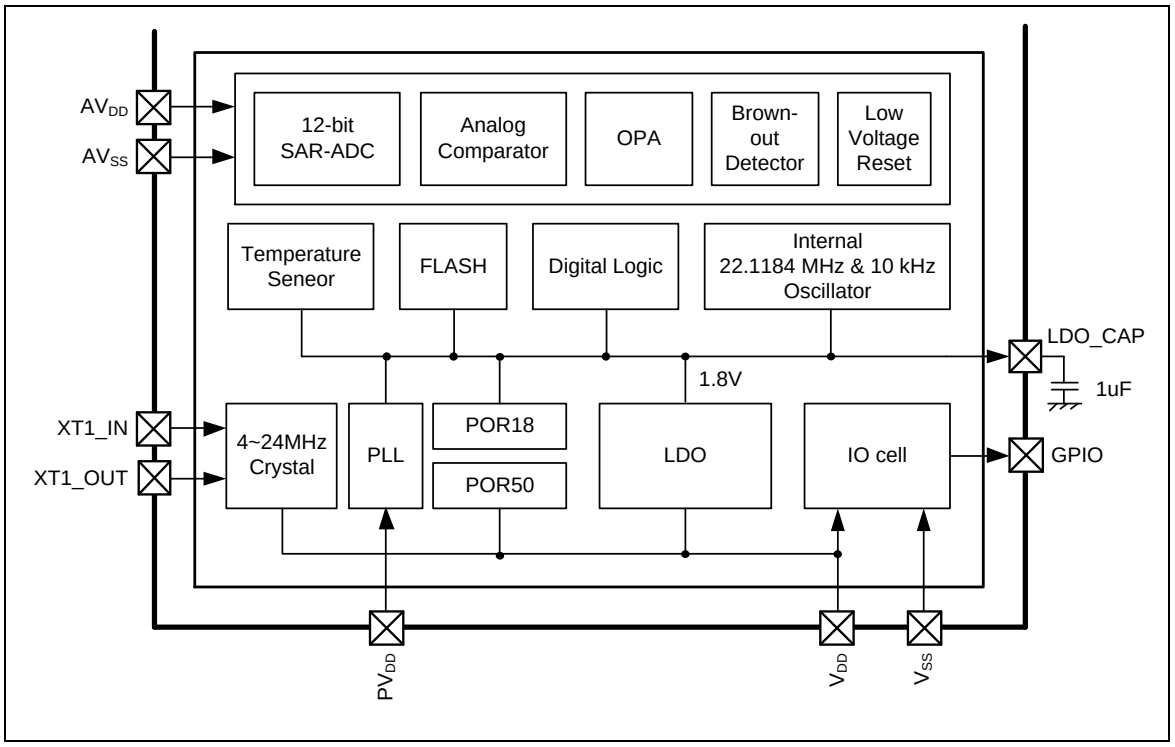


Figure 6-2 NuMicro® M0519 Series Power Distribution Diagram

6.2.5 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.6.2 *Vector Table*

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table

6.2.6.3 *Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® M0519 Series is equipped with 128/64 KB on-chip embedded flash for application program memory (APROM) and data flash, and with 8K bytes for ISP loader program memory (LDROM) that could be programmed boot loader to update APROM and data flash through In System Programming (ISP) procedure. ISP function enables user to update embedded flash when chip is soldered on PCB. After chip is powered on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select CBS (Config0[7:6]). By the way, the NuMicro® M0519 Series also provides data flash for user to store some application dependent data before chip power off. For 128 KB APROM device, the data flash is shared with original 128 KB program memory and its start address is configurable in Config1. For 64 KB APROM device, the data flash is fixed at 4K bytes.

6.4.2 Features

- Runs up to 72 MHz and optional up to 50 MHz with zero wait state for continuous address read access
- Supports 512 bytes page erase for all embedded flash
- Supports 128/64 Kbytes application program ROM (APROM)
- Supports 8 KB loader ROM (LDROM)
- Supports 4KB data flash for 64 Kbytes APROM device
- Supports configurable data flash size for 128KB APROM device
- Supports 8 bytes User Configuration block to control system initiation
- Support In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded flash memory

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software from running to uncontrollable state by any unpredictable condition usually generated by external interferences or unexpected logical conditions.

When the window function is used to trim the watchdog behavior to match the application perfectly, software must refresh the counter before time-out.

6.11.2 Features

- 6-bit down counter value WWDTCVAL (WWDTCVR[5:0]) and 6-bit compare value WINCMP (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value PERIODSEL (WWDTCR[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.12 Universal Asynchronous Receiver Transmitter (UART)

6.12.1 Overview

The NuMicro® M0519 series provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART Controller performs Normal Speed UART and supports flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports seven types of interrupts. The UART controller also supports IrDA SIR, RS-485 and LIN.

6.12.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control/flow control function (nCTS, nRTS) and programmable nRTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports nCTS wake-up function
- Supports 8-bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by nRTS pin

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. I²C controller supports Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- A built-in a 14-bit time out counter requested the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- External pull-up resistors are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)

7.2 DC Electrical Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation voltage	V_{DD}	2.5	-	5.5	V	V_{DD} =2.5V ~ 5.5V				
Power Ground	V_{SS}/ AV_{SS}	-0.3	-	-	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} >= 2.5V				
Analog Operating Voltage	AV_{DD}	2.5	-	V_{DD}	V					
Analog Reference Voltage	V_{REF}	1.2	-	AV_{DD}	V					
Operating Current Normal Run Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD1}		38.7		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{DD2}		17.9		mA	5.5V	12MHz	X	✓	X
	I_{DD3}		37.2		mA	3.3V	12MHz	X	✓	✓
	I_{DD4}		16.4		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD5}		32.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD6}		15.5		mA	5.5V	12MHz	X	✓	X
	I_{DD7}		31.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD8}		14.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD9}		29.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD10}		14.5		mA	5.5V	12MHz	X	✓	X
	I_{DD11}		27.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD12}		13.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD13}		28.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD14}		14.0		mA	5.5V	12MHz	X	✓	X
	I_{DD15}		26.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD16}		12.5		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD17}		19.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD18}		10.4		mA	5.5V	12MHz	X	✓	X
	I_{DD19}		18.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD20}		8.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Idle Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE13}		22.3		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE14}		8.1		mA	5.5V	12MHz	X	✓	X
	I_{IDLE15}		20.8		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE16}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE17}		16.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE18}		6.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE19}		14.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE20}		4.9		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE21}		8.6		mA	5.5V	X	✓	X	✓
	I_{IDLE22}		2.2		mA	5.5V	X	✓	X	X
	I_{IDLE23}		8.6		mA	3.3V	X	✓	X	✓
	I_{IDLE24}		2.2		mA	3.3V	X	✓	X	X
Operating Current Idle Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE25}		7.2		mA	5.5V	12MHz	X	X	✓
	I_{IDLE26}		3.4		mA	5.5V	12MHz	X	X	X
	I_{IDLE27}		5.7		mA	3.3V	12MHz	X	X	✓
	I_{IDLE28}		1.9		mA	3.3V	12MHz	X	X	X
Operating Current Idle Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{IDLE30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{IDLE31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{IDLE32}		0.11		mA	3.3V	X	10KHz	X	X
Standby Current Power-down Mode	I_{PWD1}		-		µA	VDD	HXT	HIRC	LIRC	All digital module
						5.5V	✓	X	X	X
	I_{PWD2}		-		µA	5.5V	X	✓	X	X
	I_{PWD3}		-		µA	5.5V	X	X	✓	X
	I_{PWD4}		-		µA	3.3V	✓	X	X	X
	I_{PWD5}		-		µA	3.3V	X	✓	X	X

7.3.2 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Frequency (After calibration)	-	-	22.1184	-	MHz
	+25°C; V_{DD} = 5V	-1	-	+1	%
	-40 to +105°C; V_{DD} = 2.5V~5.5V	-2	-	+2	%
Operation Current	V_{DD} =5V	-	500	-	uA

7.3.3 Internal 10 kHz Oscillator

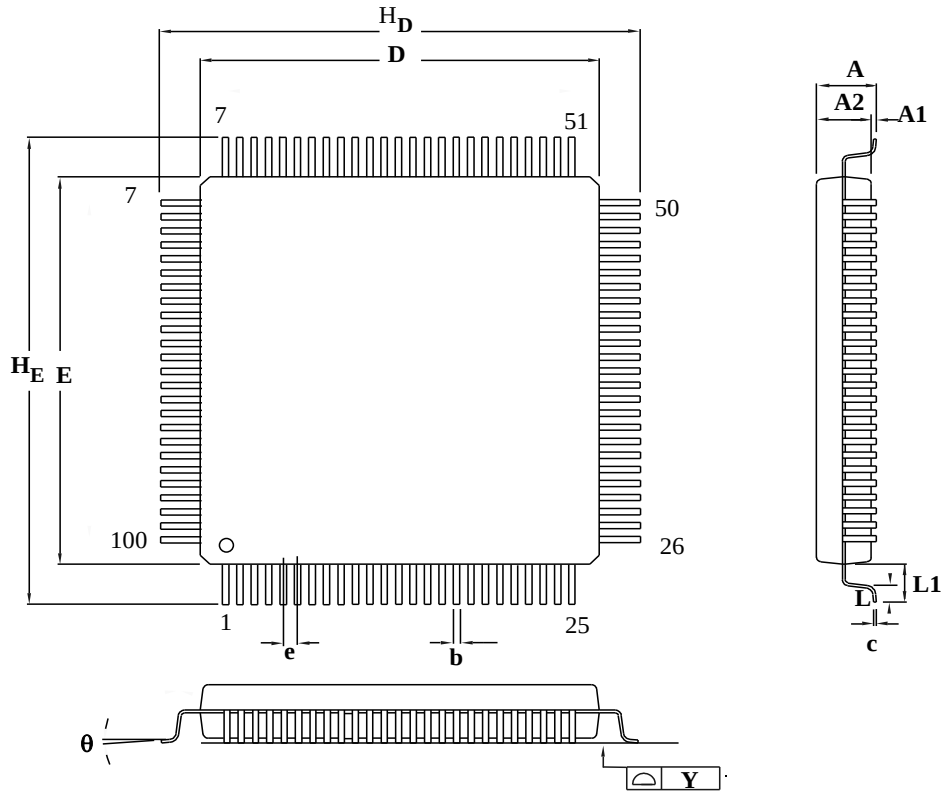
PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

7.4.8 OP Amplifier

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
AVDD	-	3.0	3.3	5.5	V
Input offset voltage	-	-	2	5	mV
Input offset average drift		-	-	1	uV/℃
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	80	-	dB
Unity gain freq.	AVDD=5V	-	-	5	MHz
Phase margin		-	50°	-	°
PSRR+	AVDD=5V	-	90	-	dB
CMRR	AVDD=5V	-	90	-	dB
Slew rate	AVDD=5V, RLOAD=33K, CLOAD=50p	6.0	-	-	V/us
Wake up time		-	-	1	us
Quiescent current		-	-	2	mA

8 PACKAGE DIMENSIONS

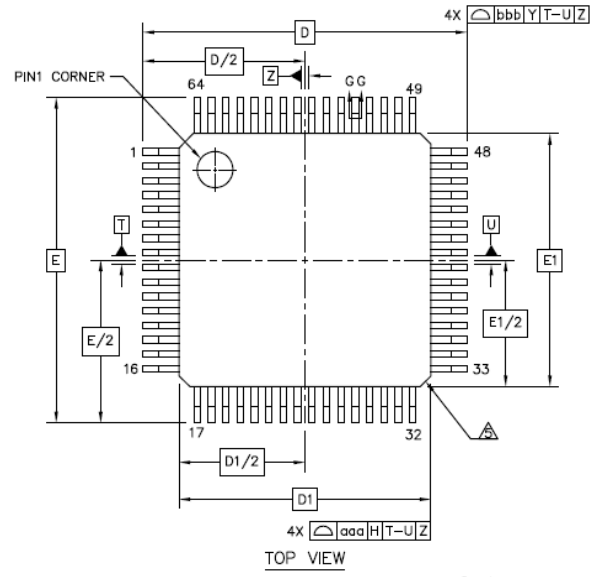
8.1 LQFP 100V (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8.2 LQFP 64S (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05