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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0519se3ae

List of Figures

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
47	-	-	P2.2	**I/O**	General purpose digital I/O pin
			ECAP0_IC1	**I**	Input 1 of Enhanced Input Capture Unit 0
46	-	-	P2.3	**I/O**	General purpose digital I/O pin
			ECAP0_IC0	**I**	Input 0 of Enhanced Input Capture Unit 0
41	28	-	P2.4	**I/O**	General purpose digital I/O pin
40	27	-	P2.5	**I/O**	General purpose digital I/O pin
39	26	22	P2.6	**I/O**	General purpose digital I/O pin
			SPI0_SS	**I/O**	SPI0 slave select pin
			UART1_nCTS	**I**	UART1 CTS pin
38	25	21	P2.7	**I/O**	General purpose digital I/O pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin
			UART1_nRTS	**O**	UART1 RTS pin
31	19	17	P3.0	**I/O**	General purpose digital I/O pin
			UART0_RXD	**I**	Data Receiver input pin for UART0
32	20	18	P3.1	**I/O**	General purpose digital I/O pin
			UART0_TXD	**O**	Data transmitter output pin for UART0
			ACMP0_O	**AO**	Analog comparator 0 output
7	3	-	P3.2	**I/O**	General purpose digital I/O pin
			INT0	**I**	External Interrupt 0 input pin
27	-	-	P3.3	**I/O**	General purpose digital I/O pin
			INT1	**I**	External Interrupt 1 input pin
6	2	-	P3.4	**I/O**	General purpose digital I/O pin
			TM0	**I/O**	Timer0 external clock
			I2C0_SDA	**I/O**	I2C0 data input/output pin
5	1	-	P3.5	**I/O**	General purpose digital I/O pin
			TM1	**I/O**	Timer1 external clock
			I2C0_SCL	**I/O**	I2C0 clock output pin
4	-	-	P3.6	**I/O**	General purpose digital I/O pin
3	-	-	P3.7	**I/O**	General purpose digital I/O pin
23	-	-	P4.0	**I/O**	General purpose digital I/O pin
			ECAP1_IC0	**I**	Input 0 of Enhanced Input Capture Unit 1
24	-	-	P4.1	**I/O**	General purpose digital I/O pin
			ECAP1_IC1	**I**	Input 1 of Enhanced Input Capture Unit 1

- 32 external interrupt inputs, each with four levels of priority
- Dedicated Non-maskable Interrupt (NMI) input
- Supports for both level-sensitive and pulse-sensitive interrupt lines
- Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode

- Debug support
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Resets
- System Power Distribution
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset , multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSRC register.

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the Reset pin (nRESET)
  - Watchdog Time-out Reset (WDT)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD)
- Software Reset
  - SYS Reset - SYSRESETREQ (AIRCR[2])
  - Cortex®-M0 Core One-shot Reset - CPU_RST (IPRSTC1[1])
  - Chip One-shot Reset - CHIP_RST (IPRSTC1[0])

Power-on Reset or CHIP_RST (IPRST1[0]) reset the whole chip including all peripherals, external crystal circuit and BS (ISPCON[1]) bit.

SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset external crystal circuit and BS (ISPCON[1]) bit.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into two segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the I/O pins and internal regulator which provides a fixed 1.8V power for digital operation.

The output of internal voltage regulators, LDO_CAP, requires an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}).

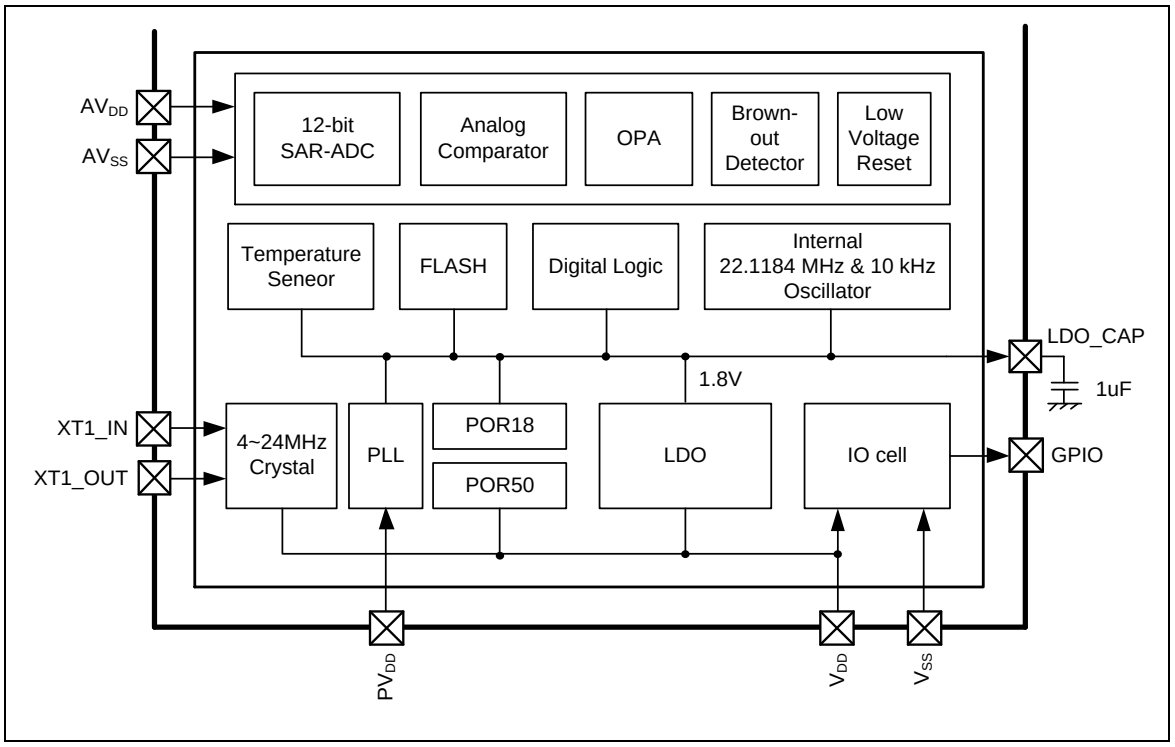


Figure 6-2 NuMicro® M0519 Series Power Distribution Diagram

6.2.6 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”, which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

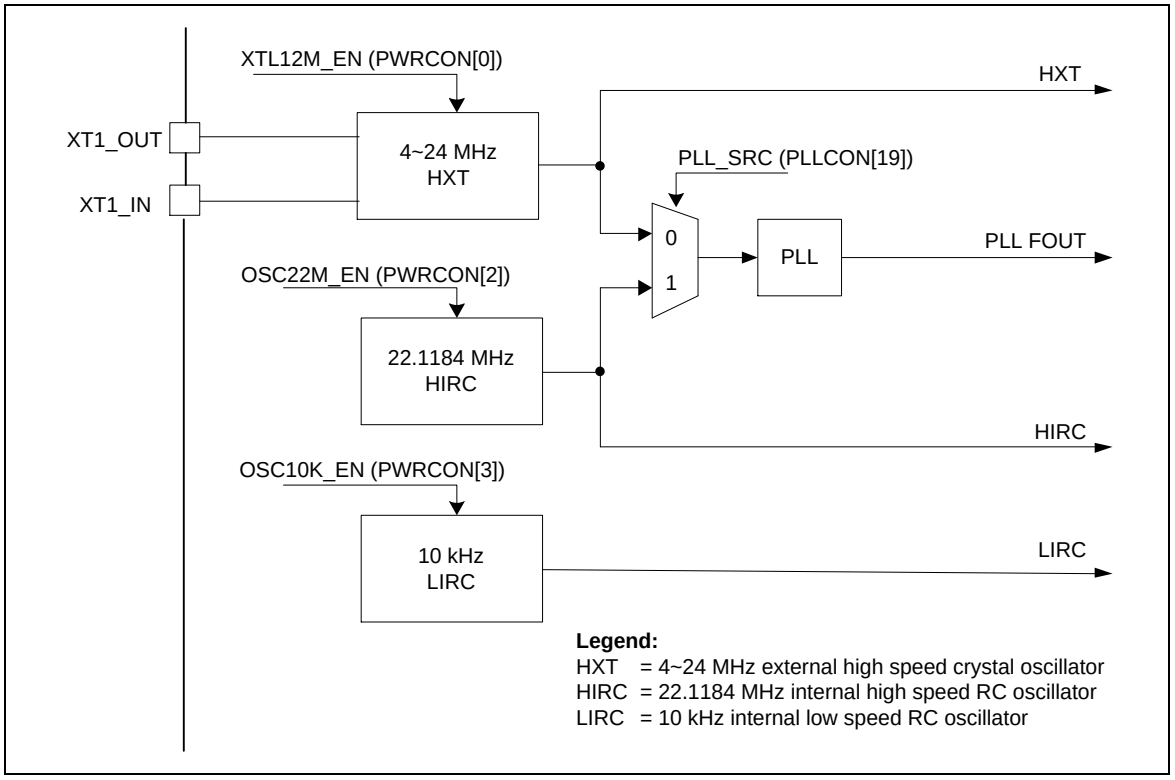


Figure 6-3 Clock Generator Block Diagram

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through TDR (TDR[23:0])
- Supports event counting function
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter

6.16 Enhanced Analog-to-Digital Converter (EADC)

6.16.1 Overview

The NuMicro® M0519 Series contains two 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 16 input channels. The two A/D converters ADCA and ADCB can be sampled with Simultaneous or Single Sampling mode. The A/D converters can be started by software, PWM triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC pulse trigger and external STADC pin input signal.

Note: The analog input port pins must be configured as input type before the EADC function is enabled.

6.16.2 Features

- Analog input voltage range: 0~V_{REF}(Max to 5.0V).
- 12-bit resolution and 10-bit accuracy is guaranteed.
- Up to 16 single-end analog input channels.
- Two SAR ADC converters.
- Four EADC interrupts with individual interrupt vector addresses.
- Maximum EADC clock frequency: 16MHz.
- Up to 1.6M SPS conversion rate, each of ADC converter conversion time less than 1.25μs.
- Two operating modes
  - Single sampling mode: two ADC converters run at normal operation.
  - Simultaneous sampling mode: Allow two ADC converters can be sampled simultaneously.
- An A/D conversion can be started by:
  - Writing 1 to ADST(ADSSTR[n]) bit (n = 0~15) through software
  - External pin STADC
  - Timer0~3 overflow pulse triggers
  - ADINT0, ADINT1 interrupt EOC pulse triggers
  - PWM triggers
- Conversion results are held in 16 data registers with valid and overrun indicators.
- SAMPLEA0~7 ADC control logic modules, each of them is configurable for ADCA converter channel AINA0~7 and trigger source.
- SAMPLEB0~7 ADC control logic modules, each of them is configurable for ADCB converter channel AINB0~7 and trigger source.
- Channel AINA0 supports 2 input sources: external analog voltage and internal OP0 Amplifier output voltage.
- Channel AINB0 supports 2 input sources: external analog voltage and internal OP1 Amplifier output voltage.
- Channel AINA7 supports 4 input sources: external analog voltage, internal fixed band-gap voltage, internal temperature sensor output, and analog ground.

6.17 Analog Comparator (ACMP)

6.17.1 Overview

The NuMicro® M0519 Series contains three comparators. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **錯誤! 找不到參照來源。**.

6.17.2 Features

- Analog input voltage range: 0~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Supports comparator output inverse function
- Supports the comparator output can be the brake source for EPWM function
- ACMP0 supports
  - 2 positive sources: ACMP0_P and OP0_O
  - 2 negative sources: ACMP0_N and Internal band-gap voltage (V_{BG})
- ACMP1 supports
  - 2 positive sources: ACMP1_P and OP1_O
  - 2 negative sources: ACMP1_N and Internal band-gap voltage (V_{BG})
- ACMP2 supports
  - 1 positive sources: ACMP2_P
  - 2 negative sources: ACMP2_N and Internal band-gap voltage (V_{BG})
- Shares one ACMP interrupt vector for all comparators

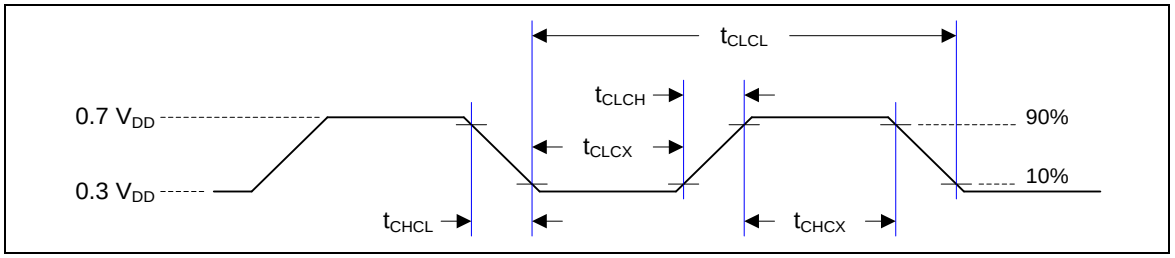
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD21}		11.7		mA	5.5V	X	✓	X	✓
	I_{DD22}		5.3		mA	5.5V	X	✓	X	X
	I_{DD23}		11.6		mA	3.3V	X	✓	X	✓
	I_{DD24}		5.2		mA	3.3V	X	✓	X	X
Operating Current Normal Run Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD25}		8.6		mA	5.5V	12MHz	X	X	✓
	I_{DD26}		4.9		mA	5.5V	12MHz	X	X	X
	I_{DD27}		7.2		mA	3.3V	12MHz	X	X	✓
	I_{DD28}		3.4		mA	3.3V	12MHz	X	X	X
Operating Current Normal Run Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{DD30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{DD31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{DD32}		0.11		mA	3.3V	X	10KHz	X	X
Operating Current Idle Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE1}		30.1		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{IDLE2}		9.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE3}		28.6		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE4}		7.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE5}		25.7		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE6}		8.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE7}		24.2		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE8}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE9}		23.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE10}		8.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE11}		21.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE12}		6.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
	I_{PWD6}		-		μA	3.3V	X	X	✓	X
Logic 0 Input Current (Quasi-bidirectional mode)	I_{IL}	-	-	-75	μA					
Input Leakage Current (input only)	I_{LK}	-	-	2	μA					
Logic 1 to 0 Transition Current (Quasi-bidirectional mode)	I_{TL}[3]	-	-	-660	μA	V_{DD} = 5.5V, V_{IN}<2.0V				
Internal Pull-High Resistor of /RESET[1]	R_{RST}	15	-	-	kΩ					
Input Low Voltage (TTL input)	V_{IL}	-0.3	-	$0.2V_{DD}$-0.1	V					
Input Low Voltage (Schmitt input)	V_{IL1}	-0.3		$0.3V_{DD}$	V					
Input Low Voltage (/RESET, XTAL in)	V_{IL2}	-0.3		$0.15V_{DD}$	V					
Input High Voltage (TTL input)	V_{IH}	$0.2V_{DD}$+0.9	-	V_{DD} +0.3	V					
Input High Voltage (Schmitt input, /RESET, XTAL in)	V_{IH1}	$0.7V_{DD}$	-	V_{DD} +0.3	V					
Hysteresis voltage of (Schmitt input)	V_{HY}	-	$0.2V_{DD}$	-	V					
Source Current (Quasi-bidirectional Mode)	I_{OH}	-360	-	-	μA	V_{DD} = 4.5V, V_S = 2.4V				
		-60	-	-	μA	V_{DD} = 2.7V, V_S = 2.2V				
		-50	-	-	μA	V_{DD} = 2.5V, V_S = 2.0V				
Source Current (Push-pull Mode)	I_{OH1}	-25	-	-	mA	V_{DD} = 4.5V, V_S = 2.4V				
		-4	-	-	mA	V_{DD} = 2.7V, V_S = 2.2V				
		-3	-	-	mA	V_{DD} = 2.5V, V_S = 2.0V				
Sink Current (Quasi-bidirectional and Push-pull Mode)	I_{OL}	16	-	-	mA	V_{DD} = 4.5V, V_S = 0.45V				
		10	-	-	mA	V_{DD} = 2.7V, V_S = 0.45V				
		9	-	-	mA	V_{DD} = 2.5V, V_S = 0.45V				

Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. I/O pin can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

7.3.1 External 4~24MHz Crystal

PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
Operation Voltage V_{DD}	-	2.5	-	5.5	V
Temperature	-	-40	-	85	℃
Operating Current	12 MHz at V_{DD} = 5V	-	1	-	mA
Clock Frequency	External crystal	4		24	MHz

7.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

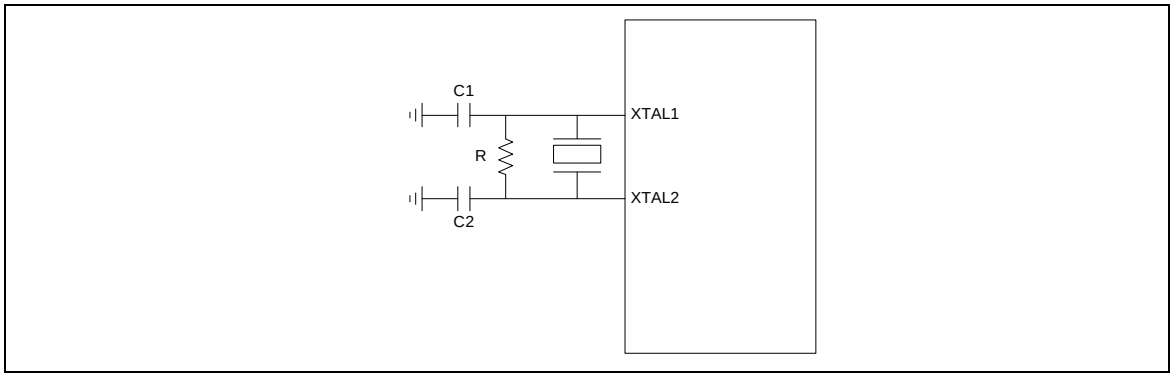


Figure 7–1 Typical Crystal Application Circuit

7.3.2 Internal 22.1184 MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Frequency (After calibration)	-	-	22.1184	-	MHz
	+25°C; V_{DD} = 5V	-1	-	+1	%
	-40 to +105°C; V_{DD} = 2.5V~5.5V	-2	-	+2	%
Operation Current	V_{DD} =5V	-	500	-	uA

7.3.3 Internal 10 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

7.4 Analog Characteristics

7.4.1 12-bit SARADC

PARAMETER	SYMBOL	CONDITON	MIN.	TYP.	MAX.	UNIT
Resolution	-		-	-	12	Bit
Differential nonlinearity error	DNL		-	-1~2	-1~4	LSB
Integral nonlinearity error	INL		-	±2	±4	LSB
Offset error	EO		-	±1	10	LSB
Full scale error	EG		-	1	1.005	LSB
Monotonic	-		Guaranteed			
ADC clock frequency	F_{ADC}	AVDD = 5V	-	-	16	MHz
		AVDD = 3V	-	-	8	
Sample rate	F_S	AVDD = 5V	-	-	800	ksps
		AVDD = 3V	-	-	400	
Sample time	T_S		-	8	-	Clock
Conversion time	T_{ADC}		-	12	-	Clock
Supply voltage	AV_{DD}		2.5	-	5.5	V
V_{REF} voltage	V_{REF}		2.0		AV_{DD}	
Supply current	I_{DDA}		-	1.5	-	mA
Reference current	I_{REF}		-	1	-	mA
Input voltage	VIN		0	-	V_{REF}	V
Capacitance	CIN		-	5	-	pF

7.4.2 LDO

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage V_{DD}	2.5		5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5 V
Operating Temperature	-40	25	105	℃	
Cbp	-	1	-	μF	R_{ESR} = 1 Ω

Note:

1. It is recommended that a 10 uF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1 μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

7.4.3 Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	105	℃
Threshold Voltage	-	1.6	2.0	2.4	V
Hysteresis	-	0	0	0	V

7.4.4 Brown-out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	105	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	105	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

7.5 Flash DC Electrical Characteristics

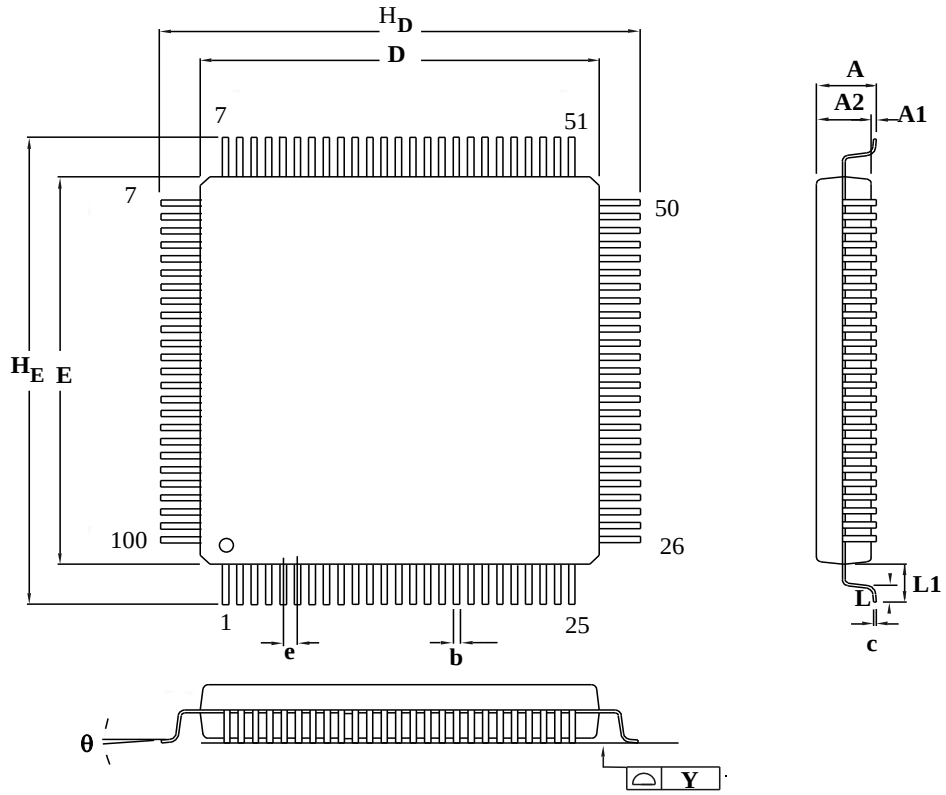
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		10000			cycles[1]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA

Note : This table is guaranteed by design, not test in production.

[1] Number of program/erase cycles.
[2] V_{DD} is source from chip LDO output voltage.

8 PACKAGE DIMENSIONS

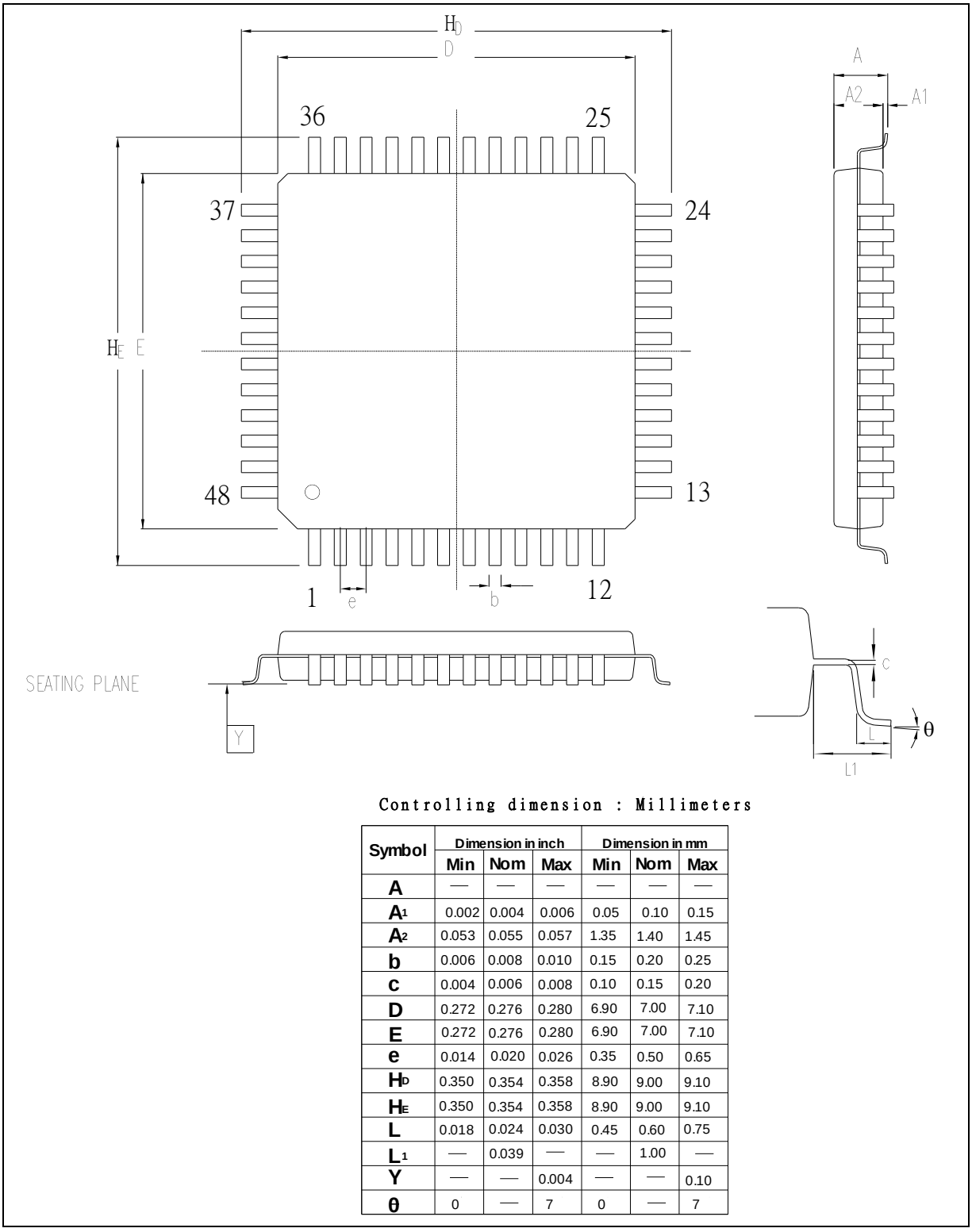
8.1 LQFP 100V (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8.3 LQFP 48L (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.