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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0519ve3ae

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 72 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode by WFI instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports Serial Wire Debug (SWD) support with two watchpoints and four breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5V to 5.5V
- Memory
  - 128K/64K bytes Flash for program memory (APROM)
  - 4KB Flash for data memory (Data Flash)
  - 8KB Flash for loader (LDROM)
  - Supports In-system program (ISP) and In-application program (IAP) application code update
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
  - 16K bytes embedded SRAM
- Clock Control
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40˚C ~ +105˚C)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - Built-in 4~24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Supports one PLL up to 72 MHz for high performance system operation, sourced from HIRC and HXT
  - Supports clock output
- Hardware divider
  - Supports signed 32-bit dividend, 16-bit divisor operation
- GPIO port
  - Four I/O modes:
  - TTL/Schmitt trigger input selectable
  - Bit control available
  - I/O pin configured as interrupt source with edge/level trigger setting
  - Supports high driver and high sink current I/O (up to 16 mA at 5V)
  - INT0 and INT1 pins with individual interrupt vectors
  - Supports up to 82/51/38 GPIOs for LQFP100/64/48 respectively
- Timers
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
  - Supports event counting function to count the event from external pin
- Watchdog Timer
  - Supports multiple clock sources from LIRC(default selection) and HCLK/2048
  - 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
  - Able to wake up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
  - Time-out reset delay period time can be selected
- Window Watchdog Timer

- Brown-out detector
  - 4 levels: 4.4V/3.7V/2.7V/2.2V
  - Optional brown-out interrupt or reset
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Low Voltage Reset
- 96-bit unique ID
- Operating Temperature: -40℃~105℃
- Develop tools: parallel writer or In-Circuit Programming (ICP) writer
- Packages:
  - All Green package (RoHS)
  - LQFP 100/64/48-pin

Pin Number			Pin Name	Pin Type[1]	Description
100- pin	64-pin	48-pin			
47	-	-	P2.2	**I/O**	General purpose digital I/O pin
			ECAP0_IC1	**I**	Input 1 of Enhanced Input Capture Unit 0
46	-	-	P2.3	**I/O**	General purpose digital I/O pin
			ECAP0_IC0	**I**	Input 0 of Enhanced Input Capture Unit 0
41	28	-	P2.4	**I/O**	General purpose digital I/O pin
40	27	-	P2.5	**I/O**	General purpose digital I/O pin
39	26	22	P2.6	**I/O**	General purpose digital I/O pin
			SPI0_SS	**I/O**	SPI0 slave select pin
			UART1_nCTS	**I**	UART1 CTS pin
38	25	21	P2.7	**I/O**	General purpose digital I/O pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin
			UART1_nRTS	**O**	UART1 RTS pin
31	19	17	P3.0	**I/O**	General purpose digital I/O pin
			UART0_RXD	**I**	Data Receiver input pin for UART0
32	20	18	P3.1	**I/O**	General purpose digital I/O pin
			UART0_TXD	**O**	Data transmitter output pin for UART0
			ACMP0_O	**AO**	Analog comparator 0 output
7	3	-	P3.2	**I/O**	General purpose digital I/O pin
			INT0	**I**	External Interrupt 0 input pin
27	-	-	P3.3	**I/O**	General purpose digital I/O pin
			INT1	**I**	External Interrupt 1 input pin
6	2	-	P3.4	**I/O**	General purpose digital I/O pin
			TM0	**I/O**	Timer0 external clock
			I2C0_SDA	**I/O**	I2C0 data input/output pin
5	1	-	P3.5	**I/O**	General purpose digital I/O pin
			TM1	**I/O**	Timer1 external clock
			I2C0_SCL	**I/O**	I2C0 clock output pin
4	-	-	P3.6	**I/O**	General purpose digital I/O pin
3	-	-	P3.7	**I/O**	General purpose digital I/O pin
23	-	-	P4.0	**I/O**	General purpose digital I/O pin
			ECAP1_IC0	**I**	Input 0 of Enhanced Input Capture Unit 1
24	-	-	P4.1	**I/O**	General purpose digital I/O pin
			ECAP1_IC1	**I**	Input 1 of Enhanced Input Capture Unit 1

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return.

Figure 6-1 shows the functional controller of processor.

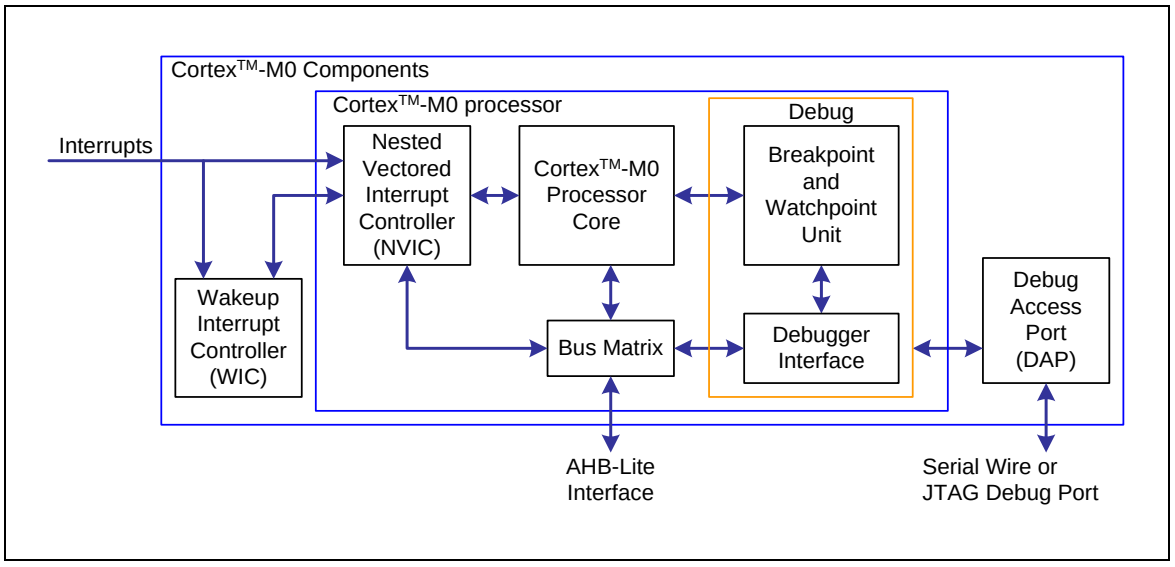


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC:

6.2.5 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the SLEEPDEEP (SCR[2]) bit is set to 1. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In the Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal oscillator and 22.1184 MHz internal high speed RC oscillator to reduce the overall system power consumption. Figure 6-3 shows the clock generator and the overview of the clock source control.

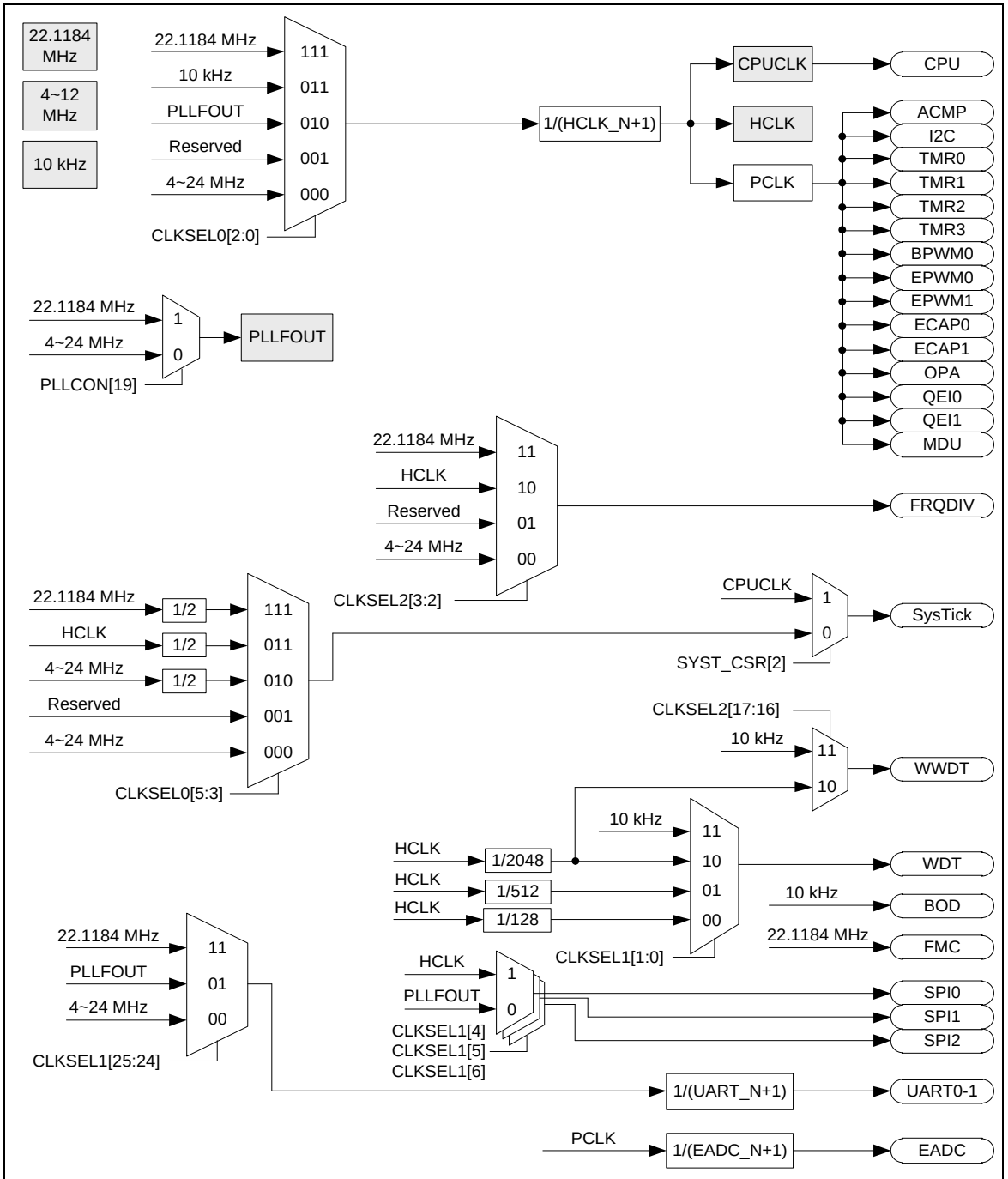
The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL_FOUT), PLL source can be selected from 4~24 MHz external high speed crystal oscillator (HXT) or 22.1184 MHz internal high speed RC oscillator (HIRC)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index (OSC22M_STB(CLKSTATUS[4]), OSC10K_STB(CLKSTATUS[3]), PLL_STB(CLKSTATUS[2]) and XTL12M_STB(CLKSTATUS[0])) are set to 1 after stable counter value reach a define value as Table 6-5. System and peripheral can use these clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will auto clear when user disables the clock source (OSC10K_EN(PWRCON[3]), OSC22M_EN(PWRCON[2]), XTL12M_EN(PWRCON[0]) and PD(PLLCON[16])). Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value
HXT	4096 HXT clock
PLL	6144 PLL source (PLL source is HXT if PLL_SRC(PLLCON[19]) = 0, or HIRC if PLL_SRC(PLLCON[19]) = 1)
HIRC	256 HIRC clock
LIRC	1 LIRC

Table 6-5 Clock Stable Count Value Table



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6-4 Clock Generator Global View Diagram

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® M0519 Series has up to 82 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 82 pins are arranged in 10 ports named as P0, P1, P2, P3, P4, P5, P6, P7, P8, P9 and PA. The P0/1/2/3/4/5/6/7/8/9 port has the maximum of 8 pins and PA port has the maximum of 2 pins. Each of the 82 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are stay at input mode. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} is from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by Px_TYPE[7:0] in Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling pin interrupt function will also enable the pin wake-up function

6.6 Timer Controller (TIMER)

6.6.1 Overview

The Timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through TDR (TDR[23:0])
- Supports event counting function
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter

6.7 Basic PWM Generator and Capture Timer (BPWM)

6.7.1 Overview

The NuMicro® M0519 series has 1 set of BPWM group (BPWM0), supporting 1 set of BPWM generators that can be configured as 2 independent BPWM outputs, BPWM0_CH0 and BPWM0_CH1, or as 1 complementary BPWM pairs, (BPWM0_CH0, BPWM0_CH1) with programmable dead-zone generator.

The BPWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two BPWM Timers including two clock selectors, two 16-bit BPWM down-counters for BPWM period control, two 16-bit comparators for BPWM duty control and one dead-zone generator. The BPWM generator provides two independent BPWM interrupt flags which are set by hardware when the corresponding BPWM period down counter reaches zero.

Each BPWM interrupt source with its corresponding enable bit can cause CPU to request BPWM interrupt. The BPWM generators can be configured as one-shot mode to produce only one BPWM cycle signal or auto-reload mode to output BPWM waveform continuously. BPWM can be used to trigger EADC when operation in center-aligned mode.

6.7.2 Features

6.7.2.1 BPWM Function:

- Up to 1 BPWM group to support 2 BPWM channels or 1 BPWM paired channels.
- Supports 8-bit prescaler from 1 to 255
- Up to 16-bit resolution BPWM timer
- PWM timer supports edge-aligned and center-aligned operation type
- One-shot or Auto-reload mode BPWM
- PWM Interrupt request synchronized with BPWM period or duty
- Supports dead-zone generator with 8-bit resolution for BPWM paired channels
- Supports trigger EADC

6.7.2.2 Capture Function:

- Supports 2 Capture input channels shared with 2 BPWM output channels
- Supports rising or falling capture condition
- Supports rising or falling capture interrupt

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software from running to uncontrollable state by any unpredictable condition usually generated by external interferences or unexpected logical conditions.

When the window function is used to trim the watchdog behavior to match the application perfectly, software must refresh the counter before time-out.

6.11.2 Features

- 6-bit down counter value WWDTCVAL (WWDTCVR[5:0]) and 6-bit compare value WINCMP (WWDTCR[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value PERIODSEL (WWDTCR[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.17 Analog Comparator (ACMP)

6.17.1 Overview

The NuMicro® M0519 Series contains three comparators. The comparator output is logic 1 when positive input voltage is greater than negative input voltage; otherwise the output is logic 0. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **錯誤! 找不到參照來源。**.

6.17.2 Features

- Analog input voltage range: 0~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Supports comparator output inverse function
- Supports the comparator output can be the brake source for EPWM function
- ACMP0 supports
  - 2 positive sources: ACMP0_P and OP0_O
  - 2 negative sources: ACMP0_N and Internal band-gap voltage (V_{BG})
- ACMP1 supports
  - 2 positive sources: ACMP1_P and OP1_O
  - 2 negative sources: ACMP1_N and Internal band-gap voltage (V_{BG})
- ACMP2 supports
  - 1 positive sources: ACMP2_P
  - 2 negative sources: ACMP2_N and Internal band-gap voltage (V_{BG})
- Shares one ACMP interrupt vector for all comparators

6.18 OP Amplifier (OPA)

6.18.1 Overview

This device integrated two operational amplifiers. It can be enabled through OP0_EN (OPACR[0]) and OP1_EN (OPACR[1]) bit. User can measure the output of the OP amplifier through the integrated A/D converter.

6.18.2 Features

- Analog input voltage range: 0~AV_{DD}
- Supports two analog OP amplifiers
- Supports OP output voltage measurement by A/D converter
- Supports Schmitt trigger buffer outputs and generate interrupt
- OP amplifier 0 output can be an optional input source of integrated comparator 0 positive input
- OP amplifier 1 output can be an optional input source of integrated comparator 1 positive input

7.2 DC Electrical Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operation voltage	V_{DD}	2.5	-	5.5	V	V_{DD} =2.5V ~ 5.5V				
Power Ground	V_{SS}/ AV_{SS}	-0.3	-	-	V					
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} >= 2.5V				
Analog Operating Voltage	AV_{DD}	2.5	-	V_{DD}	V					
Analog Reference Voltage	V_{REF}	1.2	-	AV_{DD}	V					
Operating Current Normal Run Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD1}		38.7		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{DD2}		17.9		mA	5.5V	12MHz	X	✓	X
	I_{DD3}		37.2		mA	3.3V	12MHz	X	✓	✓
	I_{DD4}		16.4		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD5}		32.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD6}		15.5		mA	5.5V	12MHz	X	✓	X
	I_{DD7}		31.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD8}		14.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD9}		29.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD10}		14.5		mA	5.5V	12MHz	X	✓	X
	I_{DD11}		27.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD12}		13.0		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD13}		28.1		mA	5.5V	12MHz	X	✓	✓
	I_{DD14}		14.0		mA	5.5V	12MHz	X	✓	X
	I_{DD15}		26.6		mA	3.3V	12MHz	X	✓	✓
	I_{DD16}		12.5		mA	3.3V	12MHz	X	✓	X
Operating Current Normal Run Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD17}		19.9		mA	5.5V	12MHz	X	✓	✓
	I_{DD18}		10.4		mA	5.5V	12MHz	X	✓	X
	I_{DD19}		18.4		mA	3.3V	12MHz	X	✓	✓
	I_{DD20}		8.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Normal Run Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD21}		11.7		mA	5.5V	X	✓	X	✓
	I_{DD22}		5.3		mA	5.5V	X	✓	X	X
	I_{DD23}		11.6		mA	3.3V	X	✓	X	✓
	I_{DD24}		5.2		mA	3.3V	X	✓	X	X
Operating Current Normal Run Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD25}		8.6		mA	5.5V	12MHz	X	X	✓
	I_{DD26}		4.9		mA	5.5V	12MHz	X	X	X
	I_{DD27}		7.2		mA	3.3V	12MHz	X	X	✓
	I_{DD28}		3.4		mA	3.3V	12MHz	X	X	X
Operating Current Normal Run Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{DD29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{DD30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{DD31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{DD32}		0.11		mA	3.3V	X	10KHz	X	X
Operating Current Idle Mode At 72MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE1}		30.1		mA	VDD	HXT	HIRC	PLL	All digital module
						5.5V	12MHz	X	✓	✓
	I_{IDLE2}		9.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE3}		28.6		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE4}		7.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 60MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE5}		25.7		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE6}		8.2		mA	5.5V	12MHz	X	✓	X
	I_{IDLE7}		24.2		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE8}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 50MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE9}		23.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE10}		8.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE11}		21.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE12}		6.9		mA	3.3V	12MHz	X	✓	X

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
Operating Current Idle Mode At 48MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE13}		22.3		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE14}		8.1		mA	5.5V	12MHz	X	✓	X
	I_{IDLE15}		20.8		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE16}		6.7		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 32MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE17}		16.0		mA	5.5V	12MHz	X	✓	✓
	I_{IDLE18}		6.4		mA	5.5V	12MHz	X	✓	X
	I_{IDLE19}		14.5		mA	3.3V	12MHz	X	✓	✓
	I_{IDLE20}		4.9		mA	3.3V	12MHz	X	✓	X
Operating Current Idle Mode At 22.1184MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE21}		8.6		mA	5.5V	X	✓	X	✓
	I_{IDLE22}		2.2		mA	5.5V	X	✓	X	X
	I_{IDLE23}		8.6		mA	3.3V	X	✓	X	✓
	I_{IDLE24}		2.2		mA	3.3V	X	✓	X	X
Operating Current Idle Mode At 12MHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE25}		7.2		mA	5.5V	12MHz	X	X	✓
	I_{IDLE26}		3.4		mA	5.5V	12MHz	X	X	X
	I_{IDLE27}		5.7		mA	3.3V	12MHz	X	X	✓
	I_{IDLE28}		1.9		mA	3.3V	12MHz	X	X	X
Operating Current Idle Mode At 10kHz while(1){} executed from flash V_{LDO} =1.8V	I_{IDLE29}		0.13		mA	VDD	HXT/ LXT	LIRC	PLL	All digital module
						5.5V	X	10KHz	X	✓
	I_{IDLE30}		0.12		mA	5.5V	X	10KHz	X	X
	I_{IDLE31}		0.11		mA	3.3V	X	10KHz	X	✓
	I_{IDLE32}		0.11		mA	3.3V	X	10KHz	X	X
Standby Current Power-down Mode	I_{PWD1}		-		µA	VDD	HXT	HIRC	LIRC	All digital module
						5.5V	✓	X	X	X
	I_{PWD2}		-		µA	5.5V	X	✓	X	X
	I_{PWD3}		-		µA	5.5V	X	X	✓	X
	I_{PWD4}		-		µA	3.3V	✓	X	X	X
	I_{PWD5}		-		µA	3.3V	X	✓	X	X

7.4.3 Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Quiescent Current	AV_{DD}=5.5 V	-	1	5	μA
Operation Temperature	-	-40	25	105	℃
Threshold Voltage	-	1.6	2.0	2.4	V
Hysteresis	-	0	0	0	V

7.4.4 Brown-out Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Voltage	-	0	-	5.5	V
Temperature	-	-40	25	105	℃
Quiescent Current	AV_{DD}=5.5 V	-	-	125	μA
Brown-out Voltage	BOD_VL[1:0]=11	4.2	4.4	4.6	V
	BOD_VL [1:0]=10	3.5	3.7	3.9	V
	BOD_VL [1:0]=01	2.6	2.7	2.8	V
	BOD_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.5 Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Temperature	-	-40	25	105	℃
Reset Voltage	V+	-	2	-	V
Quiescent Current	Vin > reset voltage	-	1	-	nA

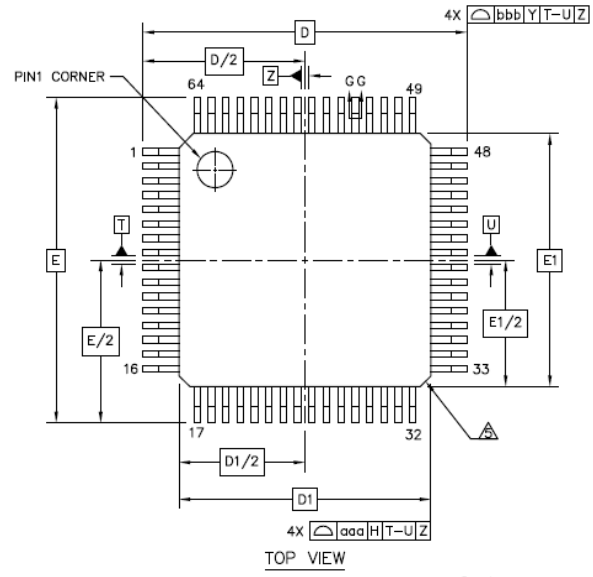
7.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		10000			cycles[1]
T_{RET}	Data Retention	At 25℃	100			year
T_{ERASE}	Page Erase Time			20		ms
T_{MER}	Mass Erase Time			40		ms
T_{PROG}	Program Time			40		μs
I_{DD1}	Read Current		-	0.15	0.5	mA/MHz
I_{DD2}	Program/Erase Current				7	mA

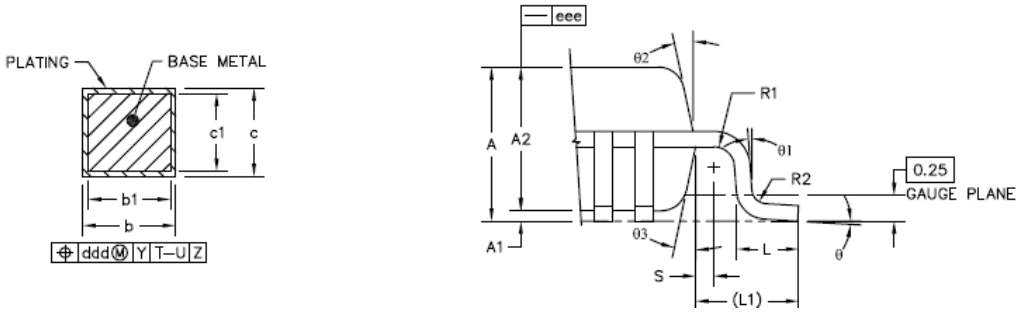
Note : This table is guaranteed by design, not test in production.

[1] Number of program/erase cycles.
[2] V_{DD} is source from chip LDO output voltage.

8.2 LQFP 64S (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



9 REVISION HISTORY

Date	Revision	Description
2015.06.11	1.00	Preliminary version.
2015.07.31	1.01	Added “Flash DC Electrical Characteristics” in section 7.5.