NXP USA Inc. - MCF52252AF80 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52252af80

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1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz[1]		up to 80 MHz[1]	up to 66 or 80 MHz[1]		up to 80 MHz[1]
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

[1] 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

  - DMA or FIFO data stream interfaces
  - Low power consumption
  - OTG protocol logic
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- Mini-FlexBus
  - External bus interface available on 144 pin packages
  - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
  - 2 chip selects ($\overline{\text{FB\_CS}}$[1:0])
  - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
  - Multiplexed mode: 16-bit data and 20-bit address bus
  - FB_CLK output to support synchronous memories
  - Programmable base address, size, and wait states to support slow peripherals
  - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I2C modules
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($0 \le n \le 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O on 100-pin package
  - Up to 96 bits of general purpose I/O on 144-pin package
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.24 Interrupt Controllers (INTC*n*)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR*n*[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

Figure 3 shows the pinout configuration for the 100 LQFP.

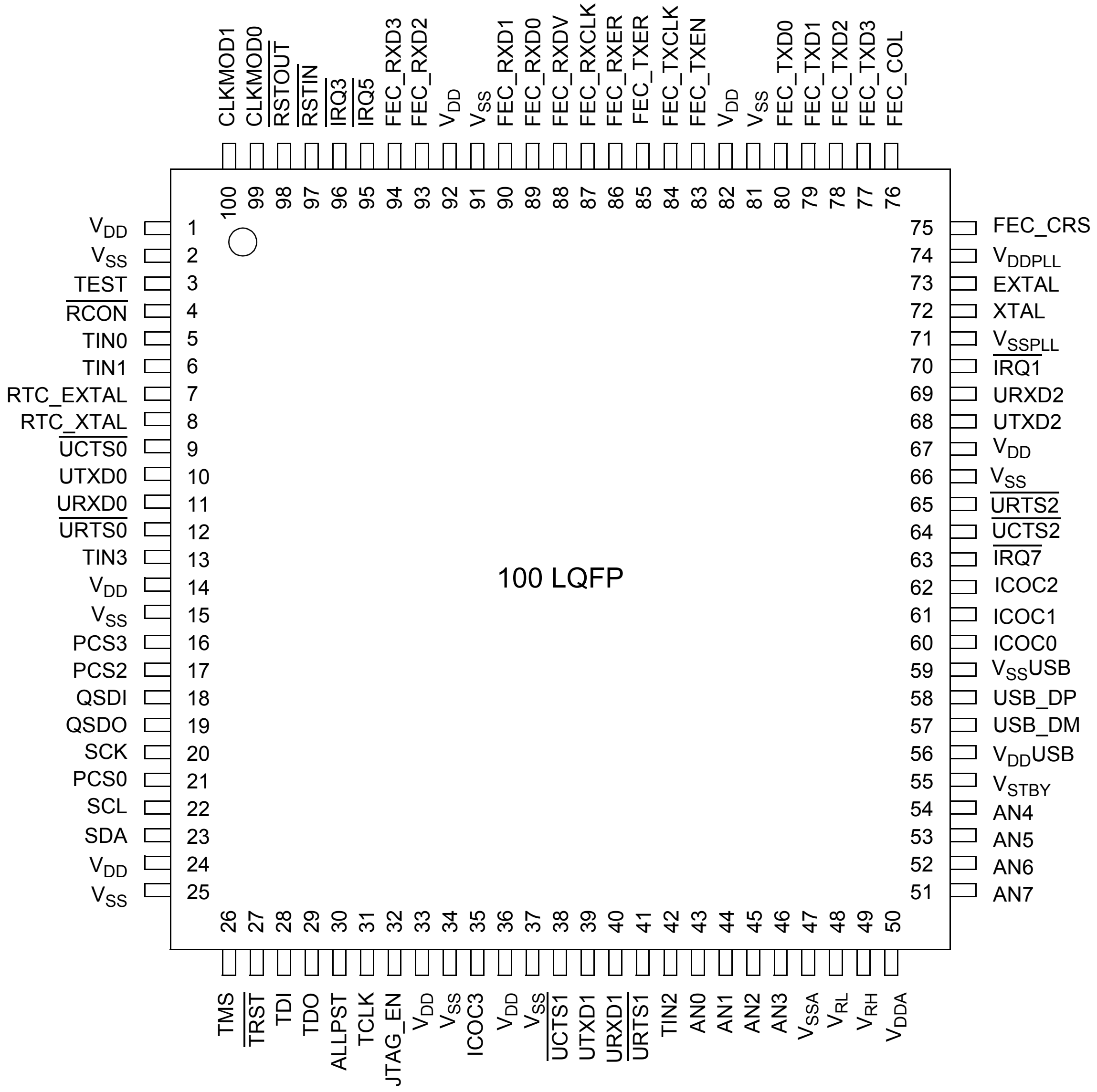
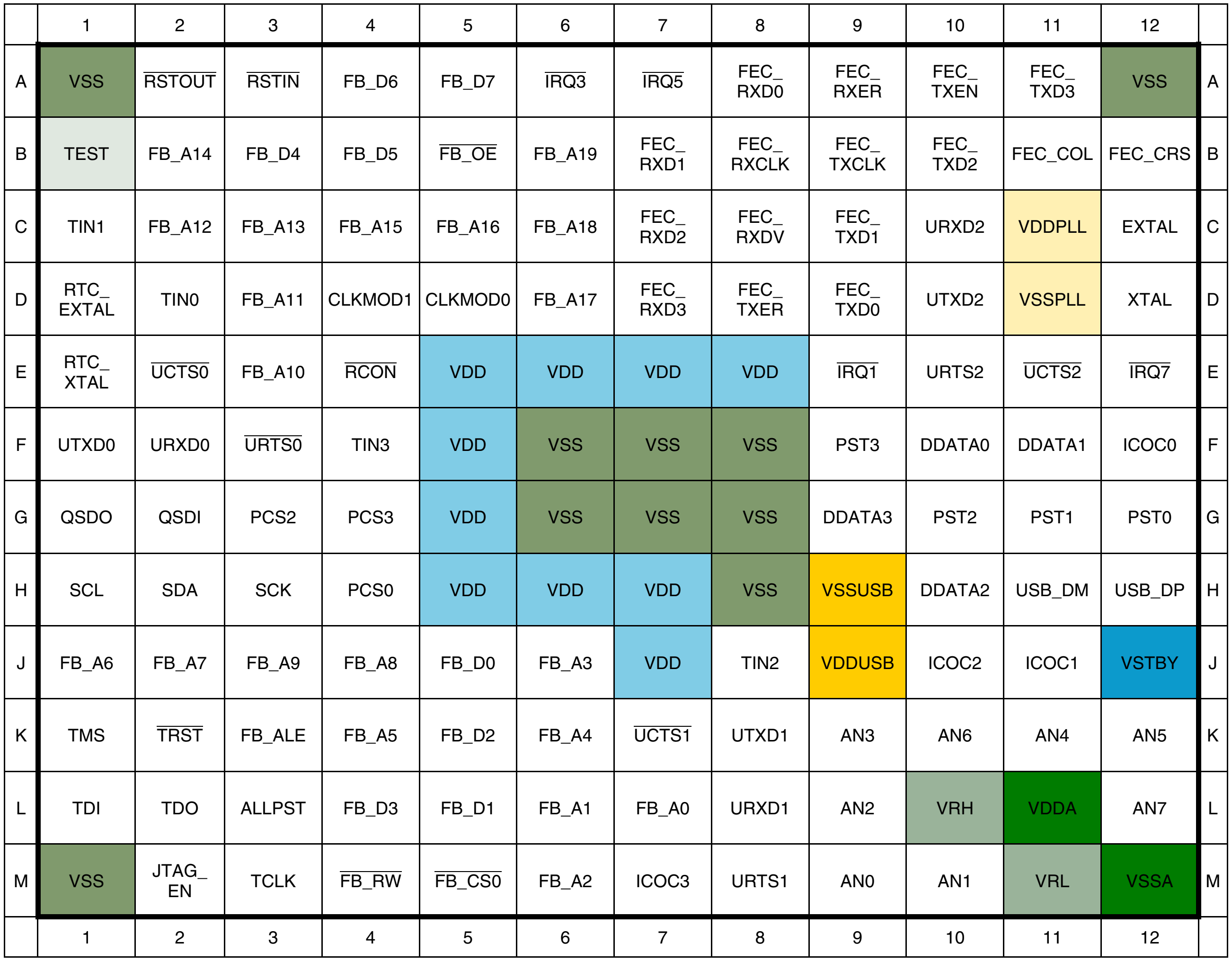


Figure 3. 100 LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 144 MAPBGA.



	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	$\overline{\text{RSTOUT}}$	$\overline{\text{RSTIN}}$	FB_D6	FB_D7	$\overline{\text{IRQ3}}$	$\overline{\text{IRQ5}}$	FEC_RXD0	FEC_RXER	FEC_TXEN	FEC_TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	$\overline{\text{FB\_OE}}$	FB_A19	FEC_RXD1	FEC_RXCLK	FEC_TXCLK	FEC_TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_RXD2	FEC_RXDV	FEC_TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_RXD3	FEC_TXER	FEC_TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_XTAL	$\overline{\text{UCTS0}}$	FB_A10	$\overline{\text{RCON}}$	VDD	VDD	VDD	VDD	$\overline{\text{IRQ1}}$	URTS2	$\overline{\text{UCTS2}}$	$\overline{\text{IRQ7}}$	E
F	UTXD0	URXD0	$\overline{\text{URTS0}}$	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	$\overline{\text{TRST}}$	FB_ALE	FB_A5	FB_D2	FB_A4	$\overline{\text{UCTS1}}$	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_EN	TCLK	$\overline{\text{FB\_RW}}$	$\overline{\text{FB\_CS0}}$	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
ADC	AN[7:0]	—	—	PAN[7:0]	Low	Low	—	L12, K10, K12, K11, K9, L9, M10, M9	74–77; 69, 68, 67 ,66	51–54, 46, 45, 44, 43
	VDDA	—	—	—	N/A	N/A	—	L11	73	50
	VSSA	—	—	—	N/A	N/A	—	M12	70	47
	VRH	—	—	—	N/A	N/A	—	L10	72	49
	VRL	—	—	—	N/A	N/A	—	M11	71	48
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	C12	106	73
	XTAL	—	—	—	N/A	N/A	—	D12	105	72
	VDDPLL	—	—	—	N/A	N/A	—	C11	107	74
	VSSPLL	—	—	—	N/A	N/A	—	D11	104	71
RTC	RTC_EXTAL	—	—	—	N/A	N/A	—	D1	13	7
	RTC_XTAL	—	—	—	N/A	N/A	—	E1	14	8
Debug Data	ALLPST	—	—	—	Low	High	—	L3	42	30
	DDATA[3:0]	—	—	PDD[7:4]	Low	High	—	G9, H10, F11, F10	86, 85, 84, 83	—
	PST[3:0]	—	—	PDD[3:0]	Low	High	—	F9, G10, G11, G12	87–90	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Timer 1, 32-bit	DTIN1	DTOUT1	PWM2	PTC1	PSRR[17]	PDSR[17]	—	C1	12	6
Timer 0, 32-bit	DTIN0	DTOUT0	PWM0	PTC0	PSRR[16]	PDSR[16]	—	D2	11	5
UART 0	UCTS0	—	USB_VBUSE	PUA3	PSRR[11]	PDSR[11]	—	E2	15	9
	URTS0	—	USB_VBUSD	PUA2	PSRR[10]	PDSR[10]	—	F3	18	12
	URXD0	—	—	PUA1	PSRR[9]	PDSR[9]	—	F2	17	11
	UTXD0	—	—	PUA0	PSRR[8]	PDSR[8]	—	F1	16	10
UART 1	UCTS1	SYNCA	URXD2	PUB3	PSRR[15]	PDSR[15]	—	K7	61	38
	URTS1	SYNCB	UTXD2	PUB2	PSRR[14]	PDSR[14]	—	M8	64	41
	URXD1	I2C_SDA1	—	PUB1	PSRR[13]	PDSR[13]	Pull-Up[6]	L8	63	40
	UTXD1	I2C_SCL1	—	PUB0	PSRR[12]	PDSR[12]	Pull-Up[6]	K8	62	39
UART 2	UCTS2	I2C_SCL1	USB_ VBUSCHG	PUC3	PSRR[27]	PDSR[27]	Pull-Up[6]	E11	97	64
	URTS2	I2C_SDA1	USB_ VBUSDIS	PUC2	PSRR[26]	PDSR[26]	Pull-Up[6]	E10	98	65
	URXD2	CANRX	—	PUC1	PSRR[25]	PDSR[25]	—	C10	102	69
	UTXD2	CANTX	—	PUC0	PSRR[24]	PDSR[24]	—	D10	101	68
USB OTG	USB_DM	—	—	—	N/A	N/A	—	H11	80	57
	USB_DP	—	—	—	N/A	N/A	—	H12	81	58
	USB_VDD	—	—	—	N/A	N/A	—	J9	79	56
	USB_VSS	—	—	—	N/A	N/A	—	H9	82	59

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins)[4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A (T_L - T_H)	–40 to 85 or 0 to 70[6]	°C
Storage temperature range	T_{stg}	–65 to 150	°C

[1] Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

[2] This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

[3] Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[4] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[5] The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

[6] Depending on the packaging; see orderable part number summary (Table 2)

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[13,14]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,15]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board	—	θ_{JB}	25[16]	°C/W
	Junction to case	—	θ_{JC}	9[17]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[18]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

[1] θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

[2] Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

[3] Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

[4] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

[7] θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

[8] Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

[9] Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

[10] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[11] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[12] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

[13] θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

[14] Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

[15] Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

2.9 USB Operation

Table 15. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys\_USB\_min}$	16	MHz

2.10 Mini-FlexBus External Interface Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 16. Mini-FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	—	80	MHz	
MB1	Clock Period	12.5	—	ns	
MB2	Output Valid	—	8	ns	[1]
MB3	Output Hold	2	—	ns	[1]
MB4	Input Setup	6	—	ns	[2]
MB5	Input Hold	0	—	ns	[2]

[1] Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

[2] Specification is valid for all MB_D[7:0].

2.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 17. Receive Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	RXCLK frequency	—	25	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	ns
E3	RXCLK pulse width high	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	RXCLK period

[1] In MII mode, n = 3

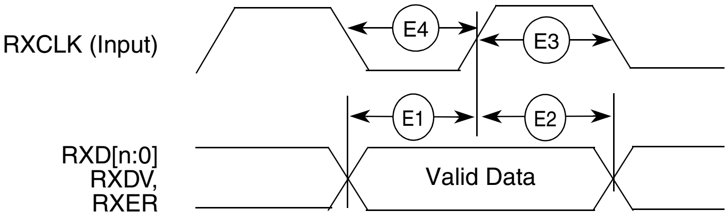


Figure 7. MII Receive Signal Timing Diagram

2.11.2 Transmit Signal Timing Specifications

Table 18. Transmit Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	TXCLK frequency	—	25	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	ns
E7	TXCLK pulse width high	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	t_{TXCLK}

[1] In MII mode, n = 3

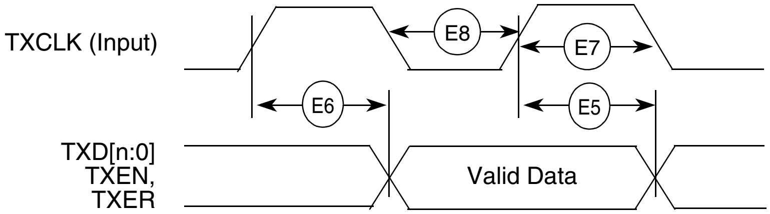


Figure 8. MII Transmit Signal Timing Diagram

2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

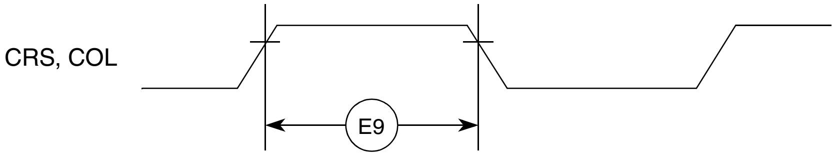


Figure 9. MII Async Inputs Timing Diagram

2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

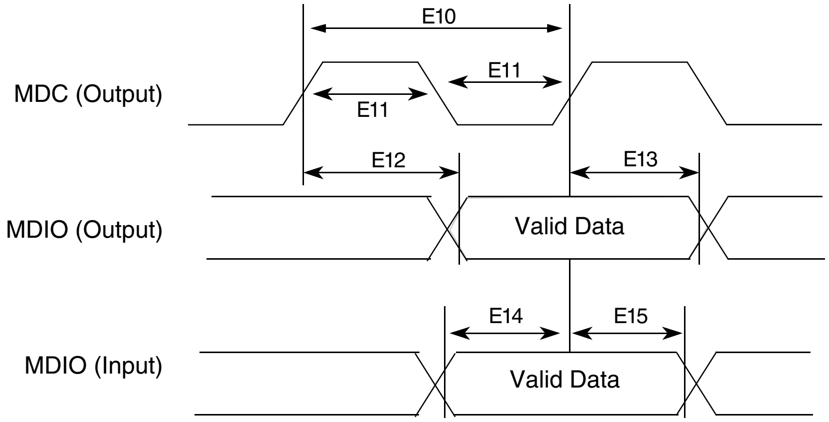


Figure 10. MII Serial Management Channel TIming Diagram

2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 21 and Figure 11.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

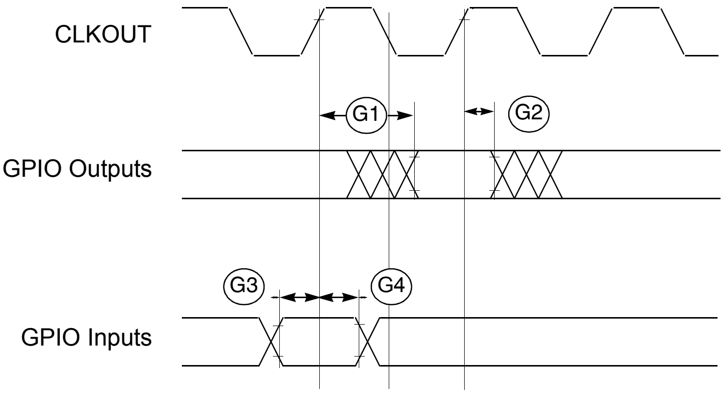


Figure 11. GPIO Timing

2.13 Reset Timing

Table 22. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

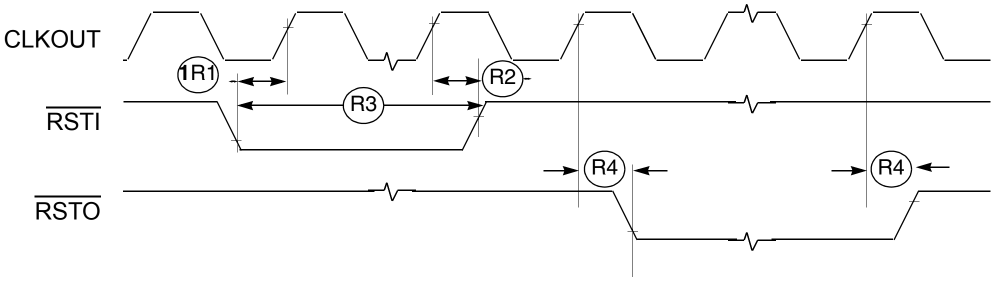


Figure 12. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.14 I2C Input/Output Timing Specifications

Table 23 lists specifications for the I2C input timing parameters shown in Figure 13.

Table 23. I2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time ($V_{IL} = 0.5$ V to $V_{IH} = 2.4$ V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4$ V to $V_{IL} = 0.5$ V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 24 lists specifications for the I2C output timing parameters shown in Figure 13.

Table 24. I2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time ($V_{IL} = 0.5$ V to $V_{IH} = 2.4$ V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time ($V_{IH} = 2.4$ V to $V_{IL} = 0.5$ V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

[1] Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

[2] Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

[3] Specified at a nominal 50 pF load.

2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

Table 26. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	3 × t_{CYC}	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	1 × t_{CYC}	—	ns

[1] All timing references to CLKOUT are given to its rising edge.

2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

Table 27. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.

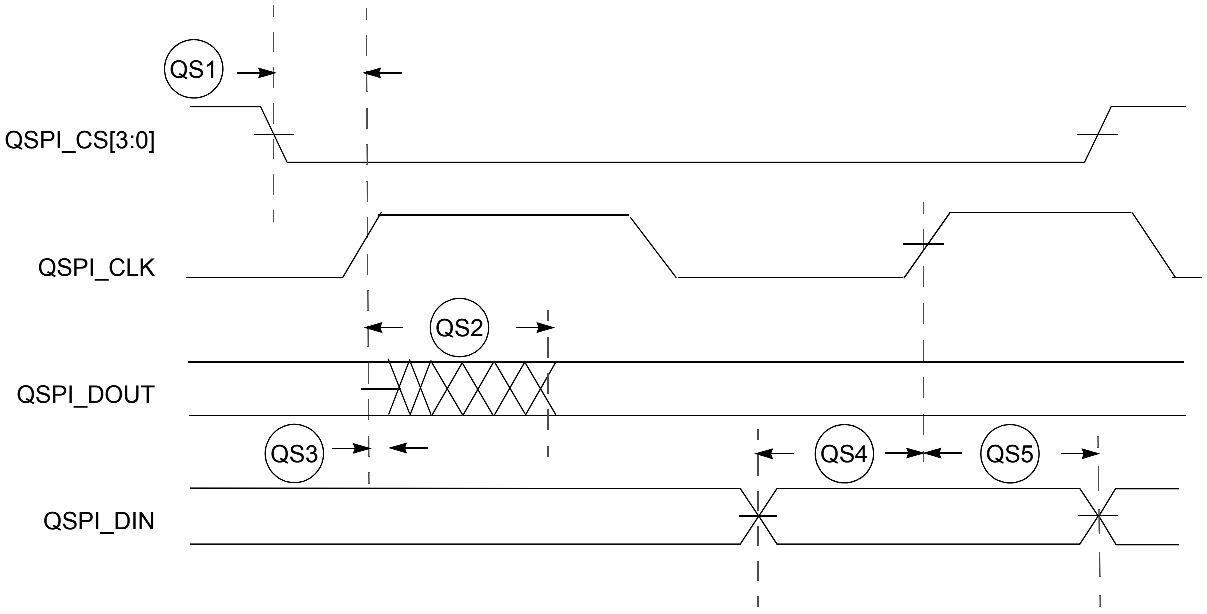


Figure 15. QSPI Timing

2.19 JTAG and Boundary Scan Timing

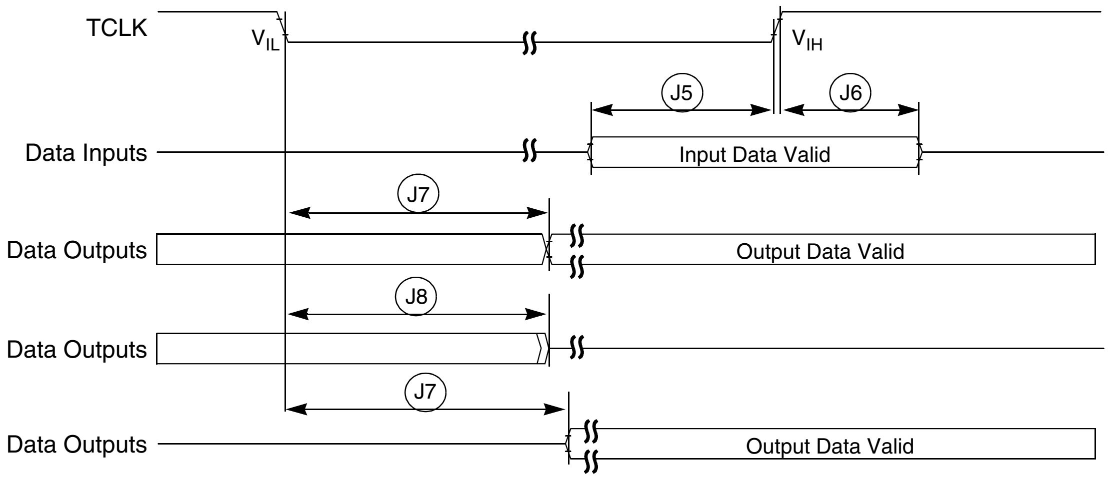


Figure 17. Boundary Scan (JTAG) Timing

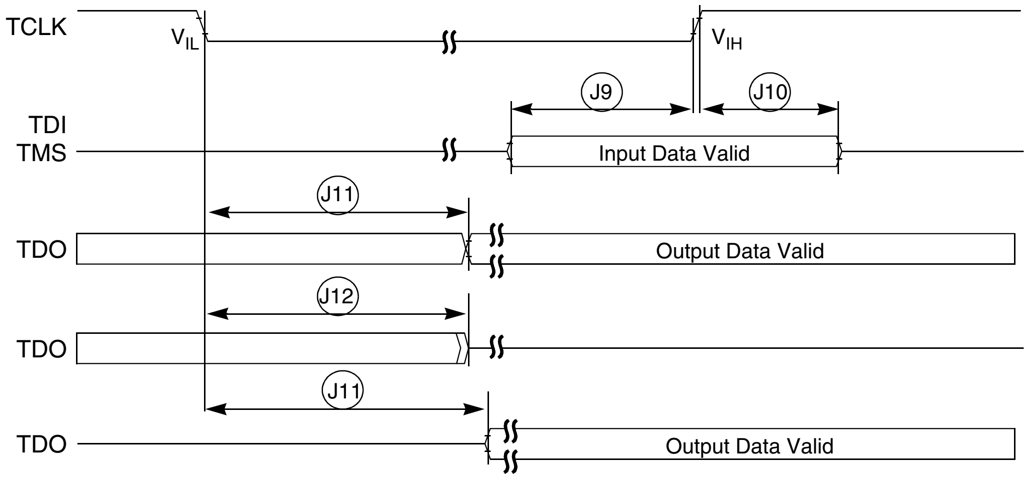


Figure 18. Test Access Port Timing

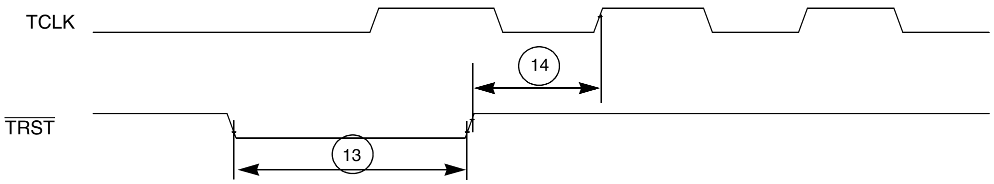


Figure 19. $\overline{\text{TRST}}$ Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

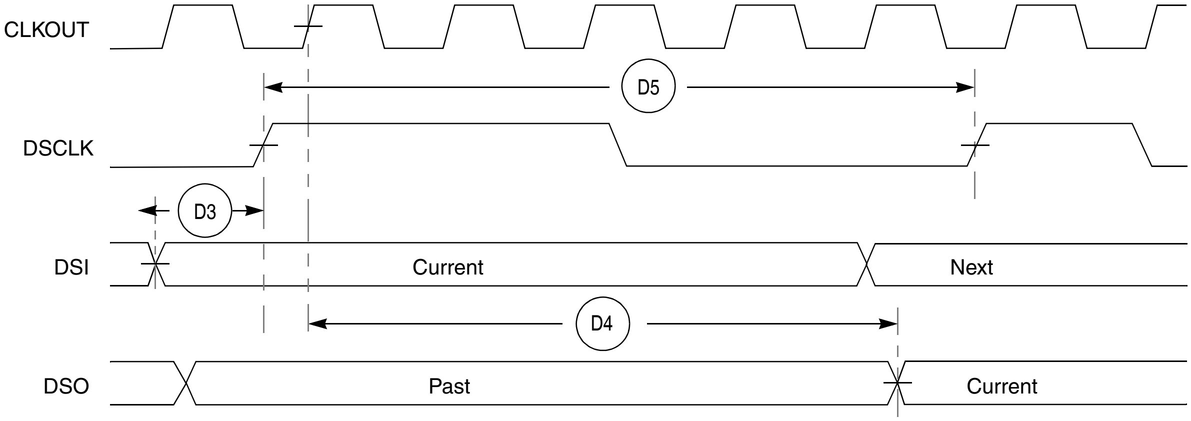


Figure 21. BDM Serial Port AC Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W 98ASH70694A
MCF52258		
MCF52259		

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