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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mcf52252caf66">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mcf52252caf66</a>

## 1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

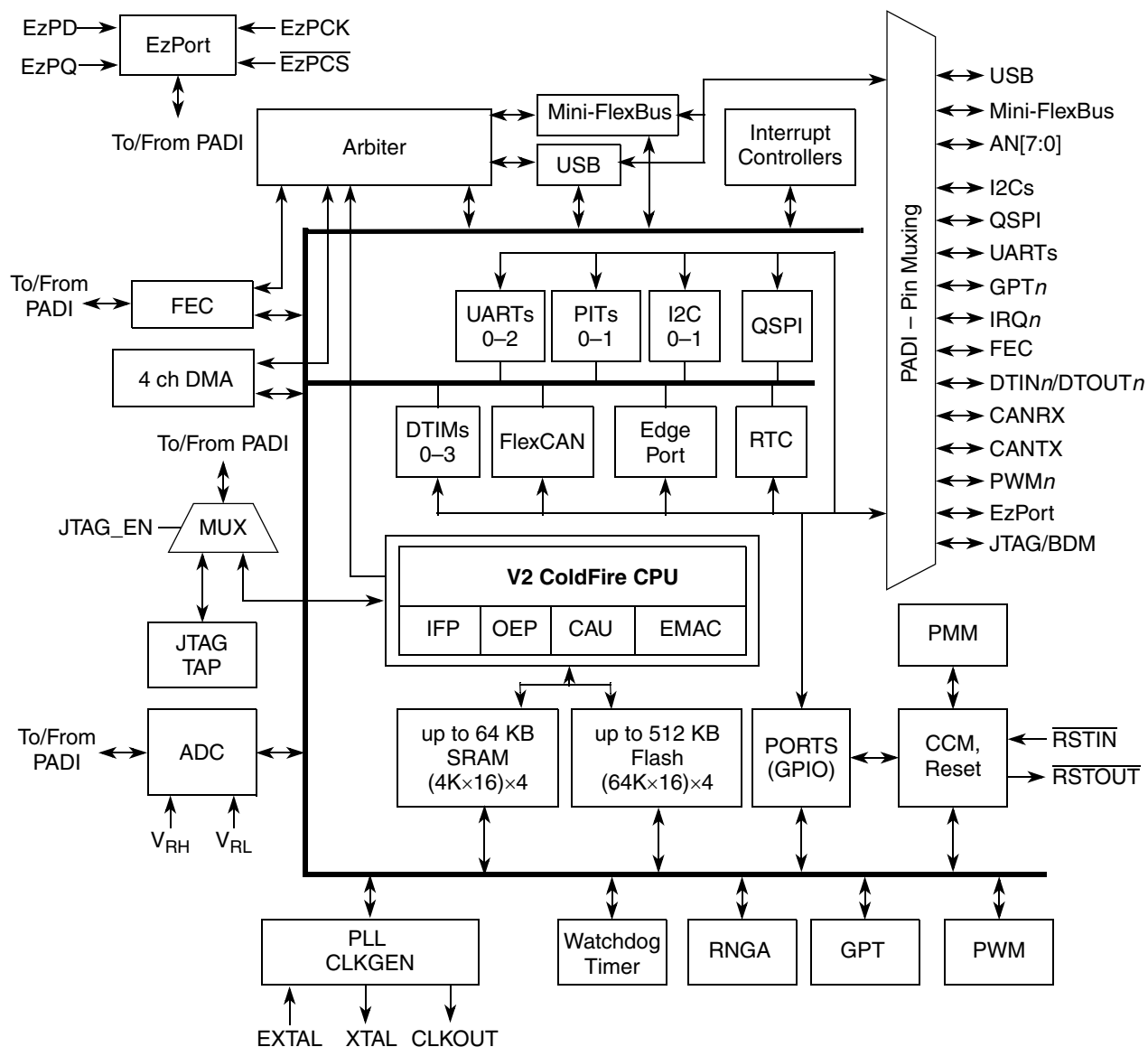


Figure 1. MCF52259 Block Diagram

## 1.2 Features

### 1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip

## Family Configurations

- Up to 80 MHz processor core frequency
- 40 MHz or 33 MHz peripheral bus frequency
- Sixteen general-purpose, 32-bit data and address registers
- Implements ColdFire ISA\_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA\_A+)
- Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support  $16 \times 16 \rightarrow 32$  or  $32 \times 32 \rightarrow 48$  operations
- Cryptographic Acceleration Unit (CAU)
  - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
  - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG\_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
  - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/s
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points

- DMA or FIFO data stream interfaces
- Low power consumption
- OTG protocol logic
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- Mini-FlexBus
  - External bus interface available on 144 pin packages
  - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
  - 2 chip selects ( $\overline{\text{FB\_CS}}[1:0]$ )
  - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
  - Multiplexed mode: 16-bit data and 20-bit address bus
  - $\text{FB\_CLK}$  output to support synchronous memories
  - Programmable base address, size, and wait states to support slow peripherals
  - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I2C modules
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125  $\mu\text{s}$  conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

## Family Configurations

- Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
  - 12.5 ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse-widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
  - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Backup watchdog timer (BWT)
  - Independent timer that can be used to help software recover from runaway code
  - 16-bit counter
  - Low-power mode support
- Clock generation features
  - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

### 1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

### 1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

### 1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

### 1.2.24 Interrupt Controllers (INTC<sub>n</sub>)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

### 1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR<sub>n</sub>[START] bit or by the occurrence of certain UART or DMA timer events.

### 1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the  $\overline{\text{RSTO}}$  pin.

## 1.2.27 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

## 1.2.28 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at [freescale.com](http://freescale.com) or contact your sales office for up-to-date RoHS information.

**Table 2. Orderable part number summary**

Freescal Part Number	FlexCAN	Encryption	Speed (MHz)	Flash (KB)	SRAM (KB)	Package	Temp range (°C)
MCF52252AF80	—	—	80	256	32	100 LQFP	0 to +70
MCF52252CAF66	•	—	66				-40 to +85
MCF52254AF80	—	—	80	512	64	100 LQFP	0 to +70
MCF52254CAF66	•	—	66				-40 to +85
MCF52255CAF80	•	•	80	512	64	100 LQFP	-40 to +85
MCF52256AG80	—	—	80	256	32	144 LQFP	0 to +70
MCF52256CAG66	•	—	66		64		-40 to +85
MCF52256CVN66	•	—	66		64	144 MAPBGA	-40 to +85
MCF52256VN80	—	—	80		32		0 to +70
MCF52258AG80	—	—	80	512	64	144 LQFP	0 to +70
MCF52258CAG66	•	—	66				-40 to +85
MCF52258CVN66	•	—	66			144 MAPBGA	-40 to +85
MCF52258VN80	—	—	80				0 to +70
MCF52259CAG80	•	•	80	512	64	144 LQFP	-40 to +85
MCF52259CVN80	•	•				144 MAPBGA	-40 to +85

Figure 2 shows the pinout configuration for the 144 LQFP.

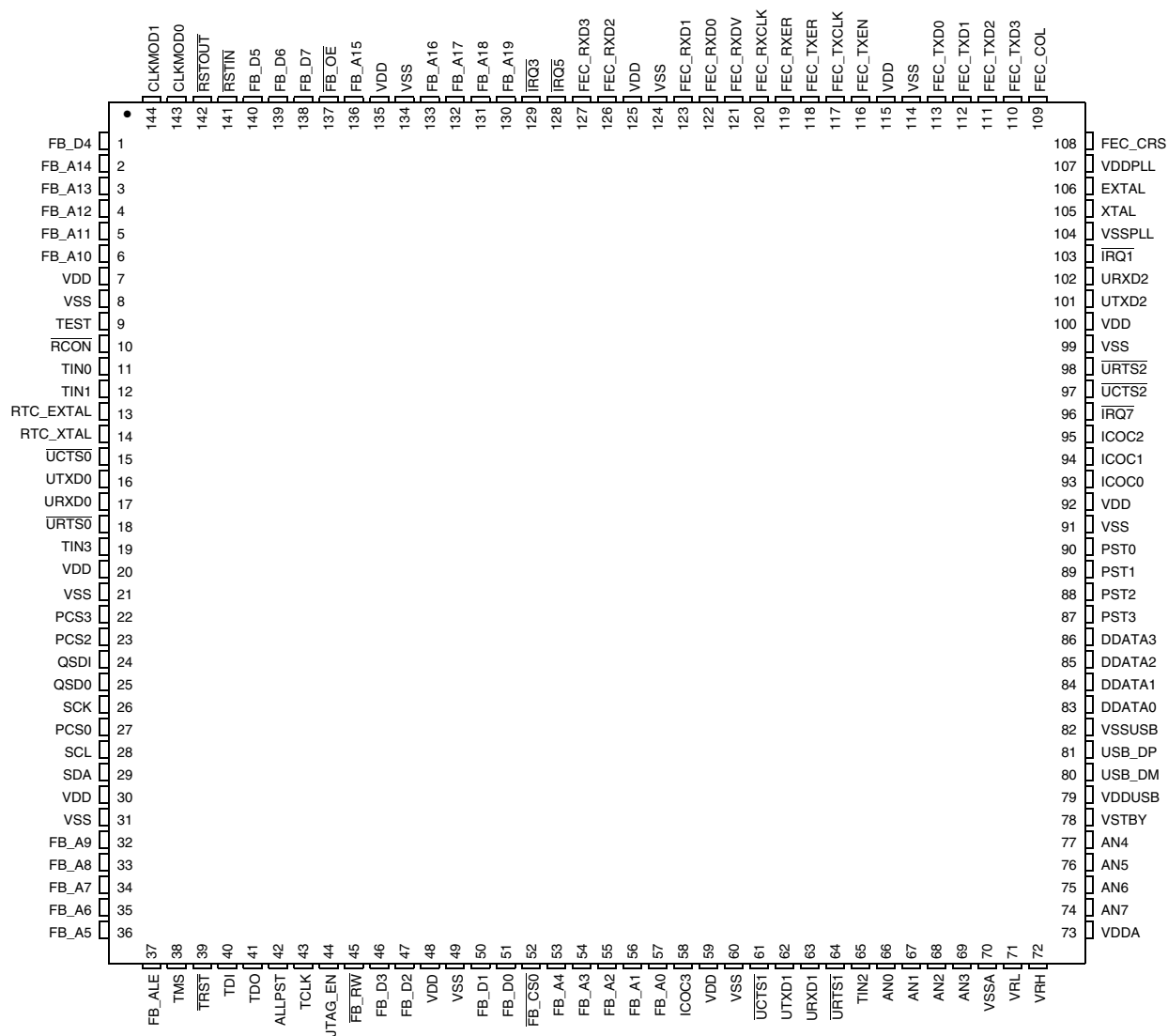




Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_RXD0	FEC_RXER	FEC_TXEN	FEC_TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_RXD1	FEC_RXCLK	FEC_TXCLK	FEC_TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_RXD2	FEC_RXDV	FEC_TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_RXD3	FEC_TXER	FEC_TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control <sup>1</sup>	Pull-up/ Pull-down <sup>2</sup>	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0 <sup>3</sup>	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up <sup>4</sup>	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up <sup>4</sup>	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up <sup>4</sup>	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up <sup>4</sup>	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up <sup>4</sup>	A6	129	96
	IRQ1	—	USB_ALT CLK	PNQ1	Low	High	Pull-Up <sup>4</sup>	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up <sup>5</sup>	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up <sup>5</sup>	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/BKPT	—	—	—	N/A	N/A	Pull-Up <sup>5</sup>	K1	38	26
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up <sup>5</sup>	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control <sup>1</sup>	Pull-up/ Pull-down <sup>2</sup>	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mini-FlexBus <sup>9</sup>	FB_ALE	FB_CS1	—	PAS2	PSRRL[20]	PDSRL[20]	—	K3	37	—
	FB_AD[7:0]	—	—	PTE[7:0]	PSRRL[7:0]	PDSRL[7:0]	—	J2, J1, K4, K6, J6, M6, L6, L7	34–36; 53–57	—
	FB_AD[15:8]	—	—	PTF[7:0]	PSRRL[15:8]	PDSRL[15:8]	—	C4, B2, C3, C2, D3, E3, J3, J4	136, 2–6, 32–33	—
	FB_AD[19:16]	—	—	PTG[3:0]	PSRRL[19:16]	PDSRL[19:16]	—	B6, C6, D6, C5	130–133	—
	FB_CS0	—	—	PTG5	PSRRL[21]	PDSRL[21]	—	M5	52	—
	FB_R/ $\overline{W}$	—	—	PTG7	PSRRL[31]	PDSRL[31]	—	M4	45	—
	FB_OE	—	—	PTG6	PSRRL[30]	PDSRL[30]	—	B5	137	—
	FB_D7	CANRX	—	PTH5	PSRRL[29]	PDSRL[29]	—	A5	138	—
	FB_D6	CANTX	—	PTH4	PSRRL[28]	PDSRL[28]	—	A4	139	—
	FB_D5	I2C_SCL1	—	PTH3	PSRRL[27]	PDSRL[27]	Pull-Up <sup>6</sup>	B4	140	—
	FB_D4	I2C_SDA1	—	PTH2	PSRRL[26]	PDSRL[26]	Pull-Up <sup>6</sup>	B3	1	—
	FB_D3	USB_VBUS <sub>D</sub>	—	PTH1	PSRRL[25]	PDSRL[25]	—	L4	46	—
	FB_D2	USB_VBU <sub>SE</sub>	—	PTH0	PSRRL[24]	PDSRL[24]	—	K5	47	—
	FB_D1	SYNCA	—	PTH7	PSRRL[23]	PDSRL[23]	—	L5	50	—
	FB_D0	SYNCB	—	PTH6	PSRRL[22]	PDSRL[22]	—	J5	51	—
Standby Voltage	VSTBY	—	—	—	N/A	N/A	—	J12	78	55
VDD <sup>10</sup>	VDD	—	—	—	N/A	N/A	—	E5–E8; F5; G5; H5–7; J7	7; 20; 30; 48; 59; 92; 100; 115; 125; 135	1; 14; 24; 33; 36; 67; 82; 92

**Table 7. Current Consumption in Low-Power Mode, Code From SRAM<sup>1,2,3</sup>**

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11) <sup>4</sup>	0.090				mA	I <sub>DD</sub>
Stop mode 2 (Stop 10) <sup>4</sup>	7					
Stop mode 1 (Stop 01) <sup>4,5</sup>	9	10	15	17		
Stop mode 0 (Stop 00) <sup>5</sup>	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

<sup>1</sup> All values are measured with a 3.3 V power supply. Tests performed at room temperature.

<sup>2</sup> Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.

<sup>3</sup> CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.

<sup>4</sup> See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.

<sup>5</sup> Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

## 2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

**Table 8. Thermal Characteristics**

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	$\theta_{JA}$	53 <sup>1,2</sup>	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JA}$	30 <sup>1,3</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	$\theta_{JMA}$	43 <sup>1,3</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	$\theta_{JMA}$	26 <sup>1,3</sup>	°C/W
	Junction to board	—	$\theta_{JB}$	16 <sup>4</sup>	°C/W
	Junction to case	—	$\theta_{JC}$	9 <sup>5</sup>	°C/W
	Junction to top of package	Natural convection	$\Psi_{jt}$	2 <sup>6</sup>	°C/W
	Maximum operating junction temperature	—	$T_j$	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	$\theta_{JA}$	44 <sup>7,8</sup>	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JA}$	35 <sup>1,9</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	$\theta_{JMA}$	35 <sup>1,3</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	$\theta_{JMA}$	29 <sup>1,3</sup>	°C/W
	Junction to board	—	$\theta_{JB}$	23 <sup>10</sup>	°C/W
	Junction to case	—	$\theta_{JC}$	7 <sup>11</sup>	°C/W
	Junction to top of package	Natural convection	$\Psi_{jt}$	2 <sup>12</sup>	°C/W
	Maximum operating junction temperature	—	$T_j$	105	°C

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	$\theta_{JA}$	53 <sup>13,14</sup>	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	$\theta_{JA}$	39 <sup>1,15</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	$\theta_{JMA}$	42 <sup>1,3</sup>	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	$\theta_{JMA}$	33 <sup>1,3</sup>	°C/W
	Junction to board	—	$\theta_{JB}$	25 <sup>16</sup>	°C/W
	Junction to case	—	$\theta_{JC}$	9 <sup>17</sup>	°C/W
	Junction to top of package	Natural convection	$\Psi_{jt}$	2 <sup>18</sup>	°C/W
	Maximum operating junction temperature	—	$T_j$	105	°C

<sup>1</sup>  $\theta_{JA}$  and  $\Psi_{jt}$  parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

<sup>2</sup> Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

<sup>3</sup> Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

<sup>4</sup> Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>5</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

<sup>7</sup>  $\theta_{JA}$  and  $\Psi_{jt}$  parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

<sup>8</sup> Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

<sup>9</sup> Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

<sup>10</sup> Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

<sup>11</sup> Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

<sup>12</sup> Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

<sup>13</sup>  $\theta_{JA}$  and  $\Psi_{jt}$  parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of  $\theta_{JA}$  and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the  $\Psi_{jt}$  parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

<sup>14</sup> Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

<sup>15</sup> Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

## 2.8 Clock Source Electrical Specifications

**Table 14. Oscillator and PLL Specifications**
 $(V_{DD} \text{ and } V_{DDPLL} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$ 

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External <sup>1</sup>	$f_{\text{crystal}}$ $f_{\text{ext}}$	12 0	25.0 <sup>2</sup> 66.67 or 80	MHz
PLL reference frequency range	$f_{\text{ref\_pll}}$	2	10.0	MHz
System frequency <sup>3</sup> • External clock mode • On-chip PLL frequency	$f_{\text{sys}}$	0 $f_{\text{ref}} / 32$	66.67 or 80 <sup>4</sup> 66.67 or 80 <sup>4</sup>	MHz
Loss of reference frequency <sup>5, 7</sup>	$f_{\text{LOR}}$	100	1000	kHz
Self clocked mode frequency <sup>6</sup>	$f_{\text{SCM}}$	1	5	MHz
Crystal start-up time <sup>7, 8</sup>	$t_{\text{cst}}$	—	0.1	ms
EXTAL input high voltage • External reference	$V_{\text{IHEXT}}$	2.0	3.0 <sup>2</sup>	V
EXTAL input low voltage • External reference	$V_{\text{ILEXT}}$	$V_{\text{SS}}$	0.8	V
PLL lock time <sup>4,9</sup>	$t_{\text{lpll}}$	—	500	μs
Duty cycle of reference <sup>4</sup>	$t_{\text{dc}}$	40	60	% $f_{\text{ref}}$
Frequency un-LOCK range	$f_{\text{UL}}$	−1.5	1.5	% $f_{\text{ref}}$
Frequency LOCK range	$f_{\text{LCK}}$	−0.75	0.75	% $f_{\text{ref}}$
CLKOUT period jitter <sup>4, 5, 10, 11</sup> , measured at $f_{\text{SYS}}$ Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	$C_{\text{jitter}}$	— —	10 .01	% $f_{\text{sys}}$
On-chip oscillator frequency	$f_{\text{oco}}$	7.84	8.16	MHz

<sup>1</sup> In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

<sup>2</sup> This value has been updated.

<sup>3</sup> All internal registers retain data at 0 Hz.

<sup>4</sup> Depending on packaging; see the orderable part number summary (Table 2).

<sup>5</sup> Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

<sup>6</sup> Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below  $f_{\text{LOR}}$  with default MFD/RFD settings.

<sup>7</sup> This parameter is characterized before qualification rather than 100% tested.

<sup>8</sup> Proper PC board layout procedures must be followed to achieve specifications.

<sup>9</sup> This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

<sup>10</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{\text{sys}}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via  $V_{\text{DDPLL}}$  and  $V_{\text{SSPLL}}$  and variation in crystal oscillator frequency increase the  $C_{\text{jitter}}$  percentage for a given interval.

<sup>11</sup> Based on slow system clock of 40 MHz measured at  $f_{\text{sys}}$  max.

## 2.9 USB Operation

Table 15. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{\text{sys\_USB\_min}}$	16	MHz

## 2.10 Mini-FlexBus External Interface Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB\_CLK. The MB\_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB\_CLK). All other timing relationships can be derived from these values.

Table 16. Mini-FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	—	80	MHz	
MB1	Clock Period	12.5	—	ns	
MB2	Output Valid	—	8	ns	<sup>1</sup>
MB3	Output Hold	2	—	ns	<sup>1</sup>
MB4	Input Setup	6	—	ns	<sup>2</sup>
MB5	Input Hold	0	—	ns	<sup>2</sup>

<sup>1</sup> Specification is valid for all MB\_A[19:0], MB\_D[7:0], MB\_CS[1:0], MB\_OE, MB\_R/W, and MB\_ALE.

<sup>2</sup> Specification is valid for all MB\_D[7:0].

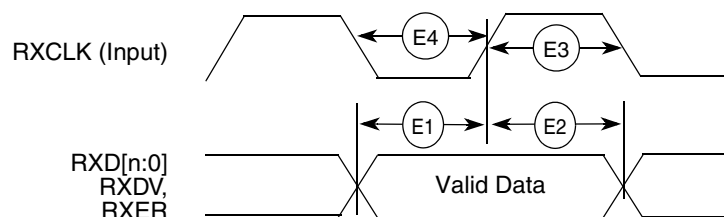
## 2.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

**Table 17. Receive Signal Timing**

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	RXCLK frequency	—	25	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup <sup>1</sup>	5	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold <sup>1</sup>	5	—	ns
E3	RXCLK pulse width high	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	RXCLK period

<sup>1</sup> In MII mode, n = 3



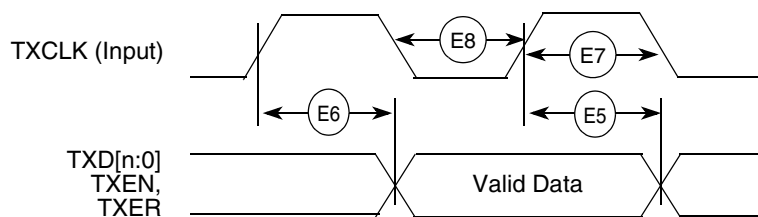
**Figure 7. MII Receive Signal Timing Diagram**

## 2.11.2 Transmit Signal Timing Specifications

**Table 18. Transmit Signal Timing**

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	TXCLK frequency	—	25	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid <sup>1</sup>	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid <sup>1</sup>	—	25	ns
E7	TXCLK pulse width high	35%	65%	t <sub>TXCLK</sub>
E8	TXCLK pulse width low	35%	65%	t <sub>TXCLK</sub>

<sup>1</sup> In MII mode, n = 3



**Figure 8. MII Transmit Signal Timing Diagram**



## 2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

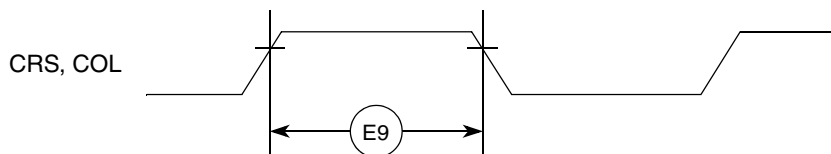


Figure 9. MII Async Inputs Timing Diagram

## 2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	$t_{MDC}$	400	—	ns
E11	MDC pulse width		40	60	% $t_{MDC}$
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

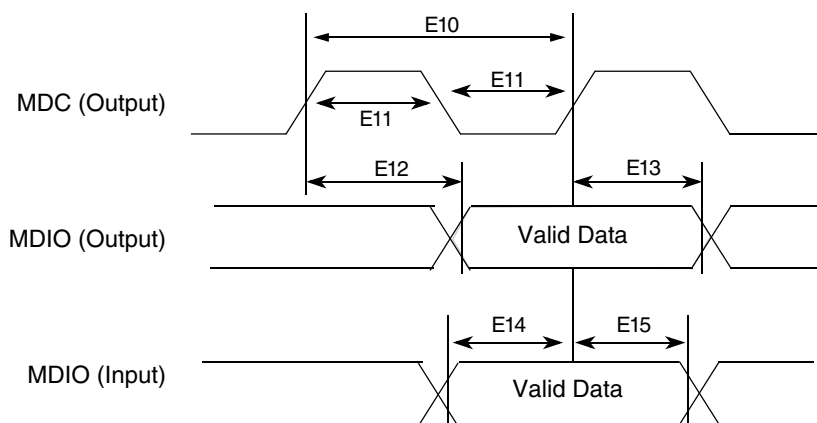


Figure 10. MII Serial Management Channel Timing Diagram

## 2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in [Table 21](#) and [Figure 11](#).

The GPIO timing is met under the following load test conditions:

- 50 pF / 50  $\Omega$  for high drive

## 2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

**Table 26. Timer Module AC Timing Specifications**

Name	Characteristic <sup>1</sup>	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

<sup>1</sup> All timing references to CLKOUT are given to its rising edge.

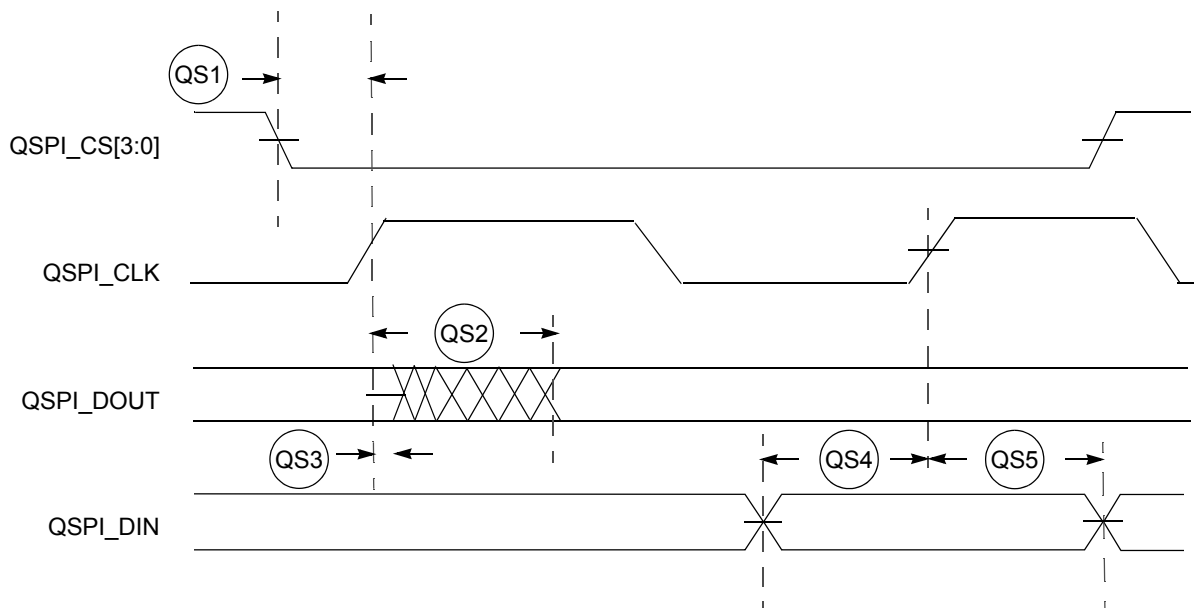
## 2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

**Table 27. QSPI Modules AC Timing Specifications**

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	$t_{CYC}$
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.



**Figure 15. QSPI Timing**

## 2.19 JTAG and Boundary Scan Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

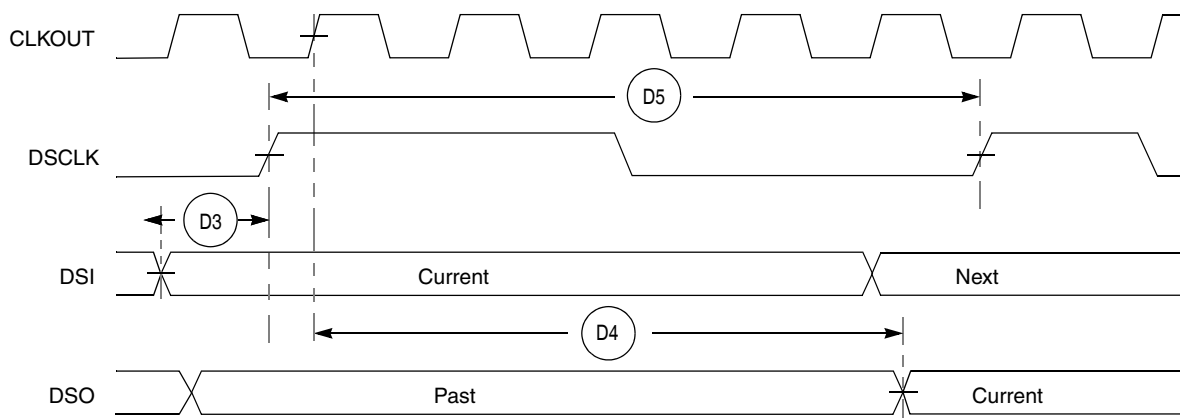


Figure 21. BDM Serial Port AC Timing

### 3 Package Information

The latest package outline drawings are available on the product summary pages on <http://www.freescale.com/coldfire>. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W
MCF52258		
MCF52259		98ASH70694A

## 4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	<ul style="list-style-type: none"> <li>Added package dimensions to package diagrams</li> <li>Added listing of devices for MCF52259 family</li> <li>Changed "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation" to "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation"</li> <li>Updated the figure <b>Pinout Top View (144 MAPBGA)</b></li> <li>Removed an extraneous instance of the table <b>Pin Functions by Primary and Alternate Purpose</b></li> <li>In the table <b>Pin Functions by Primary and Alternate Purpose</b>, changed a footnote from "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC" to "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL"</li> <li>In the table <b>SGFM Flash Program and Erase Characteristics</b>, changed "(V<sub>DDF</sub> = 2.7 to 3.6 V)" to "(V<sub>DD</sub> = 3.0 to 3.6 V)"</li> <li>In the table <b>SGFM Flash Module Life Characteristics</b>, changed "(V<sub>DDF</sub> = 2.7 to 3.6 V)" to "(V<sub>DD</sub> = 3.0 to 3.6 V)"</li> <li>In the table <b>Oscillator and PLL Specifications</b>, changed "V<sub>DD</sub> and V<sub>DDPLL</sub> = 2.7 to 3.6 V" to "V<sub>DD</sub> and V<sub>DDPLL</sub> = 3.0 to 3.6 V"</li> <li>In the table <b>Reset and Configuration Override Timing</b>, changed "V<sub>DD</sub> = 2.7 to 3.6 V" to "V<sub>DD</sub> = 3.0 to 3.6 V"</li> </ul>
2	<ul style="list-style-type: none"> <li>Added EzPort Electrical Specifications.</li> <li>Updated <a href="#">Table 2</a> for part numbers.</li> <li>In <a href="#">Table 13</a>, added slew rate column, updated derive strength, pull-up/pull-down values, JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP.</li> <li>Updated <a href="#">Table 14</a>.</li> <li>Updated <a href="#">Table 13</a>, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V).</li> <li>Updated <a href="#">Figure 2</a> for RTC_EXTAL and RTC_XTAL pin positions.</li> </ul>
3	<ul style="list-style-type: none"> <li>Updated EzPort Electrical Specifications</li> <li>Added hysteresis note in the DC electrical table</li> <li>Clarified pin function table for VSS pins.</li> <li>Clarified orderable part summary.</li> </ul>
4	<ul style="list-style-type: none"> <li>Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, "This value has been update"</li> <li>Updated crystal frequency value to 25 MHz</li> </ul>
5	<ul style="list-style-type: none"> <li>Updated TOC</li> </ul>

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