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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I ² C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52254af80

1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz ¹		up to 80 MHz ¹	up to 66 or 80 MHz ¹		up to 80 MHz ¹
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

¹ 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

Family Configurations

- Up to 80 MHz processor core frequency
- 40 MHz or 33 MHz peripheral bus frequency
- Sixteen general-purpose, 32-bit data and address registers
- Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
- Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 48$ operations
- Cryptographic Acceleration Unit (CAU)
 - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
 - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
 - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
 - Based on and includes all existing features of the Freescale TouCAN module
 - Full implementation of the CAN protocol specification version 2.0B
 - Standard data and remote frames (up to 109 bits long)
 - Extended data and remote frames (up to 127 bits long)
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
 - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
 - Unused MB space can be used as general purpose RAM space
 - Listen-only mode capability
 - Content-related addressing
 - No read/write semaphores
 - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
 - Programmable transmit-first scheme: lowest ID or lowest buffer number
 - Time stamp based on 16-bit free-running timer
 - Global network time, synchronized by a specific message
 - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
 - Full-speed / low-speed host controller
 - USB 1.1 and 2.0 compliant full-speed / low speed device controller
 - 16 bidirectional end points

Family Configurations

- Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
 - 12.5 ns resolution at 80 MHz
 - Programmable sources for clock input, including an external clock option
 - Programmable prescaler
 - Input capture capability with programmable trigger edge on input pin
 - Output compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts on input capture or output compare
 - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
 - 16-bit architecture
 - Programmable prescaler
 - Output pulse-widths variable from microseconds to seconds
 - Single 16-bit input pulse accumulator
 - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
 - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
 - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
 - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
 - Programmable period and duty cycle
 - Programmable enable/disable for each channel
 - Software selectable polarity for each channel
 - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
 - Programmable center or left aligned outputs on individual channels
 - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
 - Emergency shutdown
- Two periodic interrupt timers (PITs)
 - 16-bit counter
 - Selectable as free running or count down
- Real-Time Clock (RTC)
 - Maintains system time-of-day clock
 - Provides stopwatch and alarm interrupt functions
 - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
 - 32-bit counter
 - Low-power mode support
- Backup watchdog timer (BWT)
 - Independent timer that can be used to help software recover from runaway code
 - 16-bit counter
 - Low-power mode support
- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator

1.2.27 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

1.2.28 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable part number summary

Freescal Part Number	FlexCAN	Encryption	Speed (MHz)	Flash (KB)	SRAM (KB)	Package	Temp range (°C)
MCF52252AF80	—	—	80	256	32	100 LQFP	0 to +70
MCF52252CAF66	•	—	66				-40 to +85
MCF52254AF80	—	—	80	512	64	100 LQFP	0 to +70
MCF52254CAF66	•	—	66				-40 to +85
MCF52255CAF80	•	•	80	512	64	100 LQFP	-40 to +85
MCF52256AG80	—	—	80	256	32	144 LQFP	0 to +70
MCF52256CAG66	•	—	66		64		-40 to +85
MCF52256CVN66	•	—	66		64	144 MAPBGA	-40 to +85
MCF52256VN80	—	—	80		32		0 to +70
MCF52258AG80	—	—	80	512	64	144 LQFP	0 to +70
MCF52258CAG66	•	—	66				-40 to +85
MCF52258CVN66	•	—	66			144 MAPBGA	-40 to +85
MCF52258VN80	—	—	80				0 to +70
MCF52259CAG80	•	•	80	512	64	144 LQFP	-40 to +85
MCF52259CVN80	•	•				144 MAPBGA	-40 to +85

Family Configurations

Figure 2 shows the pinout configuration for the 144 LQFP.

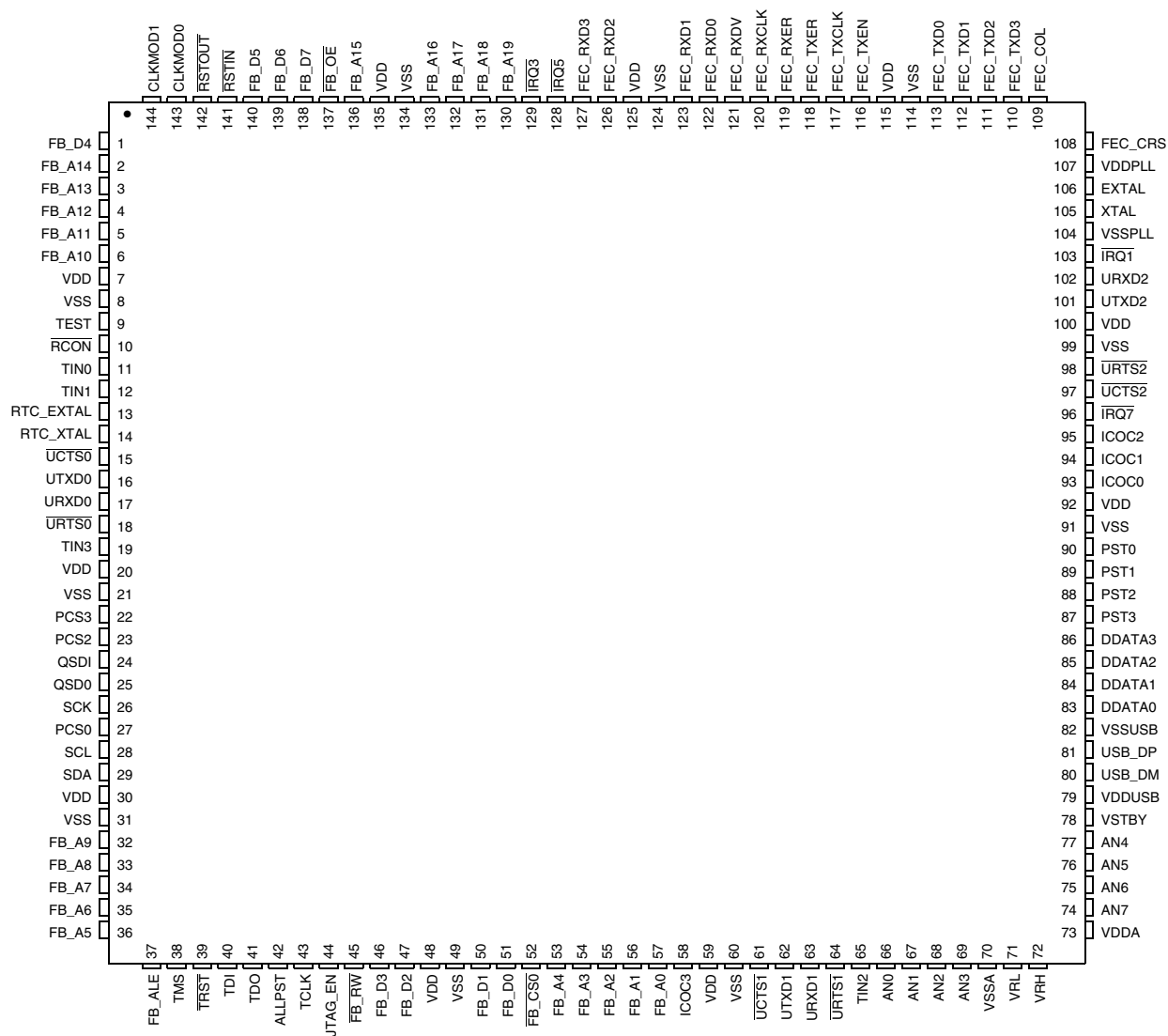


Figure 2. 144 LQFP Pin Assignment

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_RXD0	FEC_RXER	FEC_TXEN	FEC_TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_RXD1	FEC_RXCLK	FEC_TXCLK	FEC_TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_RXD2	FEC_RXDV	FEC_TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_RXD3	FEC_TXER	FEC_TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/ Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0 ³	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up ⁴	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up ⁴	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up ⁴	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up ⁴	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up ⁴	A6	129	96
	IRQ1	—	USB_ALT CLK	PNQ1	Low	High	Pull-Up ⁴	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up ⁵	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up ⁵	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/BKPT	—	—	—	N/A	N/A	Pull-Up ⁵	K1	38	26
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up ⁵	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mode Selection	RCON/EZPCS	—	—	—	N/A	N/A	Pull-Up	E4	10	4
	CLKMOD[1:0]	—	—	—	N/A	N/A	Pull-Down	D4, D5	144, 143	100, 99
QSPI	QSPI_CS3	SYNCA	USB_DP_PDOWN	PQS6	PSRR[7]	PDSR[7]	—	G4	22	16
	QSPI_CS2	SYNCB	USB_DM_PDOWN	PQS5	PSRR[6]	PDSR[6]	—	G3	23	17
	QSPI_CS0	I2C_SDA0	UCTS1	PQS3	PSRR[4]	PDSR[4]	Pull-Up ⁶	H4	27	21
	QSPI_CLK/EZPCK	I2C_SCL0	URTS1	PQS2	PSRR[3]	PDSR[3]	Pull-Up ⁶	H3	26	20
QSPI	QSPI_DIN/EZPD	I2C_SDA1	URXD1	PQS1	PSRR[2]	PDSR[2]	Pull-Up ⁶	G2	24	18
	QSPI_DOUT/EZPQ	I2C_SCL1	UTXD1	PQS0	PSRR[1]	PDSR[1]	Pull-Up ⁶	G1	25	19
Reset ⁷	RSTI	—	—	—	N/A	N/A	Pull-Up ⁷	A3	141	97
	RSTO	—	—	—	Low	High	—	A2	142	98
Test	TEST	—	—	—	N/A	N/A	Pull-Down	B1	9	3
Timer 3, 16-bit	GPT3	—	PWM7	PTA3	PSRR[23]	PDSR[23]	Pull-Up ⁸	M7	58	35
Timer 2, 16-bit	GPT2	—	PWM5	PTA2	PSRR[22]	PDSR[22]	Pull-Up ⁸	J10	95	62
Timer 1, 16-bit	GPT1	—	PWM3	PTA1	PSRR[21]	PDSR[21]	Pull-Up ⁸	J11	94	61
Timer 0, 16-bit	GPT0	—	PWM1	PTA0	PSRR[20]	PDSR[20]	Pull-Up ⁸	F12	93	60
Timer 3, 32-bit	DTIN3	DTOUT3	PWM6	PTC3	PSRR[19]	PDSR[19]	—	F4	19	13
Timer 2, 32-bit	DTIN2	DTOUT2	PWM4	PTC2	PSRR[18]	PDSR[18]	—	J8	65	42

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	−0.3 to +4.0	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 or 0 to 70 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see orderable part number summary ([Table 2](#))

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 11. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{\text{sys}} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{\text{sys}} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{\text{cyc}}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.6 ESD Protection

Table 12. ESD Protection Characteristics^{1, 2}

Characteristics	Symbol	Value	Units
ESD target for Human Body Model	HBM	2000	V
ESD target for Machine Model	MM	200	V
HBM circuit description	R_{series}	1500	Ω
	C	100	pF
MM circuit description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM)			
• Positive pulses	—	1	—
• Negative pulses	—	1	—
Number of pulses per pin (MM)			
• Positive pulses	—	3	—
• Negative pulses	—	3	—
Interval of pulses	—	1	sec

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications ¹

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis ²	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS} , digital pins	I_{in}	-1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = -2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$ mA	V_{OL}	—	0.5	V
Output high voltage (high drive) $I_{OH} = -5$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5$ mA	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (low drive) $I_{OL} = 2$ mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max. ³	I_{APU}	-10	-130	μA
Input Capacitance ⁴ • All input-only pins • All input/output (three-state) pins	C_{in}	— —	7 7	pF

¹ Refer to Table 14 for additional PLL specifications.

² Only for pins: IRQ1, IRQ3, IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

³ Refer to Table 3 for pins having internal pull-up devices.

⁴ This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 14. Oscillator and PLL Specifications
 $(V_{DD} \text{ and } V_{DDPLL} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	f_{crystal} f_{ext}	12 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	$f_{\text{ref_pll}}$	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{\text{ref}} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4,9}	t_{lpll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK range	f_{UL}	−1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	−0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary (Table 2).

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

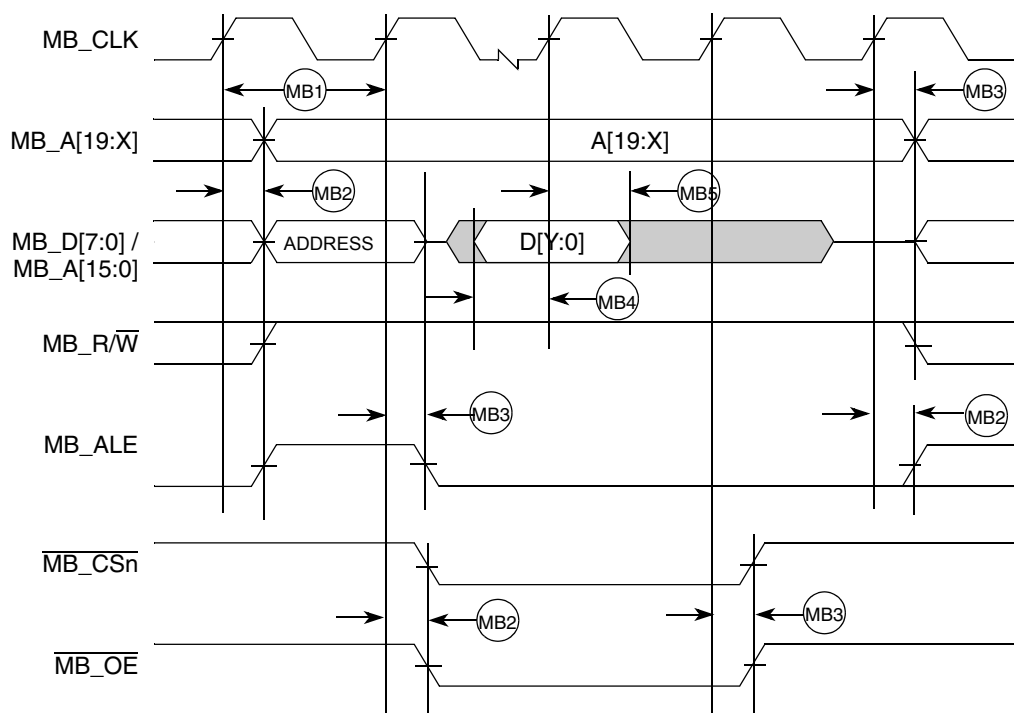


Figure 5. Mini-FlexBus Read Timing

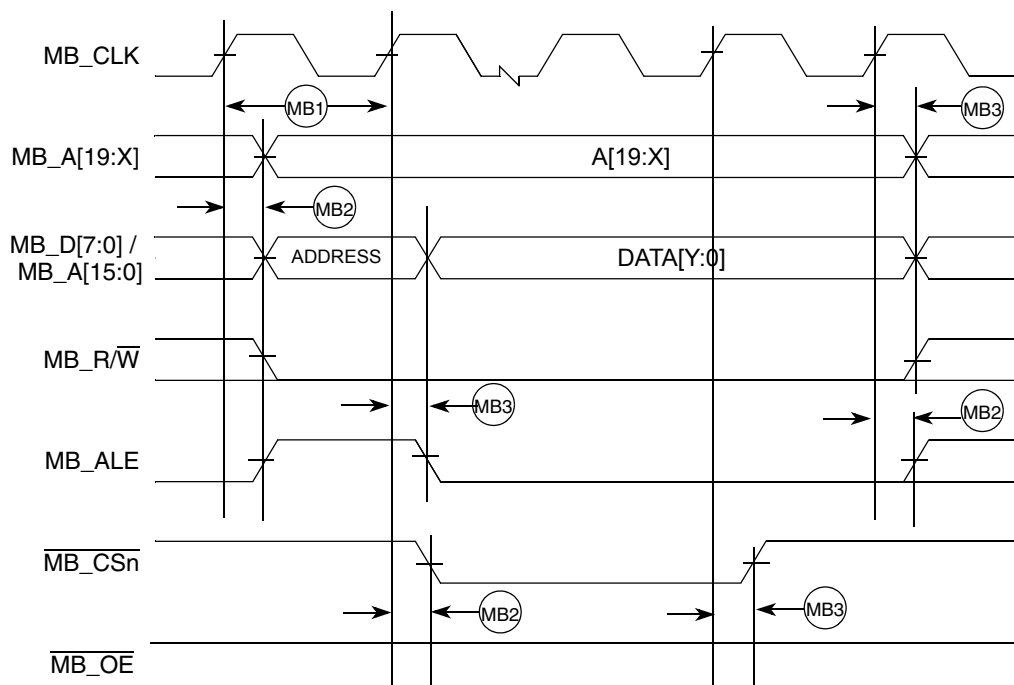


Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

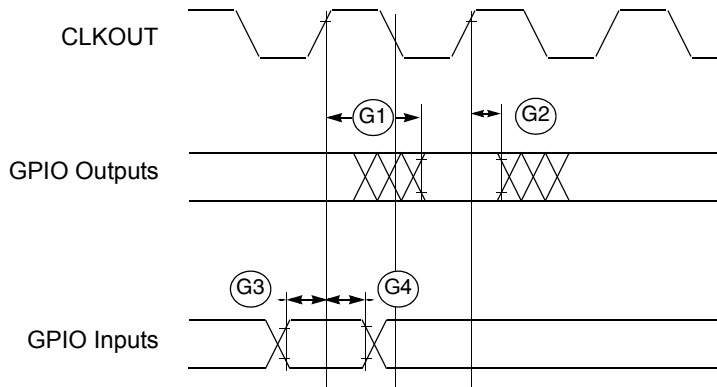


Figure 11. GPIO Timing

2.13 Reset Timing

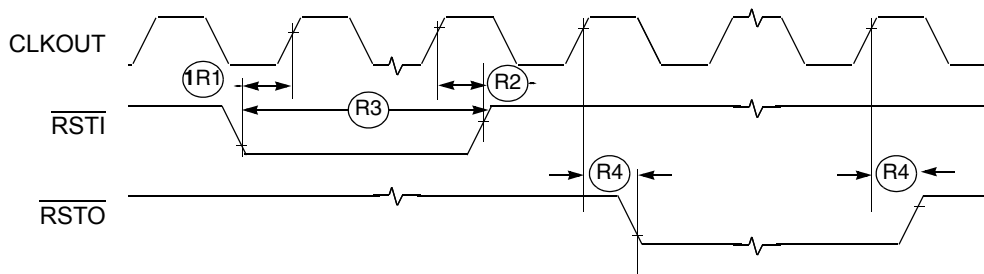
Table 22. Reset and Configuration Override Timing

($V_{DD} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H)¹

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

Figure 12. $\overline{RSTI}$ and Configuration Override Timing

2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

Table 26. Timer Module AC Timing Specifications

Name	Characteristic ¹	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

¹ All timing references to CLKOUT are given to its rising edge.

2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

Table 27. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.

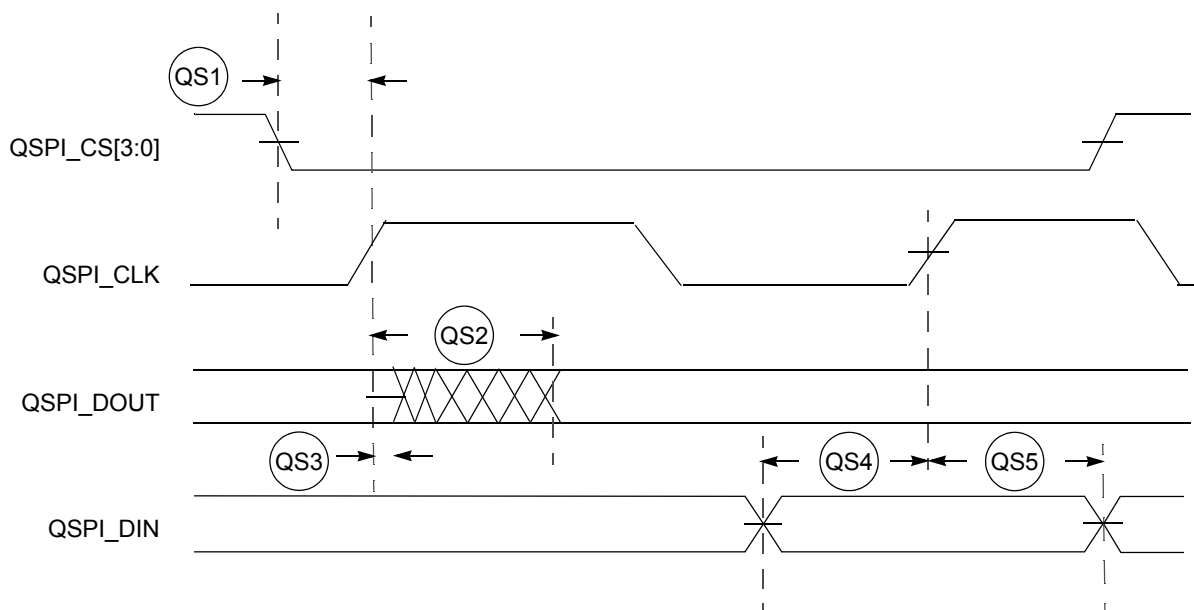


Figure 15. QSPI Timing

2.19 JTAG and Boundary Scan Timing

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys}/2$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

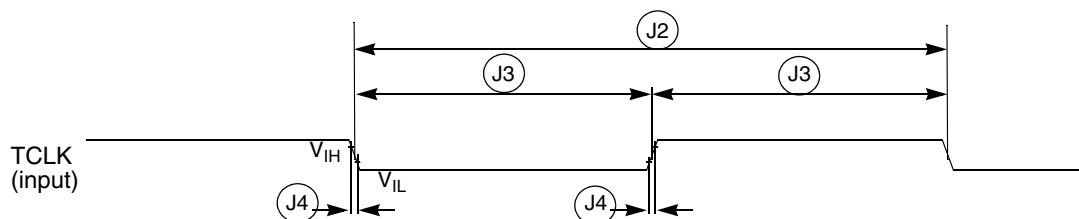


Figure 16. Test Clock Input Timing

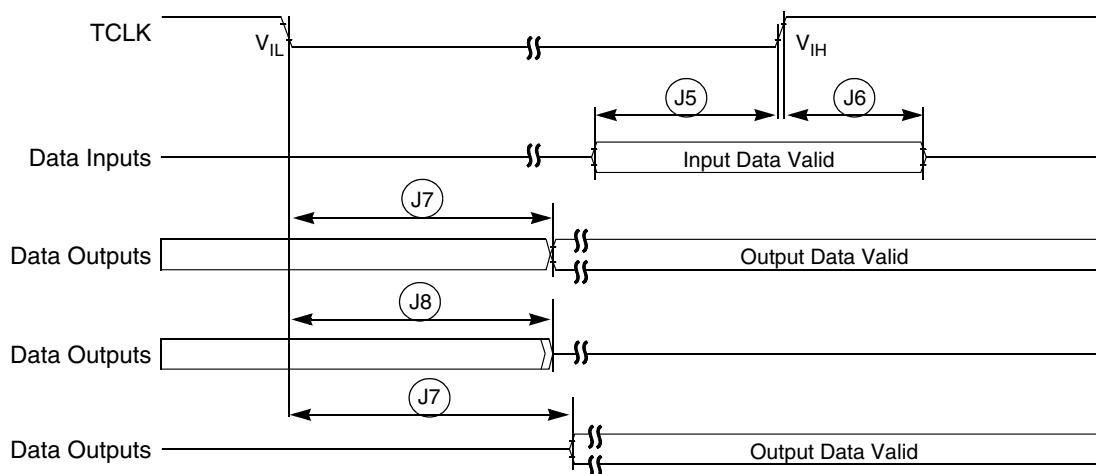


Figure 17. Boundary Scan (JTAG) Timing

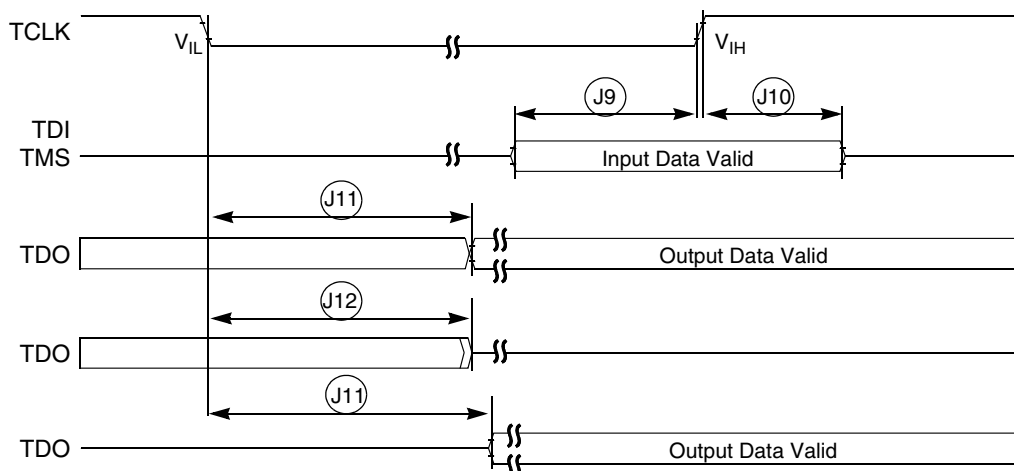
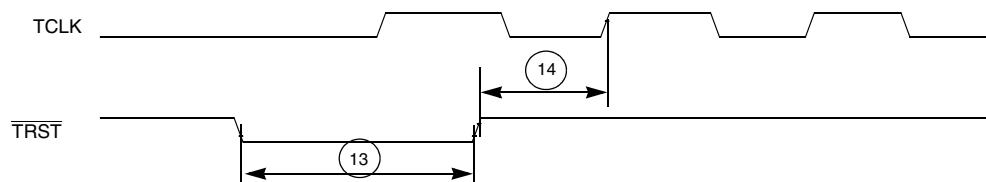


Figure 18. Test Access Port Timing

Figure 19. $\overline{\text{TRST}}$ Timing

2.20 Debug AC Timing Specifications

Table 29 lists specifications for the debug AC timing parameters shown in Figure 21.

Table 29. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 ¹	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 20 shows real-time trace timing for the values in Table 29.

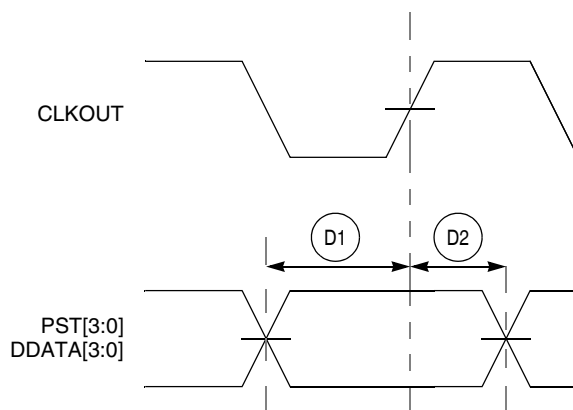


Figure 20. Real-Time Trace AC Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

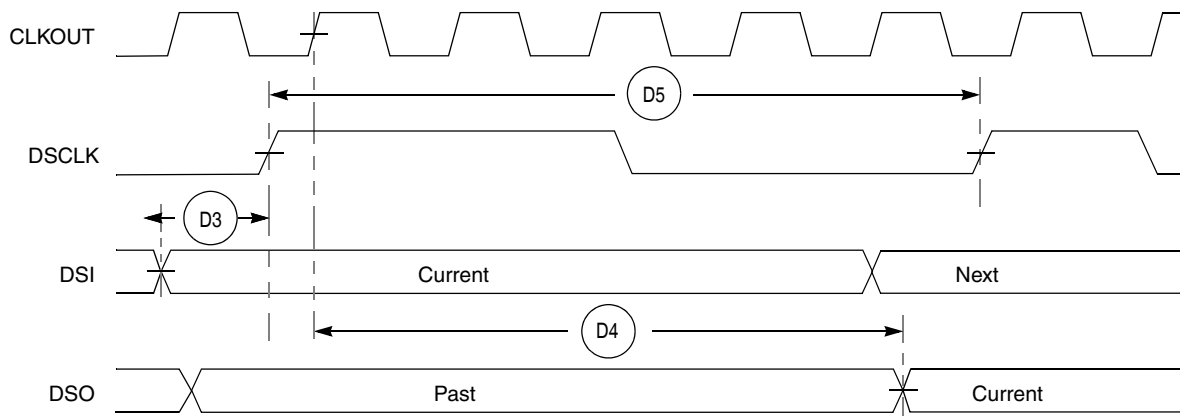


Figure 21. BDM Serial Port AC Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on <http://www.freescale.com/coldfire>. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W
MCF52258		
MCF52259		98ASH70694A

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	- Added package dimensions to package diagrams - Added listing of devices for MCF52259 family - Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation” - Updated the figure Pinout Top View (144 MAPBGA) - Removed an extraneous instance of the table Pin Functions by Primary and Alternate Purpose - In the table Pin Functions by Primary and Alternate Purpose, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL” - In the table SGFM Flash Program and Erase Characteristics, changed “(V_{DDF} = 2.7 to 3.6 V)” to “(V_{DD} = 3.0 to 3.6 V)” - In the table SGFM Flash Module Life Characteristics, changed “(V_{DDF} = 2.7 to 3.6 V)” to “(V_{DD} = 3.0 to 3.6 V)” - In the table Oscillator and PLL Specifications, changed “V_{DD} and V_{DDPLL} = 2.7 to 3.6 V” to “V_{DD} and V_{DDPLL} = 3.0 to 3.6 V” - In the table Reset and Configuration Override Timing, changed “V_{DD} = 2.7 to 3.6 V” to “V_{DD} = 3.0 to 3.6 V”
2	- Added EzPort Electrical Specifications. - Updated Table 2 for part numbers. - In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values, JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. - Updated Table 14. - Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). - Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	- Updated EzPort Electrical Specifications - Added hysteresis note in the DC electrical table - Clarified pin function table for VSS pins. - Clarified orderable part summary.
4	- Updated EXTAL input high voltage (External reference) Maximum to “3.0V” (Instead of “VDD”). Also, added a footnote saying, “This value has been update” - Updated crystal frequency value to 25 MHz
5	Updated TOC