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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, Ethernet, I ² C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52254caf66

1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz ¹		up to 80 MHz ¹	up to 66 or 80 MHz ¹		up to 80 MHz ¹
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

¹ 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

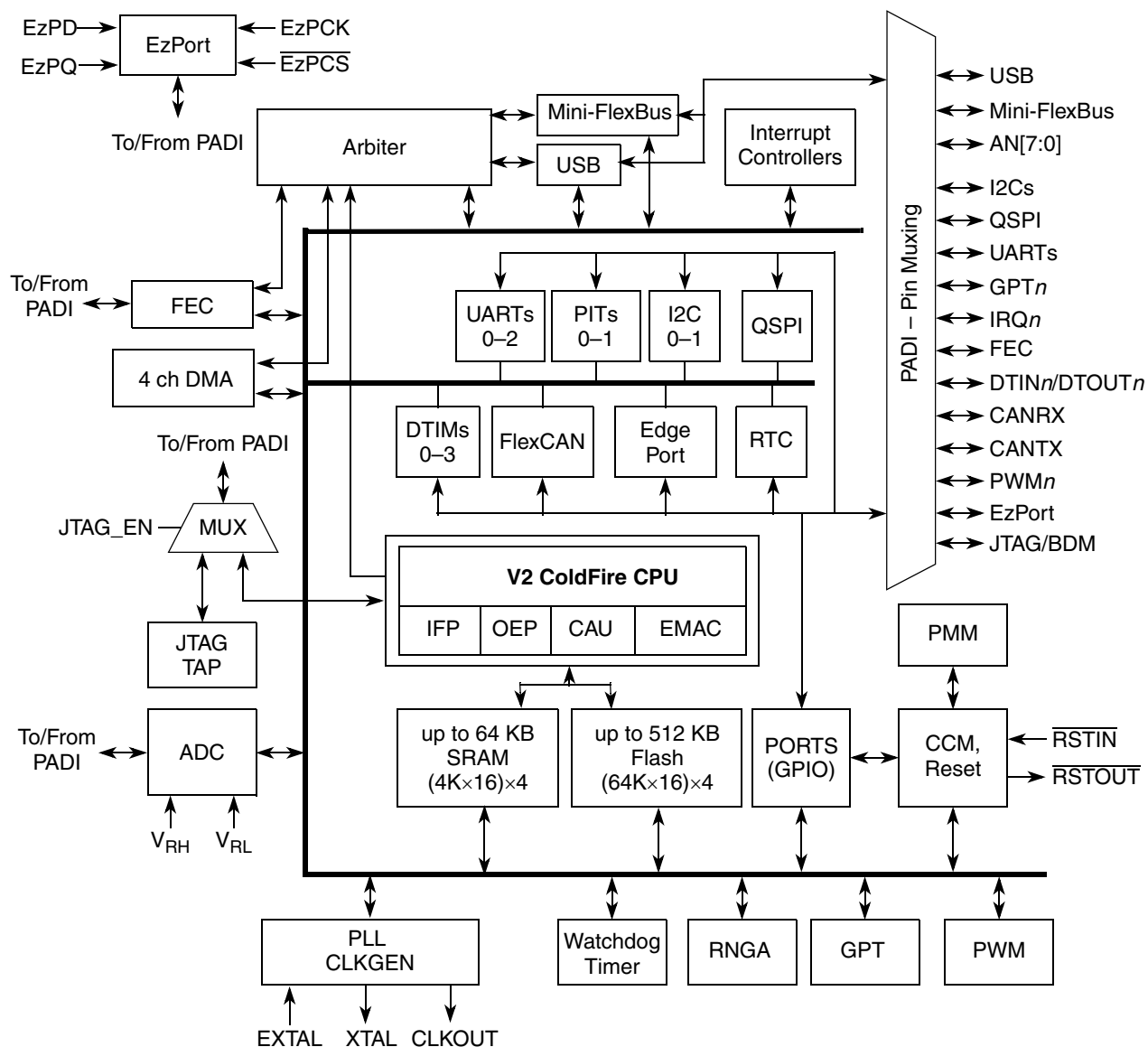


Figure 1. MCF52259 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip

Family Configurations

- Up to 80 MHz processor core frequency
- 40 MHz or 33 MHz peripheral bus frequency
- Sixteen general-purpose, 32-bit data and address registers
- Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
- Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 48$ operations
- Cryptographic Acceleration Unit (CAU)
 - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
 - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
 - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
 - Based on and includes all existing features of the Freescale TouCAN module
 - Full implementation of the CAN protocol specification version 2.0B
 - Standard data and remote frames (up to 109 bits long)
 - Extended data and remote frames (up to 127 bits long)
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
 - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
 - Unused MB space can be used as general purpose RAM space
 - Listen-only mode capability
 - Content-related addressing
 - No read/write semaphores
 - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
 - Programmable transmit-first scheme: lowest ID or lowest buffer number
 - Time stamp based on 16-bit free-running timer
 - Global network time, synchronized by a specific message
 - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
 - Full-speed / low-speed host controller
 - USB 1.1 and 2.0 compliant full-speed / low speed device controller
 - 16 bidirectional end points

- DMA or FIFO data stream interfaces
- Low power consumption
- OTG protocol logic
- Fast Ethernet controller (FEC)
 - 10/100 BaseT/TX capability, half duplex or full duplex
 - On-chip transmit and receive FIFOs
 - Built-in dedicated DMA controller
 - Memory-based flexible descriptor rings
- Mini-FlexBus
 - External bus interface available on 144 pin packages
 - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
 - 2 chip selects ($\overline{\text{FB_CS}}[1:0]$)
 - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
 - Multiplexed mode: 16-bit data and 20-bit address bus
 - FB_CLK output to support synchronous memories
 - Programmable base address, size, and wait states to support slow peripherals
 - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- Two I2C modules
 - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
 - Fully compatible with industry-standard I2C bus
 - Master and slave modes support multiple masters
 - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to three chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution
 - Minimum 1.125 μs conversion time
 - Simultaneous sampling of two channels for motor control applications
 - Single-scan or continuous operation
 - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

Family Configurations

- Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
 - 12.5 ns resolution at 80 MHz
 - Programmable sources for clock input, including an external clock option
 - Programmable prescaler
 - Input capture capability with programmable trigger edge on input pin
 - Output compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts on input capture or output compare
 - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
 - 16-bit architecture
 - Programmable prescaler
 - Output pulse-widths variable from microseconds to seconds
 - Single 16-bit input pulse accumulator
 - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
 - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
 - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
 - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
 - Programmable period and duty cycle
 - Programmable enable/disable for each channel
 - Software selectable polarity for each channel
 - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
 - Programmable center or left aligned outputs on individual channels
 - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
 - Emergency shutdown
- Two periodic interrupt timers (PITs)
 - 16-bit counter
 - Selectable as free running or count down
- Real-Time Clock (RTC)
 - Maintains system time-of-day clock
 - Provides stopwatch and alarm interrupt functions
 - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
 - 32-bit counter
 - Low-power mode support
- Backup watchdog timer (BWT)
 - Independent timer that can be used to help software recover from runaway code
 - 16-bit counter
 - Low-power mode support
- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.9 Mini-FlexBus

A multi-function external bus interface called the Mini-FlexBus is provided on the device with basic functionality of interfacing to slave-only devices with a maximum slave bus frequency up to 40 MHz in 1:2 mode and 80 MHz in 1:1 mode. It can be directly connected to the following asynchronous or synchronous devices with little or no additional circuitry:

- External ROMs
- Flash memories
- Programmable logic devices
- Other simple target (slave) devices

The Mini-FlexBus is a subset of the FlexBus module found on higher-end ColdFire microprocessors. The Mini-FlexBus minimizes package pin-outs while maintaining a high level of configurability and functionality.

1.2.10 USB On-The-Go Controller

The device includes a Universal Serial Bus On-The-Go (USB OTG) dual-mode controller. USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and handheld computers to host PCs. The OTG supplement to the USB specification extends USB to peer-to-peer application, enabling devices to connect directly to each other without the need for a PC. The dual-mode controller on the device can act as a USB OTG host and as a USB device. It also supports full-speed and low-speed modes.

1.2.11 Fast Ethernet Controller (FEC)

The Ethernet media access controller (MAC) supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FECs supports the 10/100 Mbps MII, and the 10 Mbps-only 7-wire interface.

1.2.12 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.13 I2C Bus

The processor includes two I2C modules. The I2C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.14 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.15 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing. Signals on the SYNCA and SYNCA pins initiate an ADC conversion.

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.16 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN n signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR n). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.17 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.18 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

1.2.19 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.20 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
ADC	AN[7:0]	—	—	PAN[7:0]	Low	Low	—	L12, K10, K12, K11, K9, L9, M10, M9	74–77; 69, 68, 67, 66	51–54, 46, 45, 44, 43
	VDDA	—	—	—	N/A	N/A	—	L11	73	50
	VSSA	—	—	—	N/A	N/A	—	M12	70	47
	VRH	—	—	—	N/A	N/A	—	L10	72	49
	VRL	—	—	—	N/A	N/A	—	M11	71	48
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	C12	106	73
	XTAL	—	—	—	N/A	N/A	—	D12	105	72
	VDDPLL	—	—	—	N/A	N/A	—	C11	107	74
	VSSPLL	—	—	—	N/A	N/A	—	D11	104	71
RTC	RTC_EXTAL	—	—	—	N/A	N/A	—	D1	13	7
	RTC_XTAL	—	—	—	N/A	N/A	—	E1	14	8
Debug Data	ALLPST	—	—	—	Low	High	—	L3	42	30
	DDATA[3:0]	—	—	PDD[7:4]	Low	High	—	G9, H10, F11, F10	86, 85, 84, 83	—
	PST[3:0]	—	—	PDD[3:0]	Low	High	—	F9, G10, G11, G12	87–90	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
VSS	VSS	—	—	—	N/A	N/A	—	A1; A12; F6–8; G6–8; H8; M1	8; 21; 31; 49; 60; 91; 99; 114; 124; 134	2; 15; 25; 34; 37; 66; 81; 91

¹ The PDSR and PSSR registers are part of the GPIO module. All programmable signals default to 2mA drive in normal (single-chip) mode.

² All signals have a pull-up in GPIO mode.

³ I2C1 is multiplexed with specific pins of the QSPI, UART1, UART2, and Mini-FlexBus pin groups.

⁴ For primary and GPIO functions only.

⁵ Only when JTAG mode is enabled.

⁶ For secondary and GPIO functions only.

⁷ RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.

⁸ For GPIO functions, the Primary Function has pull-up control within the GPT module.

⁹ Available on 144-pin packages only.

¹⁰ This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL.

Table 7. Current Consumption in Low-Power Mode, Code From SRAM^{1,2,3}

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11) ⁴	0.090				mA	I _{DD}
Stop mode 2 (Stop 10) ⁴	7					
Stop mode 1 (Stop 01) ^{4,5}	9	10	15	17		
Stop mode 0 (Stop 00) ⁵	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

¹ All values are measured with a 3.3 V power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.

³ CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.

⁴ See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.

⁵ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

Table 8. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	30 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	43 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	26 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	16 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	44 ^{7,8}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{1,9}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	35 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	23 ¹⁰	°C/W
	Junction to case	—	θ_{JC}	7 ¹¹	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹²	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{13,14}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,15}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ¹⁶	°C/W
	Junction to case	—	θ_{JC}	9 ¹⁷	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹⁸	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

¹ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

³ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

⁴ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

⁷ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

⁸ Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

⁹ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

¹⁰ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

¹¹ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

¹² Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

¹³ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

¹⁴ Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

¹⁵ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 11. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{\text{sys}} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{\text{sys}} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{\text{cyc}}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.6 ESD Protection

Table 12. ESD Protection Characteristics^{1, 2}

Characteristics	Symbol	Value	Units
ESD target for Human Body Model	HBM	2000	V
ESD target for Machine Model	MM	200	V
HBM circuit description	R_{series}	1500	Ω
	C	100	pF
MM circuit description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM)			
• Positive pulses	—	1	—
• Negative pulses	—	1	—
Number of pulses per pin (MM)			
• Positive pulses	—	3	—
• Negative pulses	—	3	—
Interval of pulses	—	1	sec

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications ¹

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis ²	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS} , digital pins	I_{in}	-1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = -2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$ mA	V_{OL}	—	0.5	V
Output high voltage (high drive) $I_{OH} = -5$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5$ mA	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (low drive) $I_{OL} = 2$ mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max. ³	I_{APU}	-10	-130	μA
Input Capacitance ⁴ • All input-only pins • All input/output (three-state) pins	C_{in}	— —	7 7	pF

¹ Refer to Table 14 for additional PLL specifications.

² Only for pins: IRQ1, IRQ3, IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

³ Refer to Table 3 for pins having internal pull-up devices.

⁴ This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 14. Oscillator and PLL Specifications
 $(V_{DD} \text{ and } V_{DDPLL} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	f_{crystal} f_{ext}	12 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	$f_{\text{ref_pll}}$	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{\text{ref}} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4,9}	t_{lpll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK range	f_{UL}	−1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	−0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary (Table 2).

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

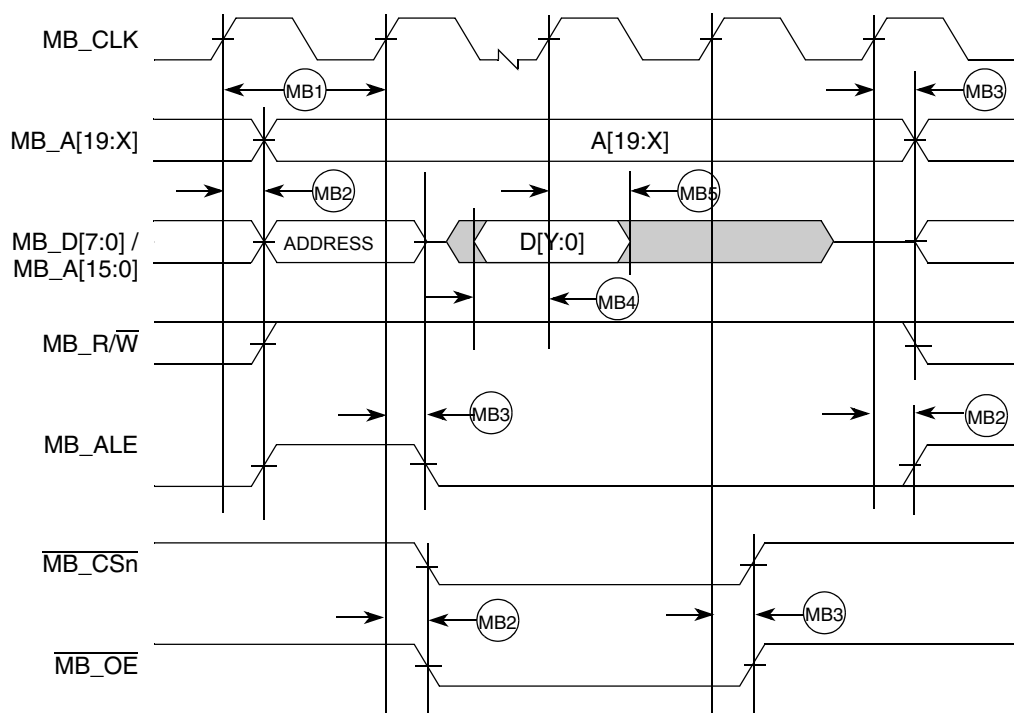


Figure 5. Mini-FlexBus Read Timing

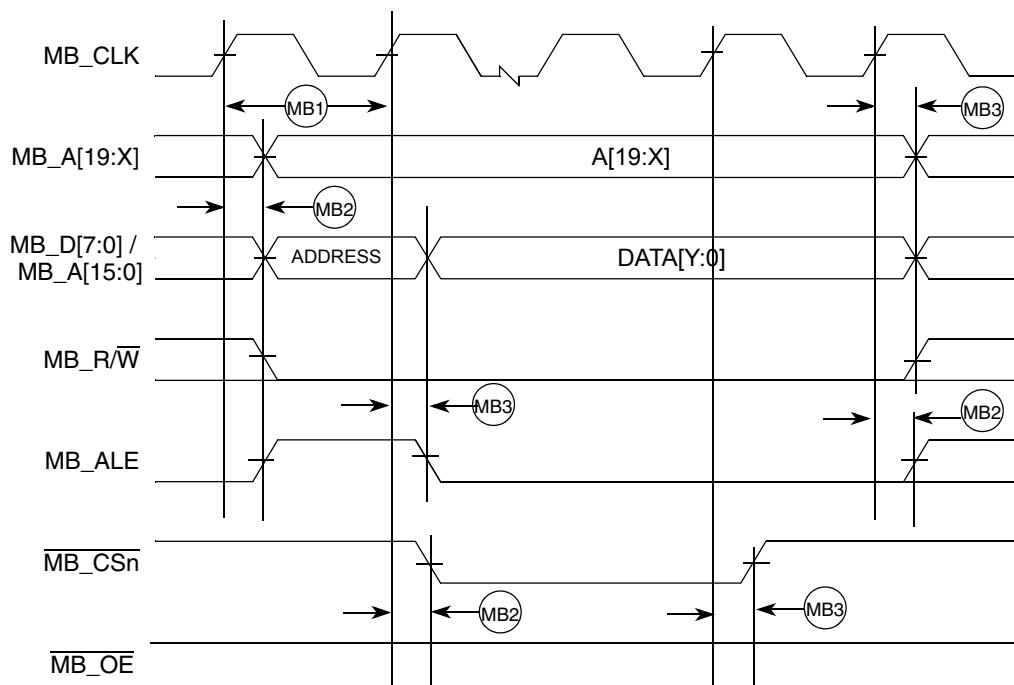


Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

2.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 17. Receive Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	RXCLK frequency	—	25	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup ¹	5	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold ¹	5	—	ns
E3	RXCLK pulse width high	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	RXCLK period

¹ In MII mode, n = 3

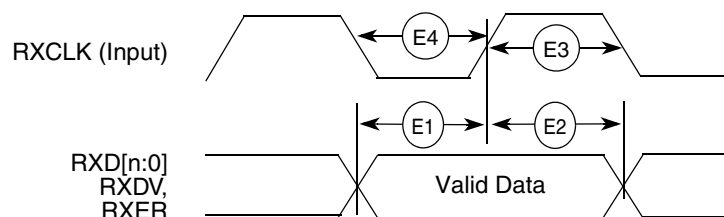


Figure 7. MII Receive Signal Timing Diagram

2.11.2 Transmit Signal Timing Specifications

Table 18. Transmit Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	TXCLK frequency	—	25	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid ¹	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid ¹	—	25	ns
E7	TXCLK pulse width high	35%	65%	t _{TXCLK}
E8	TXCLK pulse width low	35%	65%	t _{TXCLK}

¹ In MII mode, n = 3

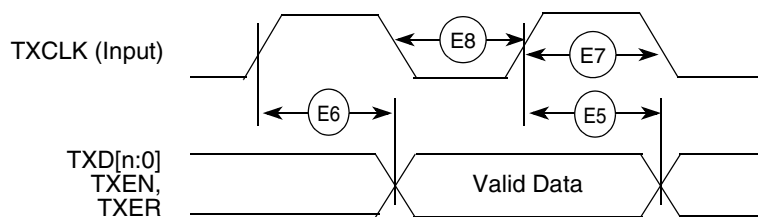


Figure 8. MII Transmit Signal Timing Diagram

2.14 I2C Input/Output Timing Specifications

Table 23 lists specifications for the I2C input timing parameters shown in Figure 13.

Table 23. I2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time ($V_{IL} = 0.5\text{ V}$ to $V_{IH} = 2.4\text{ V}$)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 24 lists specifications for the I2C output timing parameters shown in Figure 13.

Table 24. I2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 ¹	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2 ¹	Clock low period	$10 \times t_{CYC}$	—	ns
I3 ²	I2C_SCL/I2C_SDA rise time ($V_{IL} = 0.5\text{ V}$ to $V_{IH} = 2.4\text{ V}$)	—	—	μs
I4 ¹	Data hold time	$7 \times t_{CYC}$	—	ns
I5 ³	I2C_SCL/I2C_SDA fall time ($V_{IH} = 2.4\text{ V}$ to $V_{IL} = 0.5\text{ V}$)	—	3	ns
I6 ¹	Clock high time	$10 \times t_{CYC}$	—	ns
I7 ¹	Data setup time	$2 \times t_{CYC}$	—	ns
I8 ¹	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9 ¹	Stop condition setup time	$10 \times t_{CYC}$	—	ns

¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

³ Specified at a nominal 50 pF load.

Figure 13 shows timing for the values in Table 23 and Table 24.

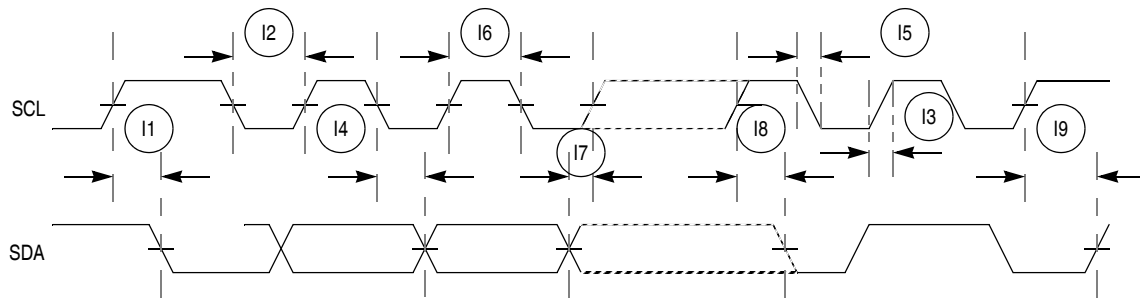


Figure 13. I2C Input/Output Timings

2.15 Analog-to-Digital Converter (ADC) Parameters

Table 25 lists specifications for the analog-to-digital converter.

Table 25. ADC Parameters¹

Name	Characteristic	Min	Typical	Max	Unit
V _{REFL}	Low reference voltage	V _{SSA}	—	V _{SSA} + 50 mV	V
V _{REFH}	High reference voltage	V _{DDA} - 50 mV	—	V _{DDA}	V
V _{DDA}	ADC analog supply voltage	3.1	3.3	3.6	V
V _{ADIN}	Input voltages	V _{REFL}	—	V _{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range) ²	—	±2.5	±3	LSB ³
INL	Integral non-linearity (10% to 90% input signal range) ⁴	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	-1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f _{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R _{AD}	Conversion range	V _{REFL}	—	V _{REFH}	V
t _{ADPU}	ADC power-up time ⁵	—	6	13	t _{AIC} cycles ⁶
t _{REC}	Recovery from auto standby	—	0	1	t _{AIC} cycles
t _{ADC}	Conversion time	—	6	—	t _{AIC} cycles
t _{ADS}	Sample time	—	1	—	t _{AIC} cycles
C _{ADI}	Input capacitance	—	See Figure 14	—	pF
X _{IN}	Input impedance	—	See Figure 14	—	W
I _{ADI}	Input injection current ⁷ , per pin	—	—	3	mA
I _{VREFH}	V _{REFH} current	—	0	—	mA
V _{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E _{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V _{OFFSET}	Offset voltage external reference	—	±3	9	mV

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys}/2$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	\overline{TRST} assert time	t_{TRSTAT}	100	—	ns
J14	\overline{TRST} setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

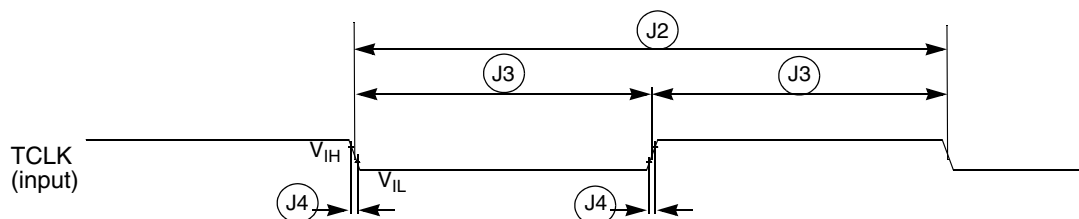


Figure 16. Test Clock Input Timing