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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52255caf80

1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz[1]		up to 80 MHz[1]	up to 66 or 80 MHz[1]		up to 80 MHz[1]
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

[1] 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

  - DMA or FIFO data stream interfaces
  - Low power consumption
  - OTG protocol logic
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- Mini-FlexBus
  - External bus interface available on 144 pin packages
  - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
  - 2 chip selects ($\overline{FB\_CS}$[1:0])
  - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
  - Multiplexed mode: 16-bit data and 20-bit address bus
  - FB_CLK output to support synchronous memories
  - Programmable base address, size, and wait states to support slow peripherals
  - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I2C modules
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

- Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
- System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
- Low power modes supported
- 2^n ($0 \le n \le 15$) low-power divider for extremely low frequency operation

- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O on 100-pin package
  - Up to 96 bits of general purpose I/O on 144-pin package
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 64 KB memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64 KB boundary within the 4 GB address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA, FEC, and USB. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 64 KB×16-bit flash memory arrays to generate 512 KB of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Cryptographic Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

Figure 2 shows the pinout configuration for the 144 LQFP.

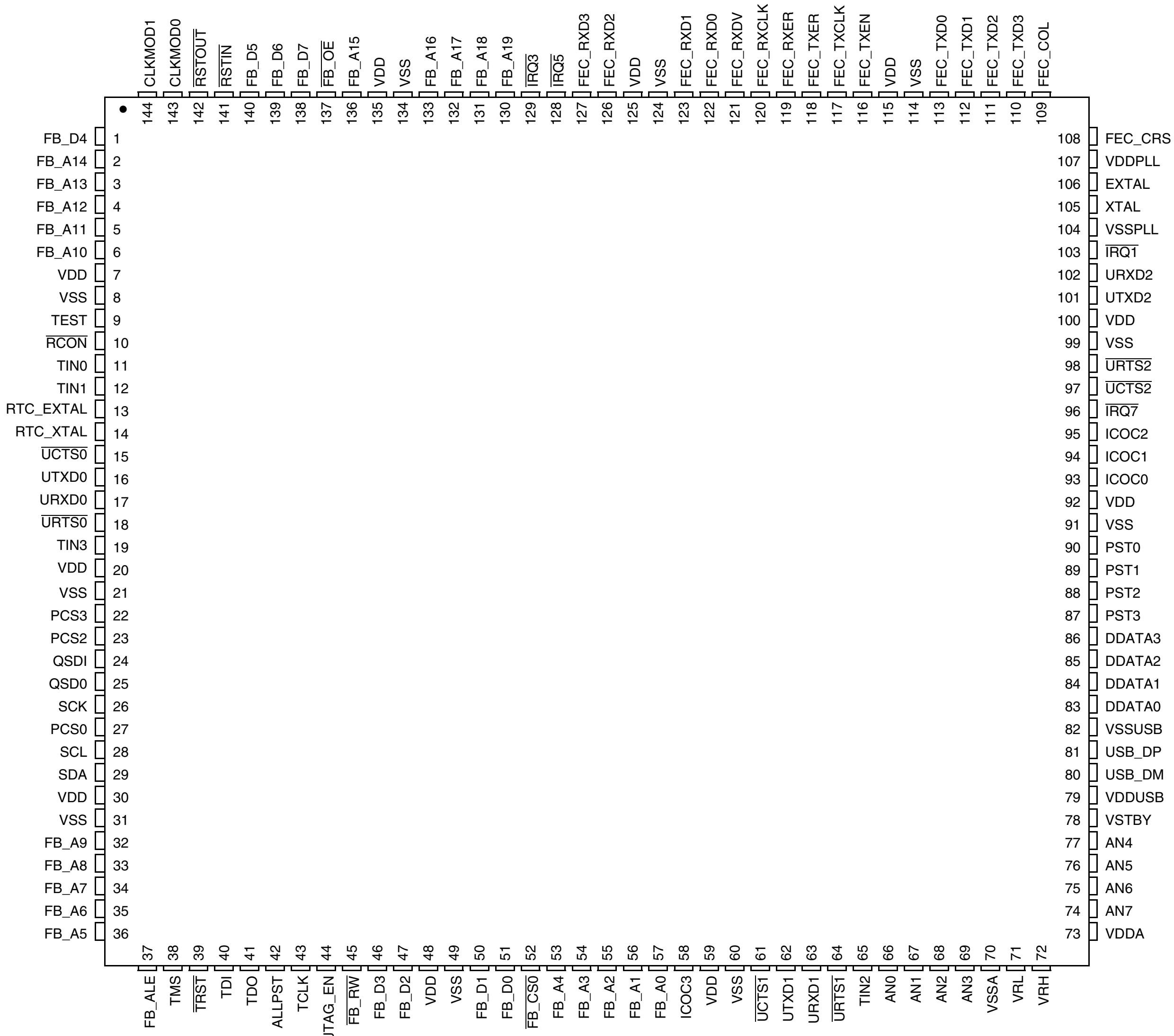


Figure 2. 144 LQFP Pin Assignment

Figure 3 shows the pinout configuration for the 100 LQFP.

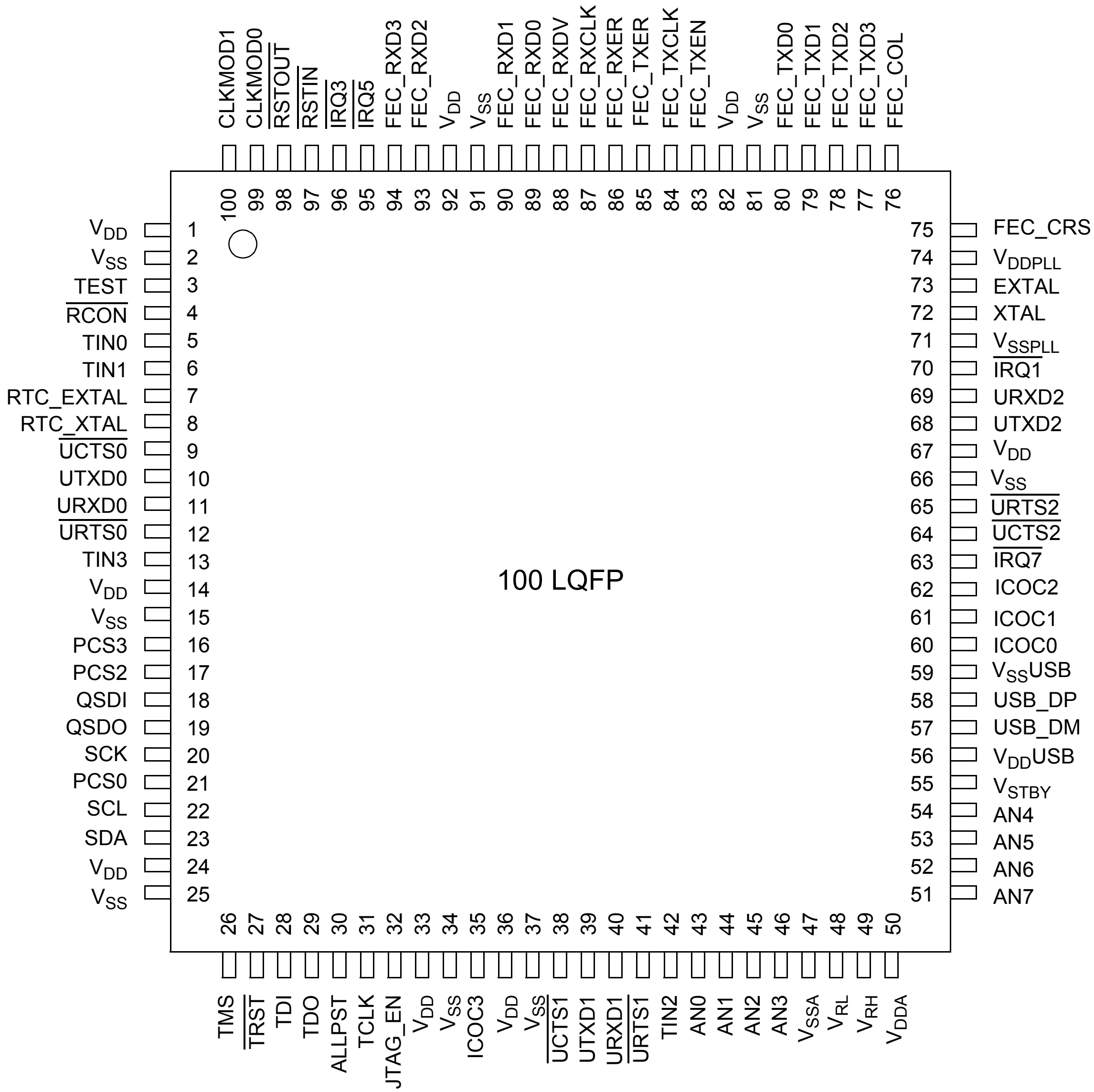


Figure 3. 100 LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_ RXD0	FEC_ RXER	FEC_ TXEN	FEC_ TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_ RXD1	FEC_ RXCLK	FEC_ TXCLK	FEC_ TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_ RXD2	FEC_ RXDV	FEC_ TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_ EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_ RXD3	FEC_ TXER	FEC_ TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_ XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_ EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0[3]	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up[4]	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up[4]	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up[4]	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up[4]	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up[4]	A6	129	96
	IRQ1	—	USB_ALT CLK	PNQ1	Low	High	Pull-Up[4]	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up[5]	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[5]	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/$\overline{BKPT}$	—	—	—	N/A	N/A	Pull-Up[5]	K1	38	26
	$\overline{TRST}$/DSCLK	—	—	—	N/A	N/A	Pull-Up[5]	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mini-FlexBus[9]	FB_ALE	$\overline{\text{FB\_CS1}}$	—	PAS2	PSRRL[20]	PDSRL[20]	—	K3	37	—
	FB_AD[7:0]	—	—	PTE[7:0]	PSRRL[7:0]	PDSRL[7:0]	—	J2, J1, K4, K6, J6, M6, L6, L7	34–36; 53–57	—
	FB_AD[15:8]	—	—	PTF[7:0]	PSRRL[15:8]	PDSRL[15:8]	—	C4, B2, C3, C2, D3, E3, J3, J4	136, 2–6, 32–33	—
	FB_AD[19:16]	—	—	PTG[3:0]	PSRRL[19:16]	PDSRL[19:16]	—	B6, C6, D6, C5	130–133	—
	$\overline{\text{FB\_CS0}}$	—	—	PTG5	PSRRL[21]	PDSRL[21]	—	M5	52	—
	FB_R/$\overline{\text{W}}$	—	—	PTG7	PSRRL[31]	PDSRL[31]	—	M4	45	—
	$\overline{\text{FB\_OE}}$	—	—	PTG6	PSRRL[30]	PDSRL[30]	—	B5	137	—
	FB_D7	CANRX	—	PTH5	PSRRL[29]	PDSRL[29]	—	A5	138	—
	FB_D6	CANTX	—	PTH4	PSRRL[28]	PDSRL[28]	—	A4	139	—
	FB_D5	I2C_SCL1	—	PTH3	PSRRL[27]	PDSRL[27]	Pull-Up[6]	B4	140	—
	FB_D4	I2C_SDA1	—	PTH2	PSRRL[26]	PDSRL[26]	Pull-Up[6]	B3	1	—
	FB_D3	USB_ VBUSD	—	PTH1	PSRRL[25]	PDSRL[25]	—	L4	46	—
	FB_D2	USB_ VBUSE	—	PTH0	PSRRL[24]	PDSRL[24]	—	K5	47	—
	FB_D1	SYNCA	—	PTH7	PSRRL[23]	PDSRL[23]	—	L5	50	—
	FB_D0	SYNCB	—	PTH6	PSRRL[22]	PDSRL[22]	—	J5	51	—
Standby Voltage	VSTBY	—	—	—	N/A	N/A	—	J12	78	55
VDD[10]	VDD	—	—	—	N/A	N/A	—	E5–E8; F5; G5; H5–7; J7	7; 20; 30; 48; 59; 92; 100; 115; 125; 135	1; 14; 24; 33; 36; 67; 82; 92

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
VSS	VSS	—	—	—	N/A	N/A	—	A1; A12; F6–8; G6–8; H8; M1	8; 21; 31; 49; 60; 91; 99; 114; 124; 134	2; 15; 25; 34; 37; 66; 81; 91

[1] The PDSR and PSSR registers are part of the GPIO module. All programmable signals default to 2mA drive in normal (single-chip) mode.
[2] All signals have a pull-up in GPIO mode.
[3] I2C1 is multiplexed with specific pins of the QSPI, UART1, UART2, and Mini-FlexBus pin groups.
[4] For primary and GPIO functions only.
[5] Only when JTAG mode is enabled.
[6] For secondary and GPIO functions only.
[7] RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
[8] For GPIO functions, the Primary Function has pull-up control within the GPT module.
[9] Available on 144-pin packages only.
[10] This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	–0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	–0.3 to +4.0	V
Digital input voltage [3]	V_{IN}	–0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins)[4, 5]	I_{DD}	25	mA
Operating temperature range (packaged)	T_A $(T_L$ - $T_H)$	–40 to 85 or 0 to 70[6]	°C
Storage temperature range	T_{stg}	–65 to 150	°C

1. Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).
3. Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
5. The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).
6. Depending on the packaging; see orderable part number summary (Table 2)

2.2 Current Consumption

Table 5. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical[1] Active (SRAM)	Typical[1] Active (Flash)	Peak[2] (Flash)	Unit
PLL @ 8 MHz	I_{DD}	22	30	36	mA
PLL @ 16 MHz		31	45	60	
PLL @ 64 MHz		84	100	155	
PLL @ 80 MHz		102	118	185	
RAM standby supply current • Normal operation: $V_{DD} > V_{STBY}$ - 0.3 V • Standby operation: $V_{DD} < V_{SS}$ + 0.5 V	I_{STBY}	— —		5 20	μA μA
Analog supply current • Normal operation	I_{DDA}	2 [3]		15	mA
USB supply current	I_{DDUSB}	—		2	mA
PLL supply current	I_{DDPLL}	—		6 [4]	mA

1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).
2 Peak current measured with all modules active, CPU polling a status register, and default drive strength with matching load.
3 Tested using Auto Power Down (APD), which powers down the ADC between conversions; ADC running at 4 MHz in Once Parallel mode with a sample rate of 3 kHz.
4 Tested with the PLL MFD set to 7 (max value). Setting the MFD to a lower value results in lower current consumption.

Table 6. Current Consumption in Low-Power Mode, Code From Flash Memory[1,2,3]

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11)[4]	0.150				mA	I_{DD}
Stop mode 2 (Stop 10)[4]	7.0					
Stop mode 1 (Stop 01)[4,5]	9	10	15	17		
Stop mode 0 (Stop 00)[5]	9	10	15	17		
Wait / Doze	21	32	56	65		
Run	23	36	70	81		

1 All values are measured with a 3.30 V power supply. Tests performed at room temperature.
2 Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.
3 CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 and CFM off before entering low-power mode. CLKOUT is disabled.
4 See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.
5 Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

Table 7. Current Consumption in Low-Power Mode, Code From SRAM[1,2,3]

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11)[4]	0.090				mA	I_{DD}
Stop mode 2 (Stop 10)[4]	7					
Stop mode 1 (Stop 01)[4,5]	9	10	15	17		
Stop mode 0 (Stop 00)[5]	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

1 All values are measured with a 3.3 V power supply. Tests performed at room temperature.
2 Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.
3 CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.
4 See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.
5 Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

Table 8. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	30[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	43[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	26[1,3]	°C/W
	Junction to board	—	θ_{JB}	16[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	44[7,8]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35[1,9]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	35[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,3]	°C/W
	Junction to board	—	θ_{JB}	23[10]	°C/W
	Junction to case	—	θ_{JC}	7[11]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[12]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

[16] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[17] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[18] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A	= ambient temperature, °C
Θ_{JA}	= package thermal resistance, junction-to-ambient, °C/W
P_D	= $P_{INT} + P_{I/O}$
P_{INT}	= chip internal power, $I_{DD} \times V_{DD}$, W
$P_{I/O}$	= power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^{\ 2} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 9 and Table 10.

Table 9. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

[1] Depending on packaging; see the orderable part number summary (Table 2).
[2] Refer to the flash memory section for more information (Section 2.4, “Flash Memory Characteristics”)

Table 10. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

[1] A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis[2]	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, digital pins	I_{in}	–1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = -2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$ mA	V_{OL}	—	0.5	V
Output high voltage (high drive) $I_{OH} = -5$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5$ mA	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2$ mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) $I_{OL} = 2$ mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[3]	I_{APU}	–10	–130	μA
Input Capacitance [4] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

[1] Refer to Table 14 for additional PLL specifications.
[2] Only for pins: IRQ1, IRQ3. IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B
[3] Refer to Table 3 for pins having internal pull-up devices.
[4] This parameter is characterized before qualification rather than 100% tested.

2.9 USB Operation

Table 15. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys\_USB\_min}$	16	MHz

2.10 Mini-FlexBus External Interface Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 16. Mini-FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	—	80	MHz	
MB1	Clock Period	12.5	—	ns	
MB2	Output Valid	—	8	ns	1
MB3	Output Hold	2	—	ns	1
MB4	Input Setup	6	—	ns	2
MB5	Input Hold	0	—	ns	2

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

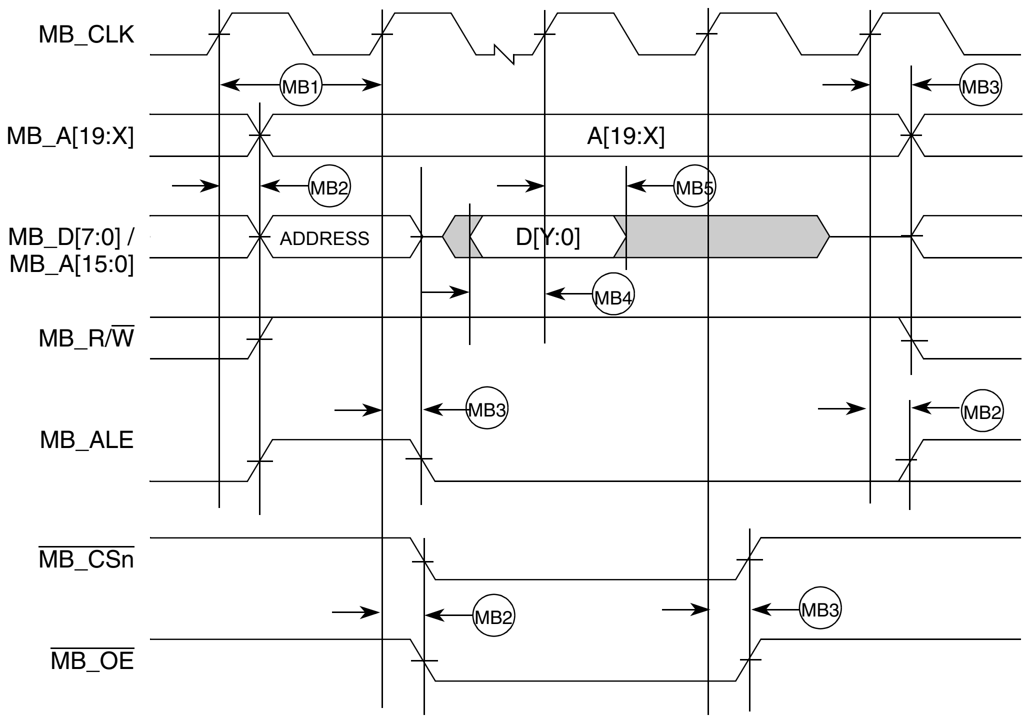


Figure 5. Mini-FlexBus Read Timing

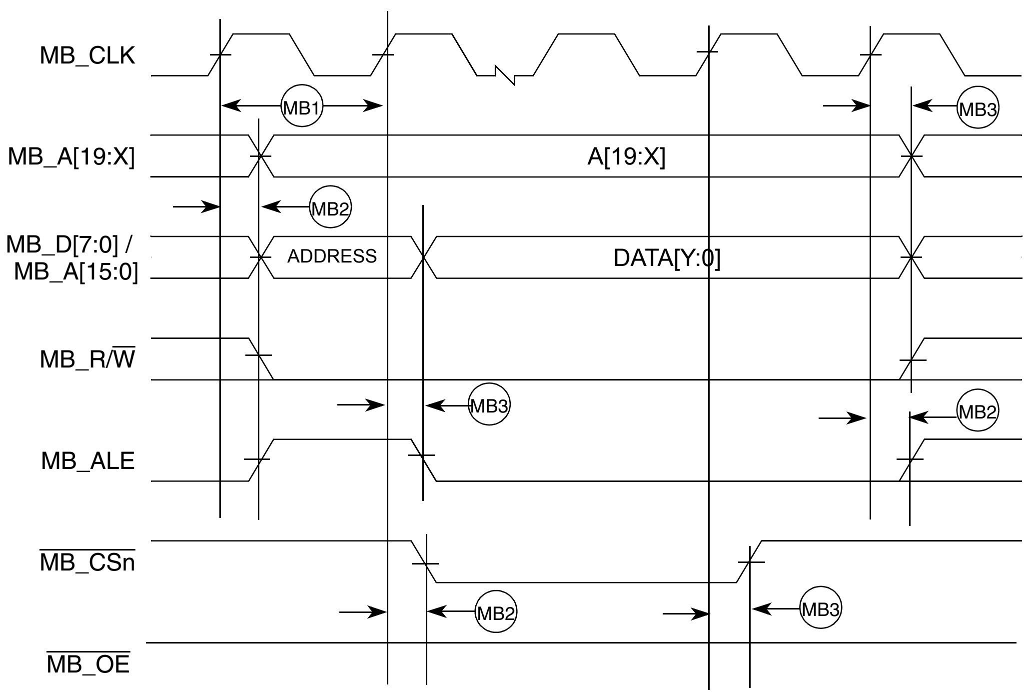


Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

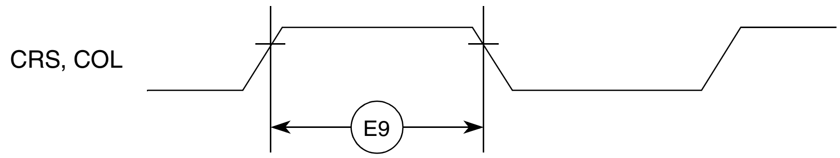


Figure 9. MII Async Inputs Timing Diagram

2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

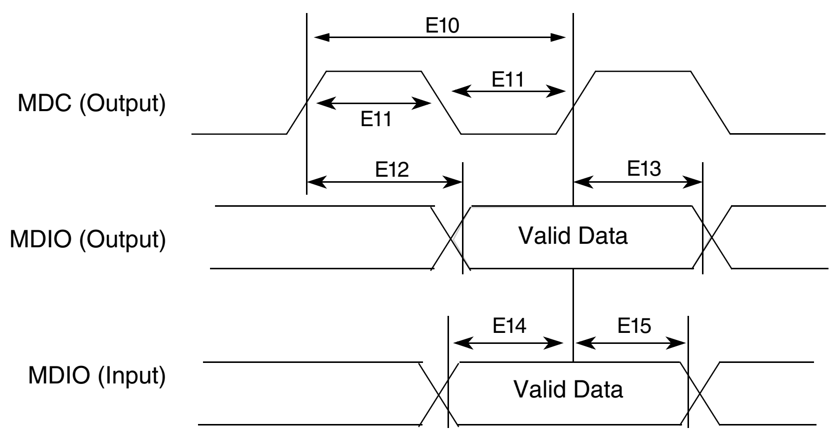


Figure 10. MII Serial Management Channel TIming Diagram

2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 21 and Figure 11.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

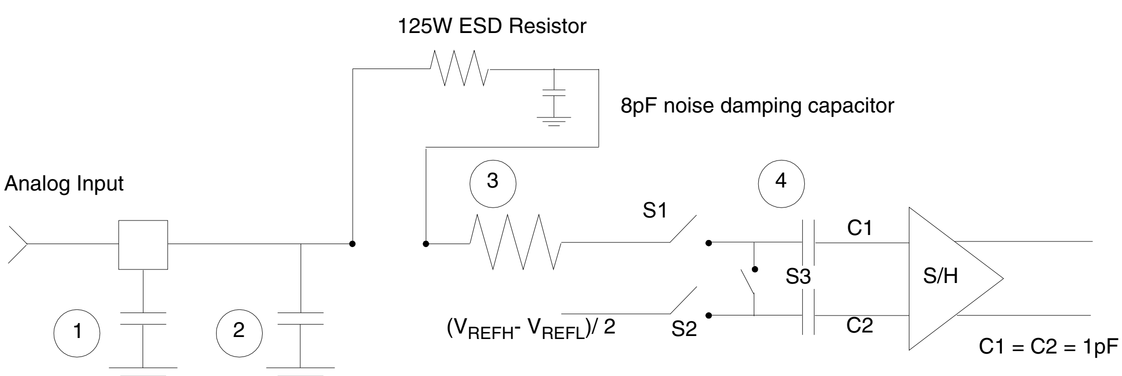
Table 25. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

1 All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3 V, V_{REFH} = 3.3 V, and V_{REFL} = ground
2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
3 LSB = Least Significant Bit
4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
5 Includes power-up of ADC and V_{REF}
6 ADC clock cycles
7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to (V_{REFH}-V_{REFL})/2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFH}-V_{REFL})/2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	• Added package dimensions to package diagrams • Added listing of devices for MCF52259 family • Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation” • Updated the figure **Pinout Top View (144 MAPBGA)** • Removed an extraneous instance of the table **Pin Functions by Primary and Alternate Purpose** • In the table **Pin Functions by Primary and Alternate Purpose**, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL” • In the table **SGFM Flash Program and Erase Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **SGFM Flash Module Life Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **Oscillator and PLL Specifications**, changed “V_{DD} and V_{DDPLL} = 2.7 to 3.6 V“ to “V_{DD} and V_{DDPLL} = 3.0 to 3.6 V“ • In the table **Reset and Configuration Override Timing**, changed “V_{DD} = 2.7 to 3.6 V“ to “V_{DD} = 3.0 to 3.6 V“
2	• Added EzPort Electrical Specifications. • Updated Table 2 for part numbers. • In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values,JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. • Updated Table 14. • Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). • Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	• Updated EzPort Electrical Specifications • Added hysteresis note in the DC electrical table • Clarified pin function table for VSS pins. • Clarified orderable part summary.
4	• Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, “This value has been update” • Updated crystal frequency value to 25 MHz
5	• Updated TOC