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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52256ag80

1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz[1]		up to 80 MHz[1]	up to 66 or 80 MHz[1]		up to 80 MHz[1]
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

[1] 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

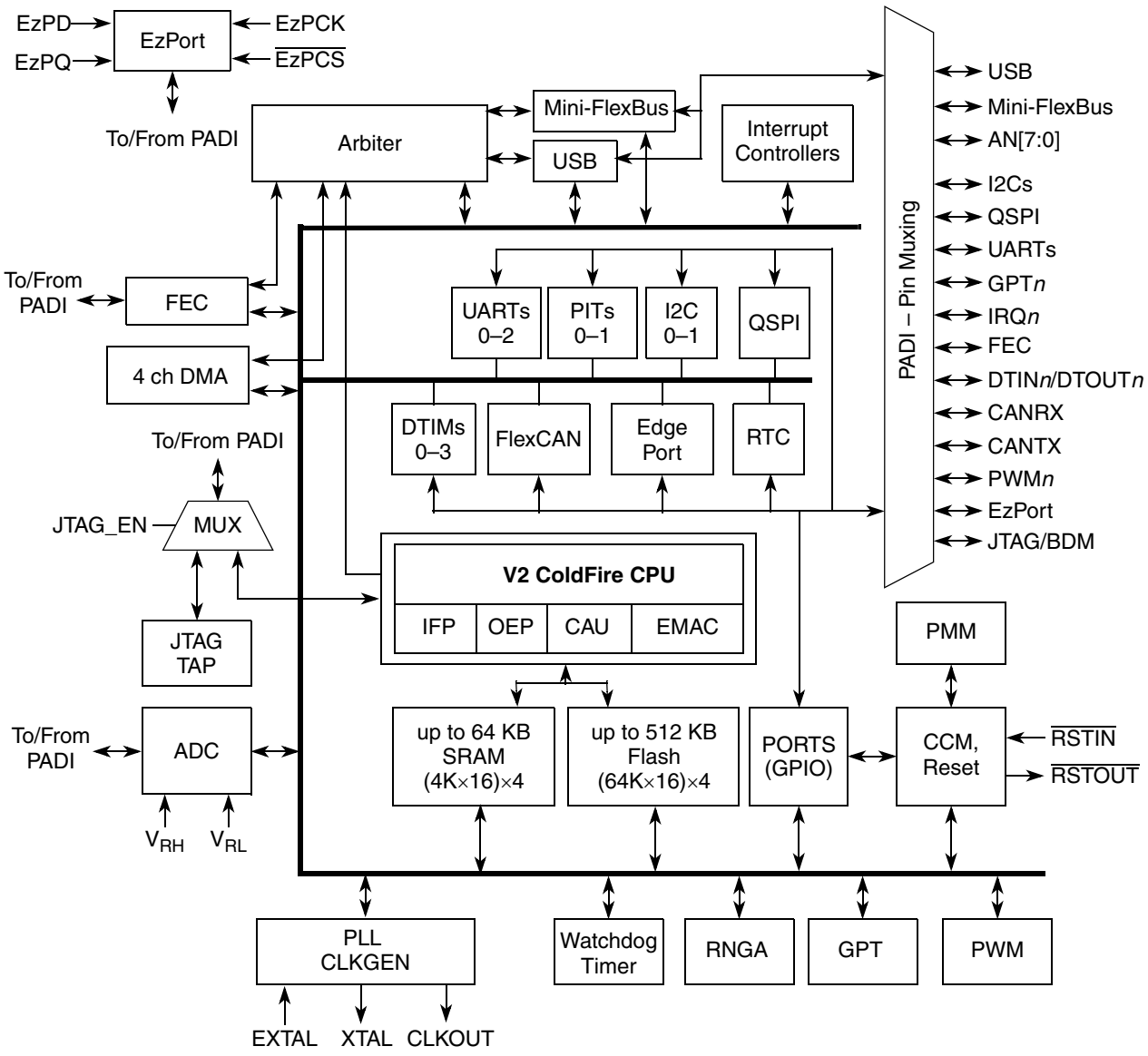

Figure 1. MCF52259 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip

  - Up to 80 MHz processor core frequency
  - 40 MHz or 33 MHz peripheral bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support 16×16 → 32 or 32×32 → 48 operations
  - Cryptographic Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
  - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/s
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points

  - DMA or FIFO data stream interfaces
  - Low power consumption
  - OTG protocol logic
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
- Mini-FlexBus
  - External bus interface available on 144 pin packages
  - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
  - 2 chip selects ($\overline{\text{FB\_CS}}$[1:0])
  - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
  - Multiplexed mode: 16-bit data and 20-bit address bus
  - FB_CLK output to support synchronous memories
  - Programmable base address, size, and wait states to support slow peripherals
  - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- Two I2C modules
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 μs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.27 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

1.2.28 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable part number summary

Freescale Part Number	FlexCAN	Encryption	Speed (MHz)	Flash (KB)	SRAM (KB)	Package	Temp range (°C)
MCF52252AF80	—	—	80	256	32	100 LQFP	0 to +70
MCF52252CAF66	•	—	66				-40 to +85
MCF52254AF80	—	—	80	512	64	100 LQFP	0 to +70
MCF52254CAF66	•	—	66				-40 to +85
MCF52255CAF80	•	•	80	512	64	100 LQFP	-40 to +85
MCF52256AG80	—	—	80	256	32	144 LQFP	0 to +70
MCF52256CAG66	•	—	66		64		-40 to +85
MCF52256CVN66	•	—	66		64	144 MAPBGA	-40 to +85
MCF52256VN80	—	—	80		32		0 to +70
MCF52258AG80	—	—	80	512	64	144 LQFP	0 to +70
MCF52258CAG66	•	—	66				-40 to +85
MCF52258CVN66	•	—	66			144 MAPBGA	-40 to +85
MCF52258VN80	—	—	80				0 to +70
MCF52259CAG80	•	•	80	512	64	144 LQFP	-40 to +85
MCF52259CVN80	•	•				144 MAPBGA	-40 to +85

Figure 2 shows the pinout configuration for the 144 LQFP.

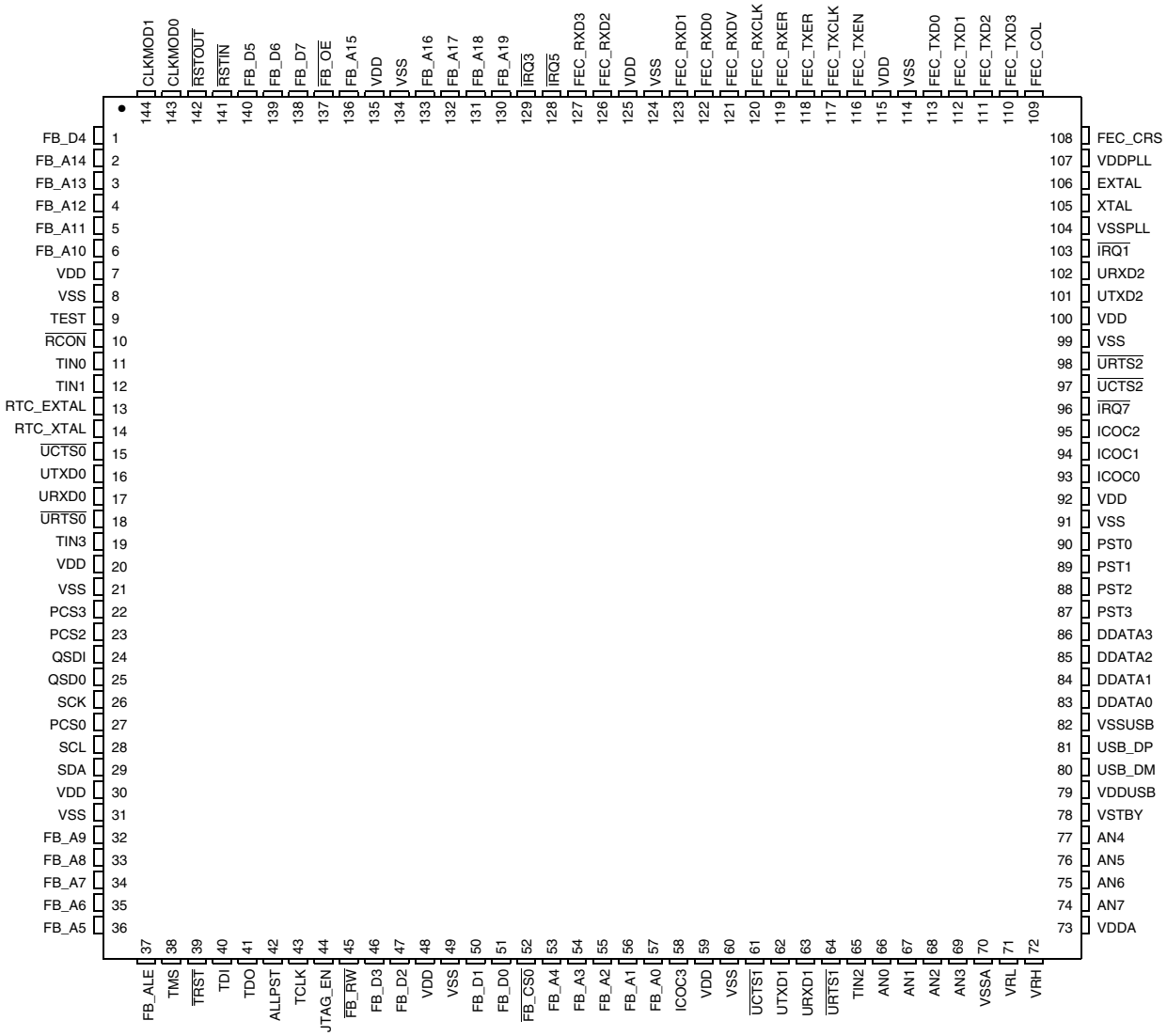

Figure 2. 144 LQFP Pin Assignment

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_ RXD0	FEC_ RXER	FEC_ TXEN	FEC_ TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_ RXD1	FEC_ RXCLK	FEC_ TXCLK	FEC_ TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_ RXD2	FEC_ RXDV	FEC_ TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_ EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_ RXD3	FEC_ TXER	FEC_ TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_ XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_ EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0[3]	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up[4]	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up[4]	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up[4]	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up[4]	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up[4]	A6	129	96
	IRQ1	—	USB_ALTCLK	PNQ1	Low	High	Pull-Up[4]	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up[5]	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[5]	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	Pull-Up[5]	K1	38	26
	$\overline{\text{TRST}}$/DSCLK	—	—	—	N/A	N/A	Pull-Up[5]	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Timer 1, 32-bit	DTIN1	DTOUT1	PWM2	PTC1	PSRR[17]	PDSR[17]	—	C1	12	6
Timer 0, 32-bit	DTIN0	DTOUT0	PWM0	PTC0	PSRR[16]	PDSR[16]	—	D2	11	5
UART 0	UCTS0	—	USB_VBUSE	PUA3	PSRR[11]	PDSR[11]	—	E2	15	9
	URTS0	—	USB_VBUSD	PUA2	PSRR[10]	PDSR[10]	—	F3	18	12
	URXD0	—	—	PUA1	PSRR[9]	PDSR[9]	—	F2	17	11
	UTXD0	—	—	PUA0	PSRR[8]	PDSR[8]	—	F1	16	10
UART 1	UCTS1	SYNCA	URXD2	PUB3	PSRR[15]	PDSR[15]	—	K7	61	38
	URTS1	SYNCB	UTXD2	PUB2	PSRR[14]	PDSR[14]	—	M8	64	41
	URXD1	I2C_SDA1	—	PUB1	PSRR[13]	PDSR[13]	Pull-Up[6]	L8	63	40
	UTXD1	I2C_SCL1	—	PUB0	PSRR[12]	PDSR[12]	Pull-Up[6]	K8	62	39
UART 2	UCTS2	I2C_SCL1	USB_VBUSCHG	PUC3	PSRR[27]	PDSR[27]	Pull-Up[6]	E11	97	64
	URTS2	I2C_SDA1	USB_VBUSDIS	PUC2	PSRR[26]	PDSR[26]	Pull-Up[6]	E10	98	65
	URXD2	CANRX	—	PUC1	PSRR[25]	PDSR[25]	—	C10	102	69
	UTXD2	CANTX	—	PUC0	PSRR[24]	PDSR[24]	—	D10	101	68
USB OTG	USB_DM	—	—	—	N/A	N/A	—	H11	80	57
	USB_DP	—	—	—	N/A	N/A	—	H12	81	58
	USB_VDD	—	—	—	N/A	N/A	—	J9	79	56
	USB_VSS	—	—	—	N/A	N/A	—	H9	82	59

[16] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[17] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[18] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, W

$P_{I/O}$ = power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 9 and Table 10.

Table 9. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

1 Depending on packaging; see the orderable part number summary (Table 2).

2 Refer to the flash memory section for more information (Section 2.4, “Flash Memory Characteristics”)

Table 10. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

[2] Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 11. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	f_{sys} / 2	MHz
EP1a	EPCK frequency of operation (READ command)	—	f_{sys} / 8	MHz
EP2	EPCS_b negation to next EPCS_b assertion	2 × T_{cyc}	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.6 ESD Protection

Table 12. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD target for Human Body Model	HBM	2000	V
ESD target for Machine Model	MM	200	V
HBM circuit description	R_{series}	1500	Ω
	C	100	pF
MM circuit description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) • Positive pulses • Negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) • Positive pulses • Negative pulses	 — —	 3 3	—
Interval of pulses	—	1	sec

[1] All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.9 USB Operation

Table 15. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys\_USB\_min}$	16	MHz

2.10 Mini-FlexBus External Interface Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 16. Mini-FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	—	80	MHz	
MB1	Clock Period	12.5	—	ns	
MB2	Output Valid	—	8	ns	[1]
MB3	Output Hold	2	—	ns	[1]
MB4	Input Setup	6	—	ns	[2]
MB5	Input Hold	0	—	ns	[2]

[1] Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

[2] Specification is valid for all MB_D[7:0].

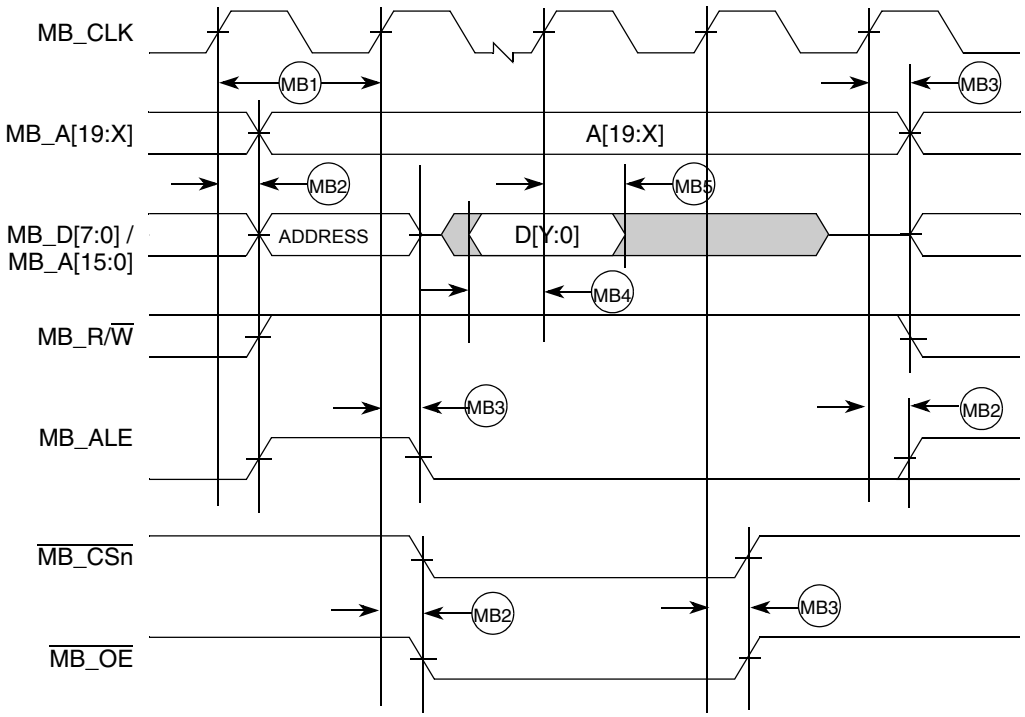

Figure 5. Mini-FlexBus Read Timing

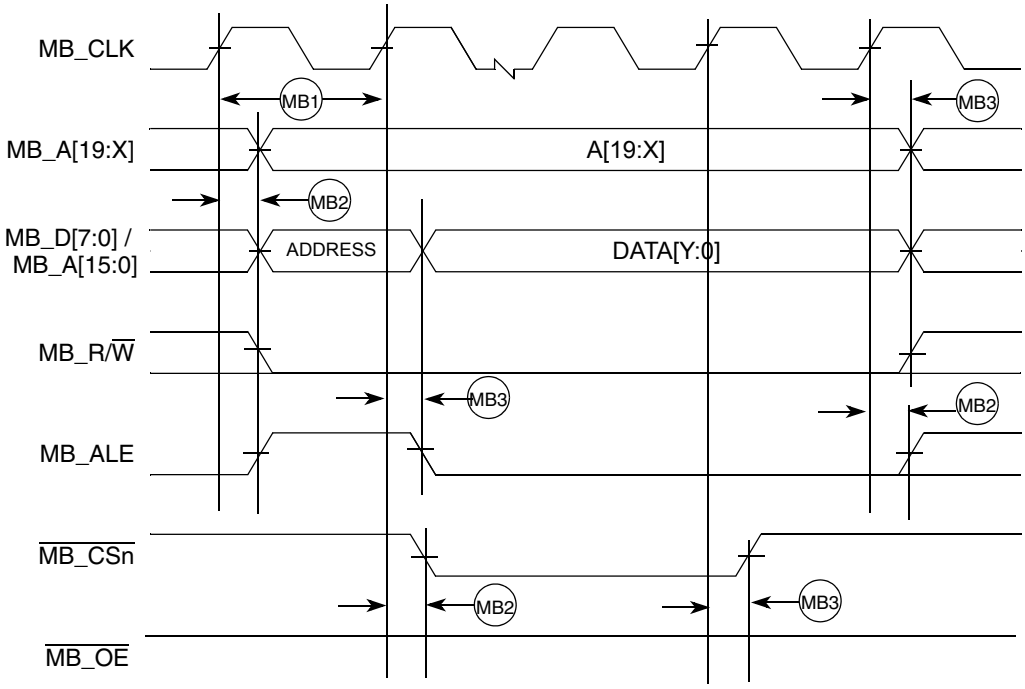

Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

2.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 17. Receive Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	RXCLK frequency	—	25	MHz
E1	RXD[n:0], RXDV, RXER to RXCLK setup[1]	5	—	ns
E2	RXCLK to RXD[n:0], RXDV, RXER hold[1]	5	—	ns
E3	RXCLK pulse width high	35%	65%	RXCLK period
E4	RXCLK pulse width low	35%	65%	RXCLK period

[1] In MII mode, n = 3

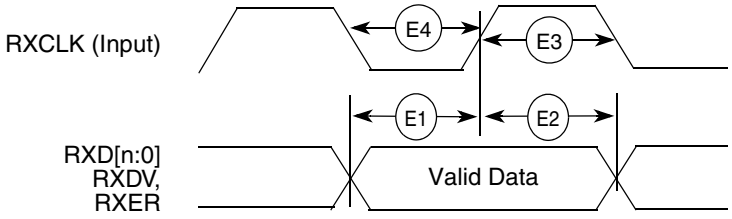

Figure 7. MII Receive Signal Timing Diagram

2.11.2 Transmit Signal Timing Specifications

Table 18. Transmit Signal Timing

Num	Characteristic	MII Mode		Unit
		Min	Max	
—	TXCLK frequency	—	25	MHz
E5	TXCLK to TXD[n:0], TXEN, TXER invalid[1]	5	—	ns
E6	TXCLK to TXD[n:0], TXEN, TXER valid[1]	—	25	ns
E7	TXCLK pulse width high	35%	65%	t_{TXCLK}
E8	TXCLK pulse width low	35%	65%	t_{TXCLK}

[1] In MII mode, n = 3

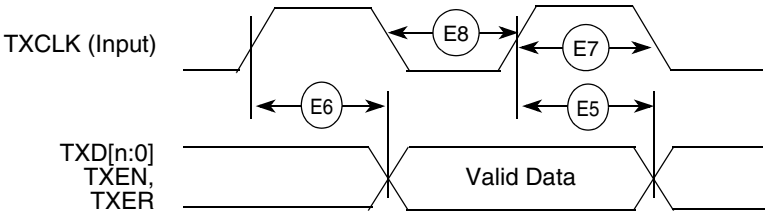

Figure 8. MII Transmit Signal Timing Diagram

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

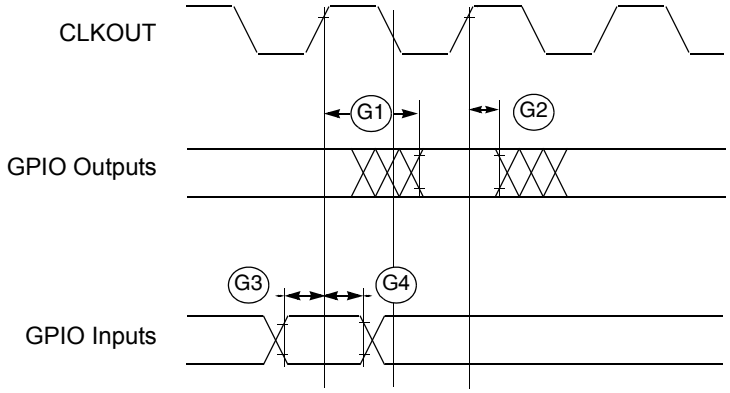

Figure 11. GPIO Timing

2.13 Reset Timing

Table 22. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

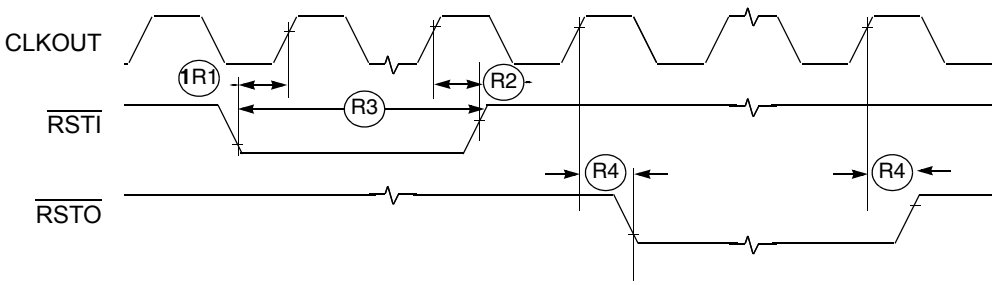

Figure 12. $\overline{RSTI}$ and Configuration Override Timing

2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

Table 26. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

1 All timing references to CLKOUT are given to its rising edge.

2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

Table 27. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.

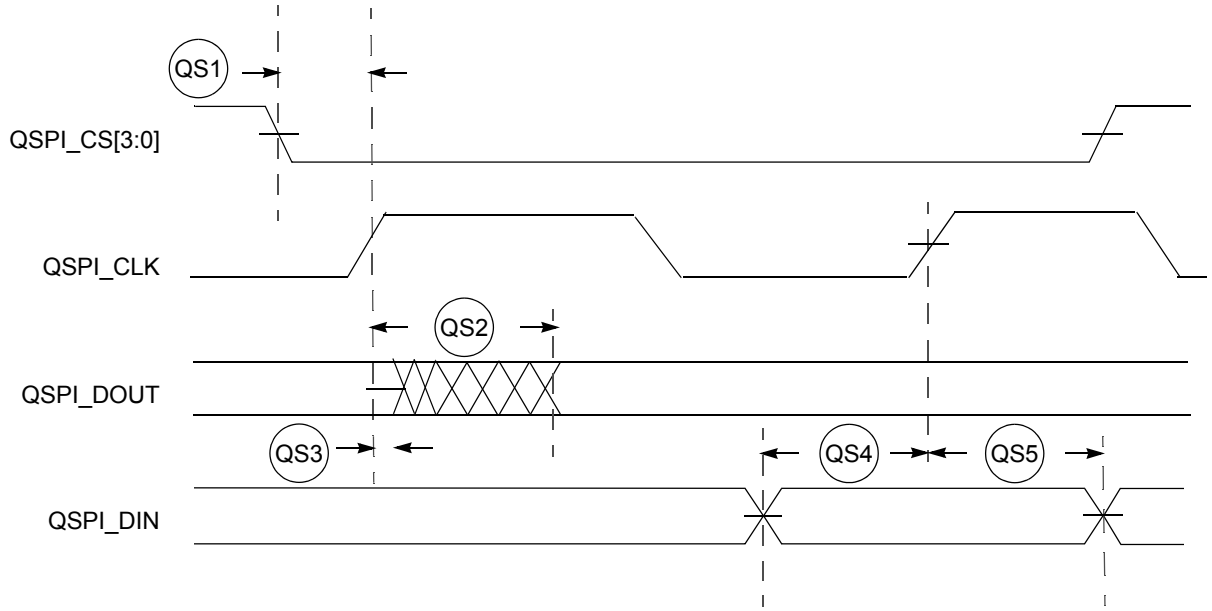

Figure 15. QSPI Timing

2.19 JTAG and Boundary Scan Timing

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

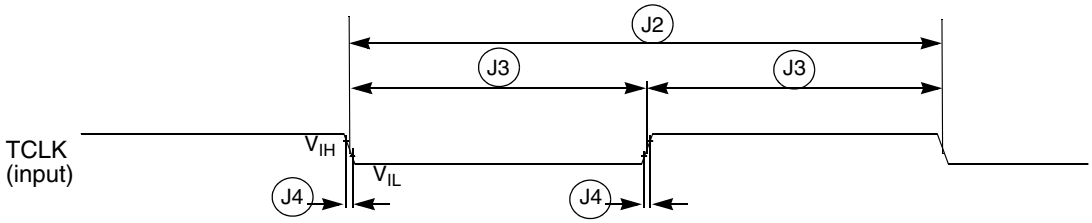

Figure 16. Test Clock Input Timing

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	• Added package dimensions to package diagrams • Added listing of devices for MCF52259 family • Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation” • Updated the figure **Pinout Top View (144 MAPBGA)** • Removed an extraneous instance of the table **Pin Functions by Primary and Alternate Purpose** • In the table **Pin Functions by Primary and Alternate Purpose**, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL” • In the table **SGFM Flash Program and Erase Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **SGFM Flash Module Life Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **Oscillator and PLL Specifications**, changed “V_{DD} and V_{DDPLL} = 2.7 to 3.6 V“ to “V_{DD} and V_{DDPLL} = 3.0 to 3.6 V“ • In the table **Reset and Configuration Override Timing**, changed “V_{DD} = 2.7 to 3.6 V“ to “V_{DD} = 3.0 to 3.6 V“
2	• Added EzPort Electrical Specifications. • Updated Table 2 for part numbers. • In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values,JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. • Updated Table 14. • Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). • Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	• Updated EzPort Electrical Specifications • Added hysteresis note in the DC electrical table • Clarified pin function table for VSS pins. • Clarified orderable part summary.
4	• Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, “This value has been update” • Updated crystal frequency value to 25 MHz
5	• Updated TOC

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