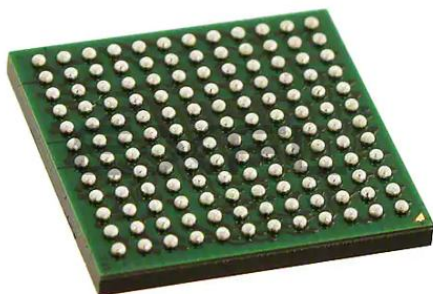


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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52256vn80j

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1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz ¹		up to 80 MHz ¹	up to 66 or 80 MHz ¹		up to 80 MHz ¹
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

¹ 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

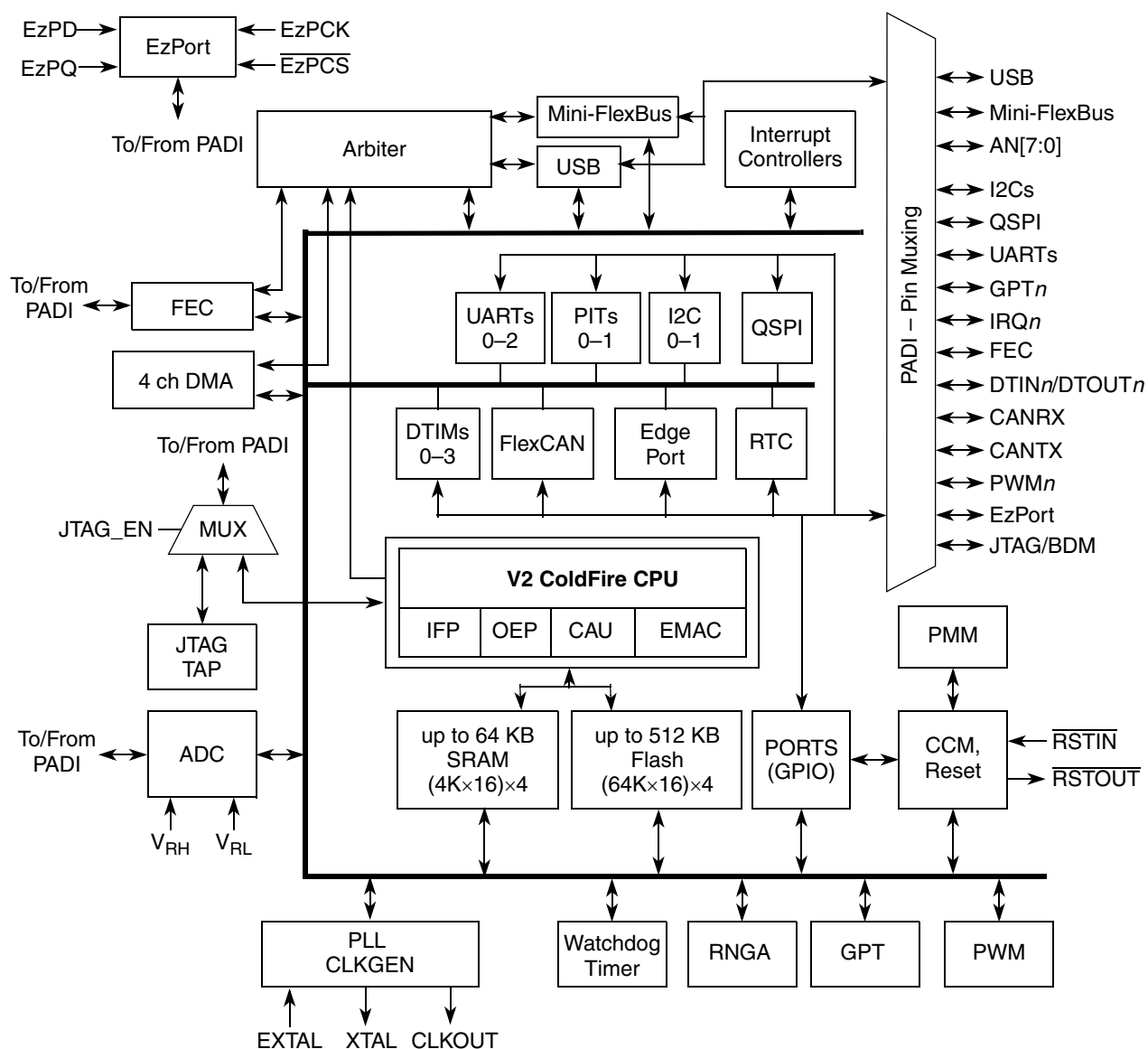


Figure 1. MCF52259 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip

- DMA or FIFO data stream interfaces
- Low power consumption
- OTG protocol logic
- Fast Ethernet controller (FEC)
 - 10/100 BaseT/TX capability, half duplex or full duplex
 - On-chip transmit and receive FIFOs
 - Built-in dedicated DMA controller
 - Memory-based flexible descriptor rings
- Mini-FlexBus
 - External bus interface available on 144 pin packages
 - Supports glueless interface with 8-bit ROM/flash/SRAM/simple slave peripherals. Can address up to 2 MB of addresses
 - 2 chip selects ($\overline{\text{FB_CS}}[1:0]$)
 - Non-multiplexed mode: 8-bit dedicated data bus, 20-bit address bus
 - Multiplexed mode: 16-bit data and 20-bit address bus
 - FB_CLK output to support synchronous memories
 - Programmable base address, size, and wait states to support slow peripherals
 - Operates at up to 40 MHz (bus clock) in 1:2 mode or up to 80 MHz (core clock) in 1:1 mode
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- Two I2C modules
 - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
 - Fully compatible with industry-standard I2C bus
 - Master and slave modes support multiple masters
 - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to three chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution
 - Minimum 1.125 μs conversion time
 - Simultaneous sampling of two channels for motor control applications
 - Single-scan or continuous operation
 - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit

Family Configurations

- Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
 - 12.5 ns resolution at 80 MHz
 - Programmable sources for clock input, including an external clock option
 - Programmable prescaler
 - Input capture capability with programmable trigger edge on input pin
 - Output compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts on input capture or output compare
 - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
 - 16-bit architecture
 - Programmable prescaler
 - Output pulse-widths variable from microseconds to seconds
 - Single 16-bit input pulse accumulator
 - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
 - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
 - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
 - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
 - Programmable period and duty cycle
 - Programmable enable/disable for each channel
 - Software selectable polarity for each channel
 - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
 - Programmable center or left aligned outputs on individual channels
 - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
 - Emergency shutdown
- Two periodic interrupt timers (PITs)
 - 16-bit counter
 - Selectable as free running or count down
- Real-Time Clock (RTC)
 - Maintains system time-of-day clock
 - Provides stopwatch and alarm interrupt functions
 - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
 - 32-bit counter
 - Low-power mode support
- Backup watchdog timer (BWT)
 - Independent timer that can be used to help software recover from runaway code
 - 16-bit counter
 - Low-power mode support
- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator

- Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
- System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
- Low power modes supported
- 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
 - Uniquely programmable vectors for all interrupt sources
 - Fully programmable level and priority for all peripheral interrupt sources
 - Seven external interrupt signals with fixed level and priority
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low-power modes
- DMA controller
 - Four fully programmable channels
 - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
 - Source/destination address pointers that can increment or remain constant
 - 24-bit byte transfer counter per channel
 - Auto-alignment transfers supported for efficient block movement
 - Bursting and cycle-steal support
 - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
 - Channel linking support
- Reset
 - Separate reset in and reset out signals
 - Seven sources of reset:
 - Power-on reset (POR)
 - External
 - Software
 - Watchdog
 - Loss of clock / loss of lock
 - Low-voltage detection (LVD)
 - JTAG
 - Status flag indication of source of last reset
- Chip configuration module (CCM)
 - System configuration during reset
 - Selects one of six clock modes
 - Configures output pad drive strength
 - Unique part identification number and part revision number
- General purpose I/O interface
 - Up to 56 bits of general purpose I/O on 100-pin package
 - Up to 96 bits of general purpose I/O on 144-pin package
 - Bit manipulation supported via set/clear functions
 - Programmable drive strengths
 - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.24 Interrupt Controllers (INTC_n)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR_n[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/ Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0 ³	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up ⁴	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up ⁴	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up ⁴	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up ⁴	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up ⁴	A6	129	96
	IRQ1	—	USB_ALT CLK	PNQ1	Low	High	Pull-Up ⁴	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up ⁵	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up ⁵	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/BKPT	—	—	—	N/A	N/A	Pull-Up ⁵	K1	38	26
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up ⁵	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mode Selection	RCON/EZPCS	—	—	—	N/A	N/A	Pull-Up	E4	10	4
	CLKMOD[1:0]	—	—	—	N/A	N/A	Pull-Down	D4, D5	144, 143	100, 99
QSPI	QSPI_CS3	SYNCA	USB_DP_PDOWN	PQS6	PSRR[7]	PDSR[7]	—	G4	22	16
	QSPI_CS2	SYNCB	USB_DM_PDOWN	PQS5	PSRR[6]	PDSR[6]	—	G3	23	17
	QSPI_CS0	I2C_SDA0	UCTS1	PQS3	PSRR[4]	PDSR[4]	Pull-Up ⁶	H4	27	21
	QSPI_CLK/EZPCK	I2C_SCL0	URTS1	PQS2	PSRR[3]	PDSR[3]	Pull-Up ⁶	H3	26	20
QSPI	QSPI_DIN/EZPD	I2C_SDA1	URXD1	PQS1	PSRR[2]	PDSR[2]	Pull-Up ⁶	G2	24	18
	QSPI_DOUT/EZPQ	I2C_SCL1	UTXD1	PQS0	PSRR[1]	PDSR[1]	Pull-Up ⁶	G1	25	19
Reset ⁷	RSTI	—	—	—	N/A	N/A	Pull-Up ⁷	A3	141	97
	RSTO	—	—	—	Low	High	—	A2	142	98
Test	TEST	—	—	—	N/A	N/A	Pull-Down	B1	9	3
Timer 3, 16-bit	GPT3	—	PWM7	PTA3	PSRR[23]	PDSR[23]	Pull-Up ⁸	M7	58	35
Timer 2, 16-bit	GPT2	—	PWM5	PTA2	PSRR[22]	PDSR[22]	Pull-Up ⁸	J10	95	62
Timer 1, 16-bit	GPT1	—	PWM3	PTA1	PSRR[21]	PDSR[21]	Pull-Up ⁸	J11	94	61
Timer 0, 16-bit	GPT0	—	PWM1	PTA0	PSRR[20]	PDSR[20]	Pull-Up ⁸	F12	93	60
Timer 3, 32-bit	DTIN3	DTOUT3	PWM6	PTC3	PSRR[19]	PDSR[19]	—	F4	19	13
Timer 2, 32-bit	DTIN2	DTOUT2	PWM4	PTC2	PSRR[18]	PDSR[18]	—	J8	65	42

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Timer 1, 32-bit	DTIN1	DTOUT1	PWM2	PTC1	PSRR[17]	PDSR[17]	—	C1	12	6
Timer 0, 32-bit	DTIN0	DTOUT0	PWM0	PTC0	PSRR[16]	PDSR[16]	—	D2	11	5
UART 0	UCTS0	—	USB_VBUS _{SE}	PUA3	PSRR[11]	PDSR[11]	—	E2	15	9
	URTS0	—	USB_VBUS _{SD}	PUA2	PSRR[10]	PDSR[10]	—	F3	18	12
	URXD0	—	—	PUA1	PSRR[9]	PDSR[9]	—	F2	17	11
	UTXD0	—	—	PUA0	PSRR[8]	PDSR[8]	—	F1	16	10
UART 1	UCTS1	SYNCA	URXD2	PUB3	PSRR[15]	PDSR[15]	—	K7	61	38
	URTS1	SYNCB	UTXD2	PUB2	PSRR[14]	PDSR[14]	—	M8	64	41
	URXD1	I2C_SDA1	—	PUB1	PSRR[13]	PDSR[13]	Pull-Up ⁶	L8	63	40
	UTXD1	I2C_SCL1	—	PUB0	PSRR[12]	PDSR[12]	Pull-Up ⁶	K8	62	39
UART 2	UCTS2	I2C_SCL1	USB_VBUSCH _G	PUC3	PSRR[27]	PDSR[27]	Pull-Up ⁶	E11	97	64
	URTS2	I2C_SDA1	USB_VBUSDIS	PUC2	PSRR[26]	PDSR[26]	Pull-Up ⁶	E10	98	65
	URXD2	CANRX	—	PUC1	PSRR[25]	PDSR[25]	—	C10	102	69
	UTXD2	CANTX	—	PUC0	PSRR[24]	PDSR[24]	—	D10	101	68
USB OTG	USB_DM	—	—	—	N/A	N/A	—	H11	80	57
	USB_DP	—	—	—	N/A	N/A	—	H12	81	58
	USB_VDD	—	—	—	N/A	N/A	—	J9	79	56
	USB_VSS	—	—	—	N/A	N/A	—	H9	82	59

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	−0.3 to +4.0	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 or 0 to 70 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see orderable part number summary ([Table 2](#))

Table 7. Current Consumption in Low-Power Mode, Code From SRAM^{1,2,3}

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11) ⁴	0.090				mA	I _{DD}
Stop mode 2 (Stop 10) ⁴	7					
Stop mode 1 (Stop 01) ^{4,5}	9	10	15	17		
Stop mode 0 (Stop 00) ⁵	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

¹ All values are measured with a 3.3 V power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.

³ CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.

⁴ See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.

⁵ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

Table 8. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	30 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	43 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	26 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	16 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	44 ^{7,8}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{1,9}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	35 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	23 ¹⁰	°C/W
	Junction to case	—	θ_{JC}	7 ¹¹	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹²	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{13,14}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,15}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ¹⁶	°C/W
	Junction to case	—	θ_{JC}	9 ¹⁷	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹⁸	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

¹ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

³ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

⁴ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

⁷ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

⁸ Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

⁹ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

¹⁰ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

¹¹ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

¹² Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

¹³ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

¹⁴ Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

¹⁵ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications ¹

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis ²	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS} , digital pins	I_{in}	-1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = -2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$ mA	V_{OL}	—	0.5	V
Output high voltage (high drive) $I_{OH} = -5$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5$ mA	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (low drive) $I_{OL} = 2$ mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max. ³	I_{APU}	-10	-130	μA
Input Capacitance ⁴ • All input-only pins • All input/output (three-state) pins	C_{in}	— —	7 7	pF

¹ Refer to Table 14 for additional PLL specifications.

² Only for pins: IRQ1, IRQ3, IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

³ Refer to Table 3 for pins having internal pull-up devices.

⁴ This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 14. Oscillator and PLL Specifications
 $(V_{DD} \text{ and } V_{DDPLL} = 3.0 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	f_{crystal} f_{ext}	12 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	$f_{\text{ref_pll}}$	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{\text{ref}} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4,9}	t_{lpll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK range	f_{UL}	−1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	−0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary (Table 2).

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

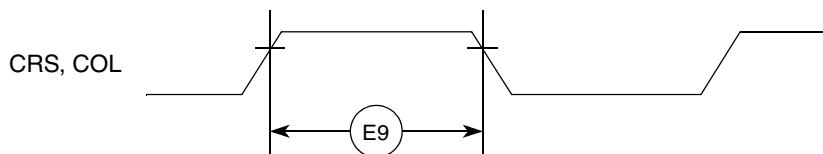


Figure 9. MII Async Inputs Timing Diagram

2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

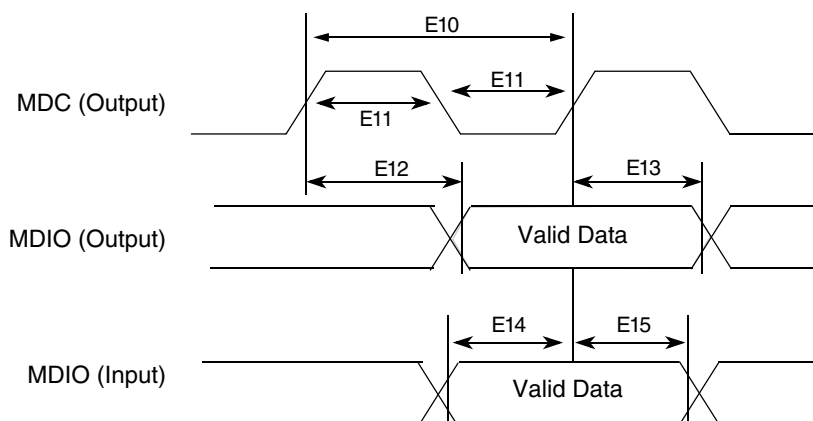


Figure 10. MII Serial Management Channel Timing Diagram

2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in [Table 21](#) and [Figure 11](#).

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys}/2$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	\overline{TRST} assert time	t_{TRSTAT}	100	—	ns
J14	\overline{TRST} setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

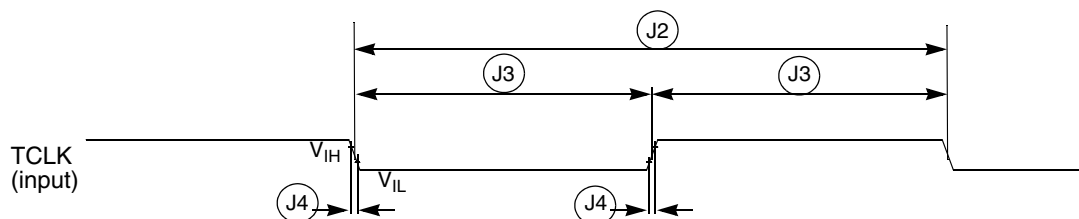


Figure 16. Test Clock Input Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

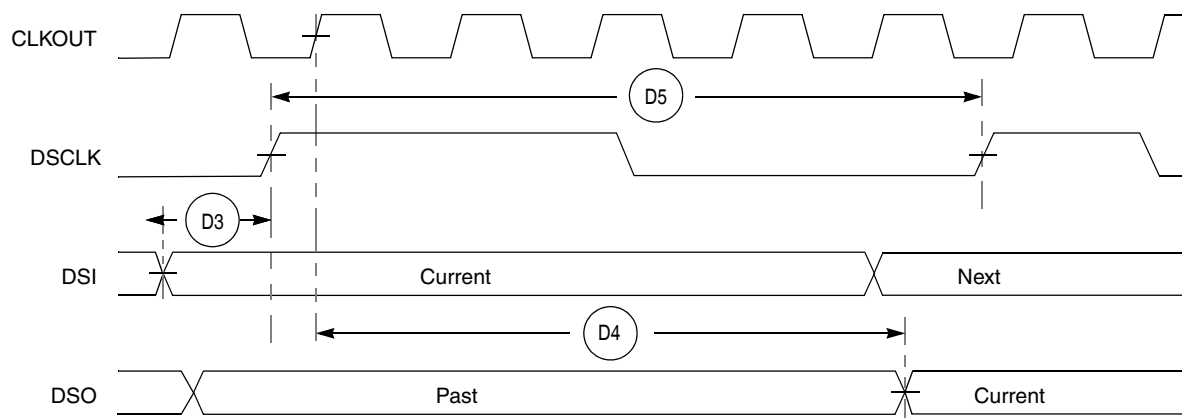


Figure 21. BDM Serial Port AC Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on <http://www.freescale.com/coldfire>. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W
MCF52258		
MCF52259		98ASH70694A

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Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

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Exchange Building 23F
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Chaoyang District
Beijing 100022
China
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