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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52258cag66

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1 Family Configurations

Table 1. MCF52259 Family Configurations

Module	52252	52254	52255	52256	52258	52259
Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit)	•	•	•	•	•	•
System Clock	up to 66 or 80 MHz[1]		up to 80 MHz[1]	up to 66 or 80 MHz[1]		up to 80 MHz[1]
Performance (Dhrystone 2.1 MIPS)	up to 63 or 76					
Flash	256 KB	512 KB	512 KB	256 KB	512 KB	512 KB
Static RAM (SRAM)	32 KB	64 KB	64 KB	32 / 64 KB	64 KB	64 KB
Two Interrupt Controllers (INTC)	•	•	•	•	•	•
Fast Analog-to-Digital Converter (ADC)	•	•	•	•	•	•
USB On-The-Go (USB OTG)	•	•	•	•	•	•
Mini-FlexBus external bus interface	—	—	—	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•	•
Random Number Generator and Cryptographic Acceleration Unit (CAU)	—	—	•	—	—	•
FlexCAN 2.0B Module	Varies	Varies	•	Varies	Varies	•
Four-channel Direct-Memory Access (DMA)	•	•	•	•	•	•
Software Watchdog Timer (WDT)	•	•	•	•	•	•
Secondary Watchdog Timer	•	•	•	•	•	•
Two-channel Periodic Interrupt Timer (PIT)	2	2	2	2	2	2
Four-Channel General Purpose Timer (GPT)	•	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4	4
QSPI	•	•	•	•	•	•
UART(s)	3	3	3	3	3	3
I2C	2	2	2	2	2	2
Eight/Four-channel 8/16-bit PWM Timer	•	•	•	•	•	•
General Purpose I/O Module (GPIO)	•	•	•	•	•	•
Chip Configuration and Reset Controller Module	•	•	•	•	•	•
Background Debug Mode (BDM)	•	•	•	•	•	•
JTAG - IEEE 1149.1 Test Access Port	•	•	•	•	•	•
Package	100 LQFP			144 LQFP or 144 MAPBGA		

[1] 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

  - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
  - 12.5 ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse-widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
  - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Backup watchdog timer (BWT)
  - Independent timer that can be used to help software recover from runaway code
  - 16-bit counter
  - Low-power mode support
- Clock generation features
  - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator

  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($0 \le n \le 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O on 100-pin package
  - Up to 96 bits of general purpose I/O on 144-pin package
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 64 KB memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64 KB boundary within the 4 GB address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA, FEC, and USB. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor’s high-speed local bus. The CFM is constructed with four banks of 64 KB×16-bit flash memory arrays to generate 512 KB of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Cryptographic Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

Figure 2 shows the pinout configuration for the 144 LQFP.

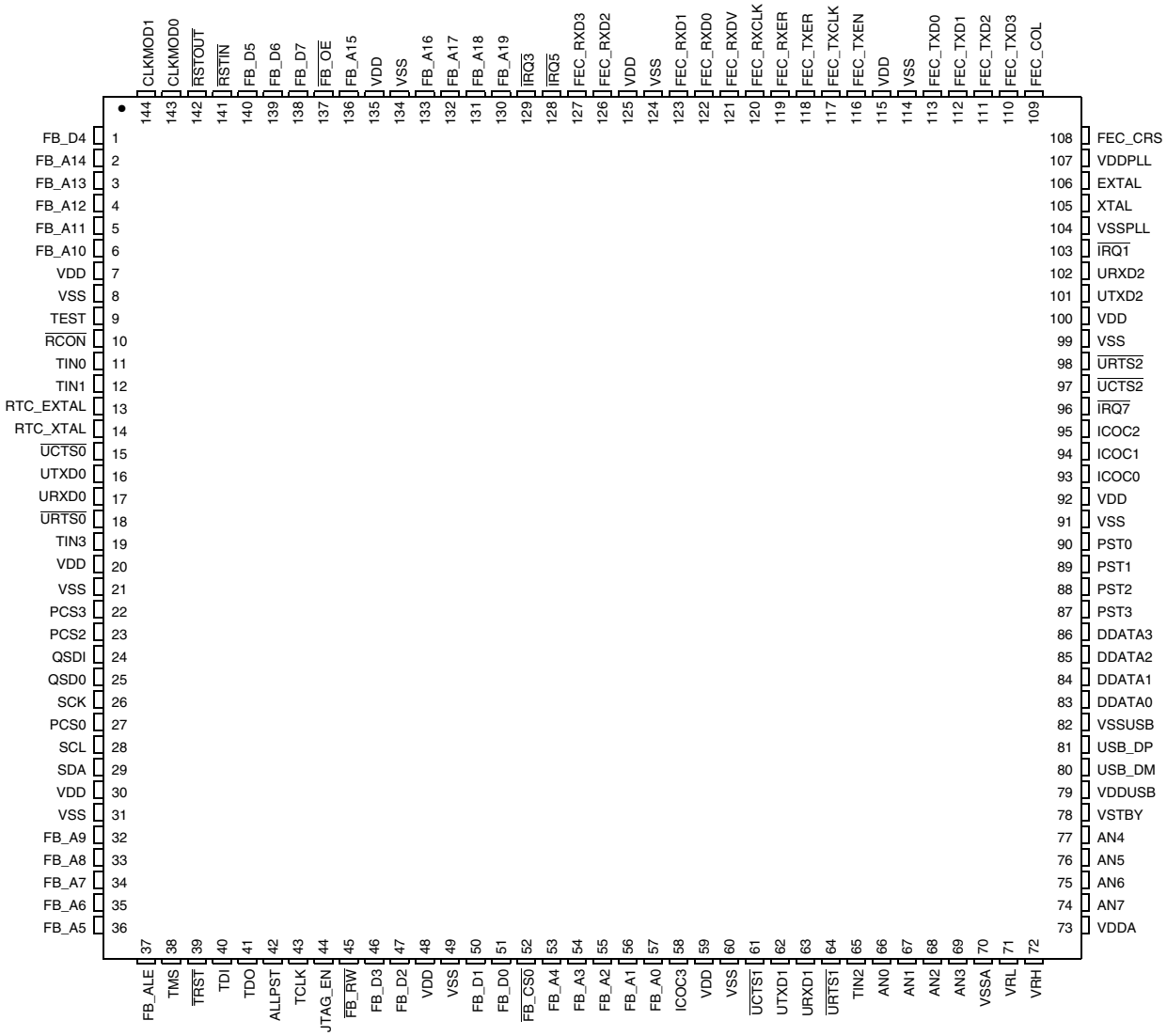


Figure 2. 144 LQFP Pin Assignment

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_ RXD0	FEC_ RXER	FEC_ TXEN	FEC_ TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_ RXD1	FEC_ RXCLK	FEC_ TXCLK	FEC_ TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_ RXD2	FEC_ RXDV	FEC_ TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_ EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_ RXD3	FEC_ TXER	FEC_ TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_ XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_ EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mode Selection	$\overline{\text{RCON}}$/$\overline{\text{EZPCS}}$	—	—	—	N/A	N/A	Pull-Up	E4	10	4
	CLKMOD[1:0]	—	—	—	N/A	N/A	Pull-Down	D4, D5	144, 143	100, 99
QSPI	QSPI_CS3	SYNCA	USB_DP_PDOWN	PQS6	PSRR[7]	PDSR[7]	—	G4	22	16
	QSPI_CS2	SYNCB	USB_DM_PDOWN	PQS5	PSRR[6]	PDSR[6]	—	G3	23	17
	QSPI_CS0	I2C_SDA0	UCTS1	PQS3	PSRR[4]	PDSR[4]	Pull-Up[6]	H4	27	21
	QSPI_CLK/ EZPCK	I2C_SCL0	URTS1	PQS2	PSRR[3]	PDSR[3]	Pull-Up[6]	H3	26	20
QSPI	QSPI_DIN/ EZPD	I2C_SDA1	URXD1	PQS1	PSRR[2]	PDSR[2]	Pull-Up[6]	G2	24	18
	QSPI_DOUT/EZPQ	I2C_SCL1	UTXD1	PQS0	PSRR[1]	PDSR[1]	Pull-Up[6]	G1	25	19
Reset[7]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	Pull-Up[7]	A3	141	97
	$\overline{\text{RSTO}}$	—	—	—	Low	High	—	A2	142	98
Test	TEST	—	—	—	N/A	N/A	Pull-Down	B1	9	3
Timer 3, 16-bit	GPT3	—	PWM7	PTA3	PSRR[23]	PDSR[23]	Pull-Up[8]	M7	58	35
Timer 2, 16-bit	GPT2	—	PWM5	PTA2	PSRR[22]	PDSR[22]	Pull-Up[8]	J10	95	62
Timer 1, 16-bit	GPT1	—	PWM3	PTA1	PSRR[21]	PDSR[21]	Pull-Up[8]	J11	94	61
Timer 0, 16-bit	GPT0	—	PWM1	PTA0	PSRR[20]	PDSR[20]	Pull-Up[8]	F12	93	60
Timer 3, 32-bit	DTIN3	DTOUT3	PWM6	PTC3	PSRR[19]	PDSR[19]	—	F4	19	13
Timer 2, 32-bit	DTIN2	DTOUT2	PWM4	PTC2	PSRR[18]	PDSR[18]	—	J8	65	42

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Timer 1, 32-bit	DTIN1	DTOUT1	PWM2	PTC1	PSRR[17]	PDSR[17]	—	C1	12	6
Timer 0, 32-bit	DTIN0	DTOUT0	PWM0	PTC0	PSRR[16]	PDSR[16]	—	D2	11	5
UART 0	UCTS0	—	USB_VBUSE	PUA3	PSRR[11]	PDSR[11]	—	E2	15	9
	URTS0	—	USB_VBUSD	PUA2	PSRR[10]	PDSR[10]	—	F3	18	12
	URXD0	—	—	PUA1	PSRR[9]	PDSR[9]	—	F2	17	11
	UTXD0	—	—	PUA0	PSRR[8]	PDSR[8]	—	F1	16	10
UART 1	UCTS1	SYNCA	URXD2	PUB3	PSRR[15]	PDSR[15]	—	K7	61	38
	URTS1	SYNCB	UTXD2	PUB2	PSRR[14]	PDSR[14]	—	M8	64	41
	URXD1	I2C_SDA1	—	PUB1	PSRR[13]	PDSR[13]	Pull-Up[6]	L8	63	40
	UTXD1	I2C_SCL1	—	PUB0	PSRR[12]	PDSR[12]	Pull-Up[6]	K8	62	39
UART 2	UCTS2	I2C_SCL1	USB_VBUSCHG	PUC3	PSRR[27]	PDSR[27]	Pull-Up[6]	E11	97	64
	URTS2	I2C_SDA1	USB_VBUSDIS	PUC2	PSRR[26]	PDSR[26]	Pull-Up[6]	E10	98	65
	URXD2	CANRX	—	PUC1	PSRR[25]	PDSR[25]	—	C10	102	69
	UTXD2	CANTX	—	PUC0	PSRR[24]	PDSR[24]	—	D10	101	68
USB OTG	USB_DM	—	—	—	N/A	N/A	—	H11	80	57
	USB_DP	—	—	—	N/A	N/A	—	H12	81	58
	USB_VDD	—	—	—	N/A	N/A	—	J9	79	56
	USB_VSS	—	—	—	N/A	N/A	—	H9	82	59

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
VSS	VSS	—	—	—	N/A	N/A	—	A1; A12; F6–8; G6–8; H8; M1	8; 21; 31; 49; 60; 91; 99; 114; 124; 134	2; 15; 25; 34; 37; 66; 81; 91

1 The PDSR and PSSR registers are part of the GPIO module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 I2C1 is multiplexed with specific pins of the QSPI, UART1, UART2, and Mini-FlexBus pin groups.
4 For primary and GPIO functions only.
5 Only when JTAG mode is enabled.
6 For secondary and GPIO functions only.
7 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
8 For GPIO functions, the Primary Function has pull-up control within the GPT module.
9 Available on 144-pin packages only.
10 This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL.

2.2 Current Consumption

Table 5. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical[1] Active (SRAM)	Typical[1] Active (Flash)	Peak[2] (Flash)	Unit
PLL @ 8 MHz	I_{DD}	22	30	36	mA
PLL @ 16 MHz		31	45	60	
PLL @ 64 MHz		84	100	155	
PLL @ 80 MHz		102	118	185	
RAM standby supply current • Normal operation: $V_{DD} > V_{STBY}$ - 0.3 V • Standby operation: $V_{DD} < V_{SS}$ + 0.5 V	I_{STBY}	— —		5 20	μA μA
Analog supply current • Normal operation	I_{DDA}	2 [3]		15	mA
USB supply current	I_{DDUSB}	—		2	mA
PLL supply current	I_{DDPLL}	—		6 [4]	mA

1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).

2 Peak current measured with all modules active, CPU polling a status register, and default drive strength with matching load.

3 Tested using Auto Power Down (APD), which powers down the ADC between conversions; ADC running at 4 MHz in Once Parallel mode with a sample rate of 3 kHz.

4 Tested with the PLL MFD set to 7 (max value). Setting the MFD to a lower value results in lower current consumption.

Table 6. Current Consumption in Low-Power Mode, Code From Flash Memory[1,2,3]

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11)[4]	0.150				mA	I_{DD}
Stop mode 2 (Stop 10)[4]	7.0					
Stop mode 1 (Stop 01)[4,5]	9	10	15	17		
Stop mode 0 (Stop 00)[5]	9	10	15	17		
Wait / Doze	21	32	56	65		
Run	23	36	70	81		

1 All values are measured with a 3.30 V power supply. Tests performed at room temperature.

2 Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.

3 CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 and CFM off before entering low-power mode. CLKOUT is disabled.

4 See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.

5 Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

[16] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[17] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[18] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, W

$P_{I/O}$ = power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 9 and Table 10.

Table 9. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

1 Depending on packaging; see the orderable part number summary (Table 2).

2 Refer to the flash memory section for more information (Section 2.4, “Flash Memory Characteristics”)

Table 10. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

Figure 13 shows timing for the values in Table 23 and Table 24.

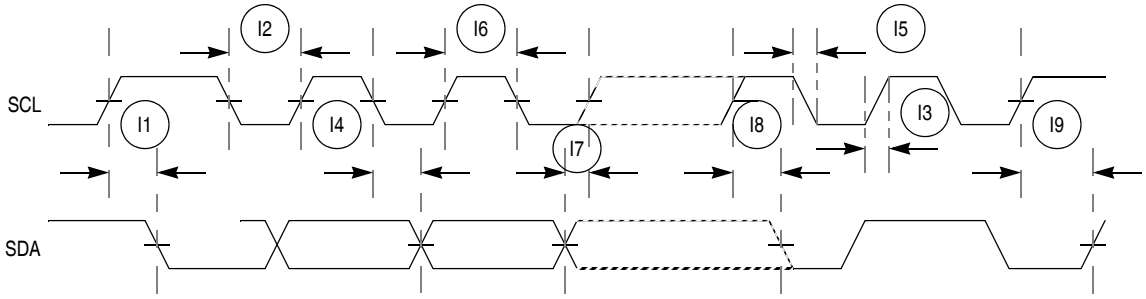


Figure 13. I2C Input/Output Timings

2.15 Analog-to-Digital Converter (ADC) Parameters

Table 25 lists specifications for the analog-to-digital converter.

Table 25. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SSA}	—	V_{SSA} + 50 mV	V
V_{REFH}	High reference voltage	V_{DDA} - 50 mV	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.1	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 14	—	pF
X_{IN}	Input impedance	—	See Figure 14	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV

Table 25. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

1 All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3 V, V_{REFH} = 3.3 V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

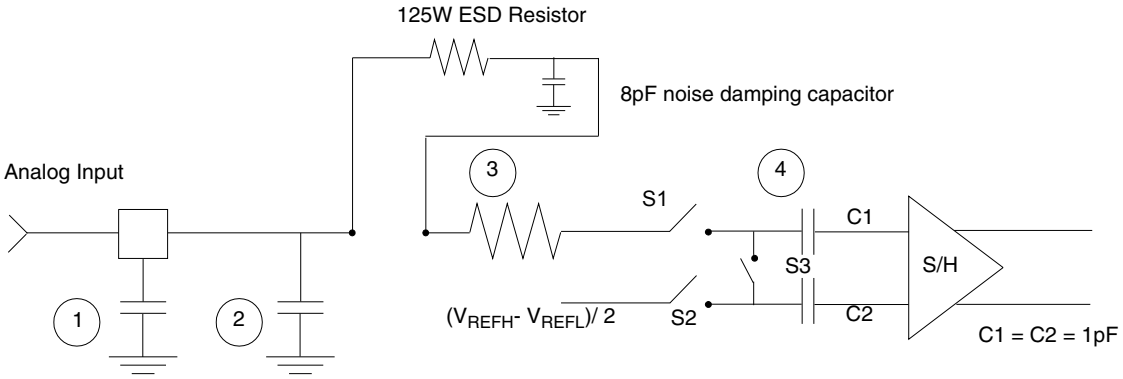
5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

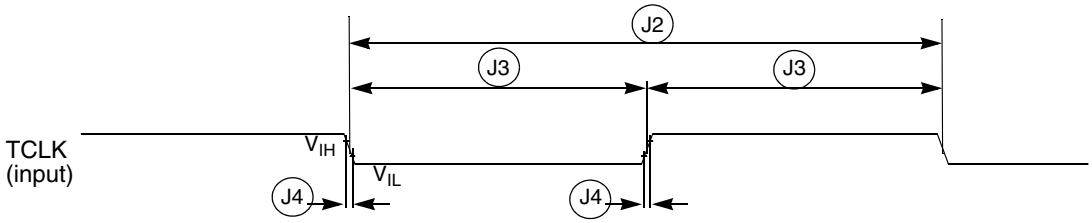


Figure 16. Test Clock Input Timing

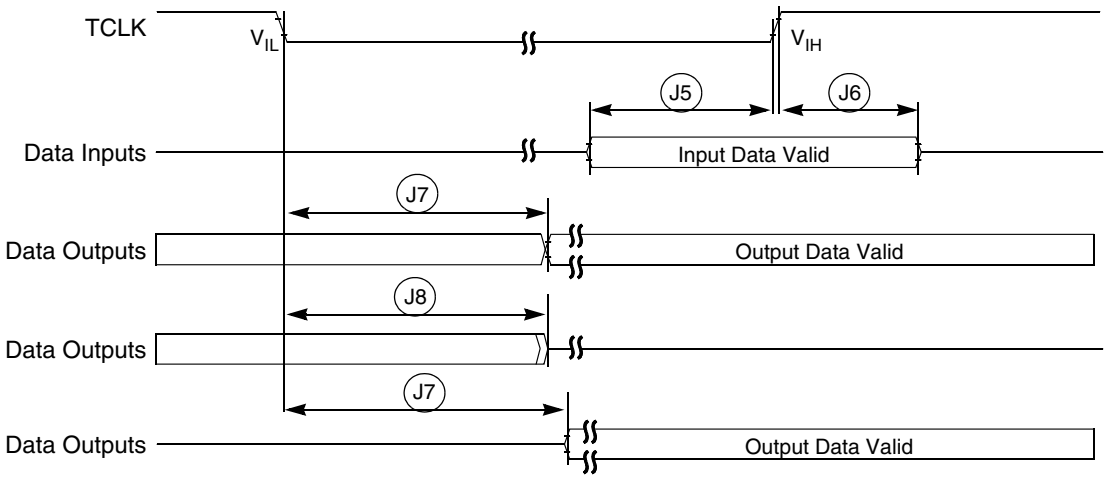


Figure 17. Boundary Scan (JTAG) Timing

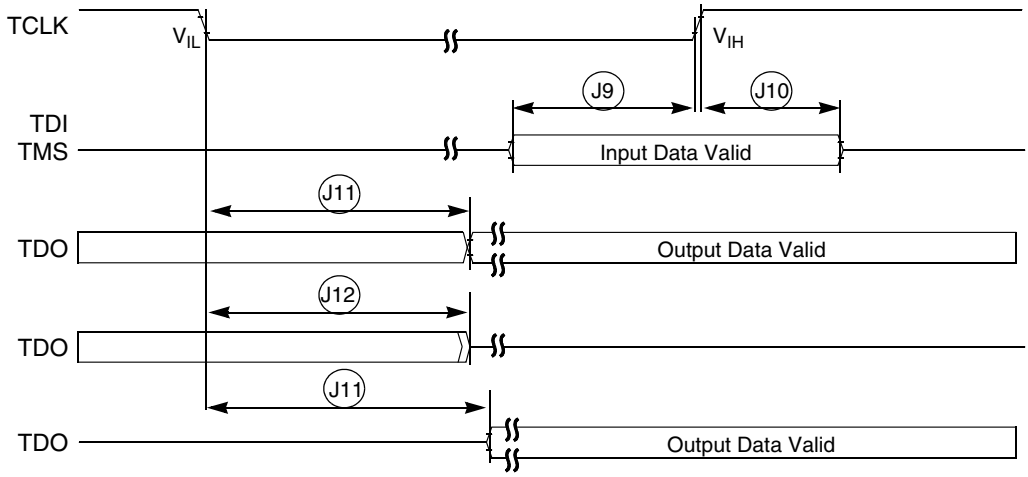


Figure 18. Test Access Port Timing

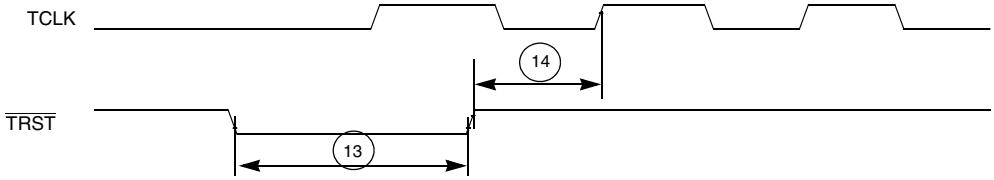


Figure 19. $\overline{TRST}$ Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

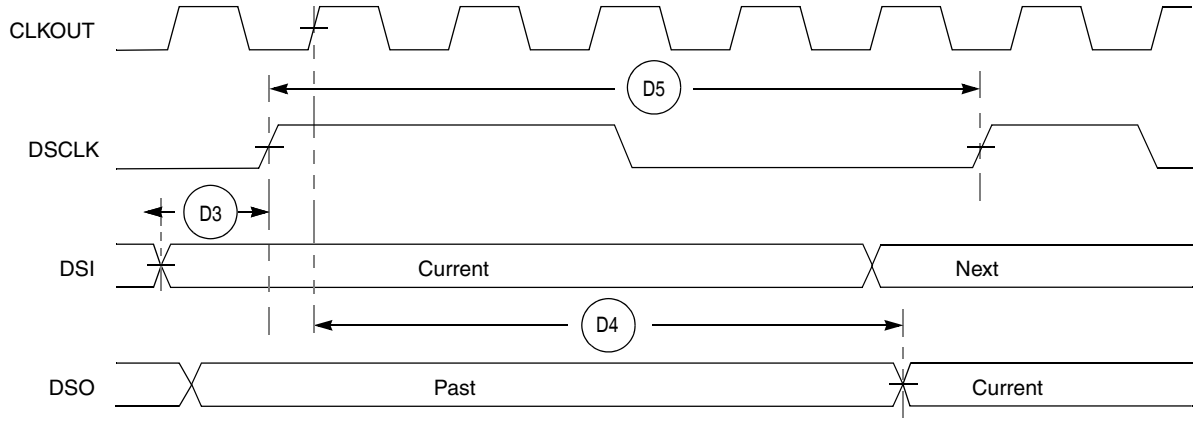


Figure 21. BDM Serial Port AC Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W 98ASH70694A
MCF52258		
MCF52259		

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	• Added package dimensions to package diagrams • Added listing of devices for MCF52259 family • Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation” • Updated the figure **Pinout Top View (144 MAPBGA)** • Removed an extraneous instance of the table **Pin Functions by Primary and Alternate Purpose** • In the table **Pin Functions by Primary and Alternate Purpose**, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL” • In the table **SGFM Flash Program and Erase Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **SGFM Flash Module Life Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **Oscillator and PLL Specifications**, changed “V_{DD} and V_{DDPLL} = 2.7 to 3.6 V“ to “V_{DD} and V_{DDPLL} = 3.0 to 3.6 V“ • In the table **Reset and Configuration Override Timing**, changed “V_{DD} = 2.7 to 3.6 V“ to “V_{DD} = 3.0 to 3.6 V“
2	• Added EzPort Electrical Specifications. • Updated Table 2 for part numbers. • In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values,JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. • Updated Table 14. • Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). • Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	• Updated EzPort Electrical Specifications • Added hysteresis note in the DC electrical table • Clarified pin function table for VSS pins. • Clarified orderable part summary.
4	• Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, “This value has been update” • Updated crystal frequency value to 25 MHz
5	• Updated TOC

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