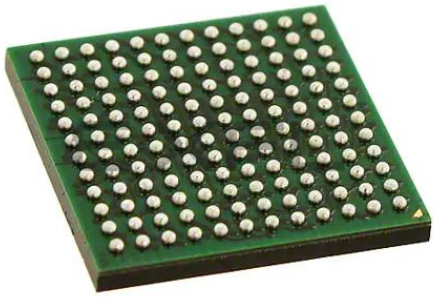

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 66MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, QSPI, UART/USART, USB OTG |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 96 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-MAPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52258cvn66j |

# 1 Family Configurations

**Table 1. MCF52259 Family Configurations**

| Module | 52252 | 52254 | 52255 | 52256 | 52258 | 52259 |
|---|---|---|---|---|---|---|
| Version 2 ColdFire Core with eMAC (Enhanced multiply-accumulate unit) and CAU (Cryptographic acceleration unit) | • | • | • | • | • | • |
| System Clock | up to 66 or 80 MHz[1] | | up to 80 MHz[1] | up to 66 or 80 MHz[1] | | up to 80 MHz[1] |
| Performance (Dhrystone 2.1 MIPS) | up to 63 or 76 | | | | | |
| Flash | 256 KB | 512 KB | 512 KB | 256 KB | 512 KB | 512 KB |
| Static RAM (SRAM) | 32 KB | 64 KB | 64 KB | 32 / 64 KB | 64 KB | 64 KB |
| Two Interrupt Controllers (INTC) | • | • | • | • | • | • |
| Fast Analog-to-Digital Converter (ADC) | • | • | • | • | • | • |
| USB On-The-Go (USB OTG) | • | • | • | • | • | • |
| Mini-FlexBus external bus interface | — | — | — | • | • | • |
| Fast Ethernet Controller (FEC) | • | • | • | • | • | • |
| Random Number Generator and Cryptographic Acceleration Unit (CAU) | — | — | • | — | — | • |
| FlexCAN 2.0B Module | Varies | Varies | • | Varies | Varies | • |
| Four-channel Direct-Memory Access (DMA) | • | • | • | • | • | • |
| Software Watchdog Timer (WDT) | • | • | • | • | • | • |
| Secondary Watchdog Timer | • | • | • | • | • | • |
| Two-channel Periodic Interrupt Timer (PIT) | 2 | 2 | 2 | 2 | 2 | 2 |
| Four-Channel General Purpose Timer (GPT) | • | • | • | • | • | • |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 | 4 | 4 |
| QSPI | • | • | • | • | • | • |
| UART(s) | 3 | 3 | 3 | 3 | 3 | 3 |
| I2C | 2 | 2 | 2 | 2 | 2 | 2 |
| Eight/Four-channel 8/16-bit PWM Timer | • | • | • | • | • | • |
| General Purpose I/O Module (GPIO) | • | • | • | • | • | • |
| Chip Configuration and Reset Controller Module | • | • | • | • | • | • |
| Background Debug Mode (BDM) | • | • | • | • | • | • |
| JTAG - IEEE 1149.1 Test Access Port | • | • | • | • | • | • |
| Package | 100 LQFP | | | 144 LQFP or 144 MAPBGA | | |

[1] 66 MHz = 63 MIPS; 80 MHz = 76 MIPS

## 1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

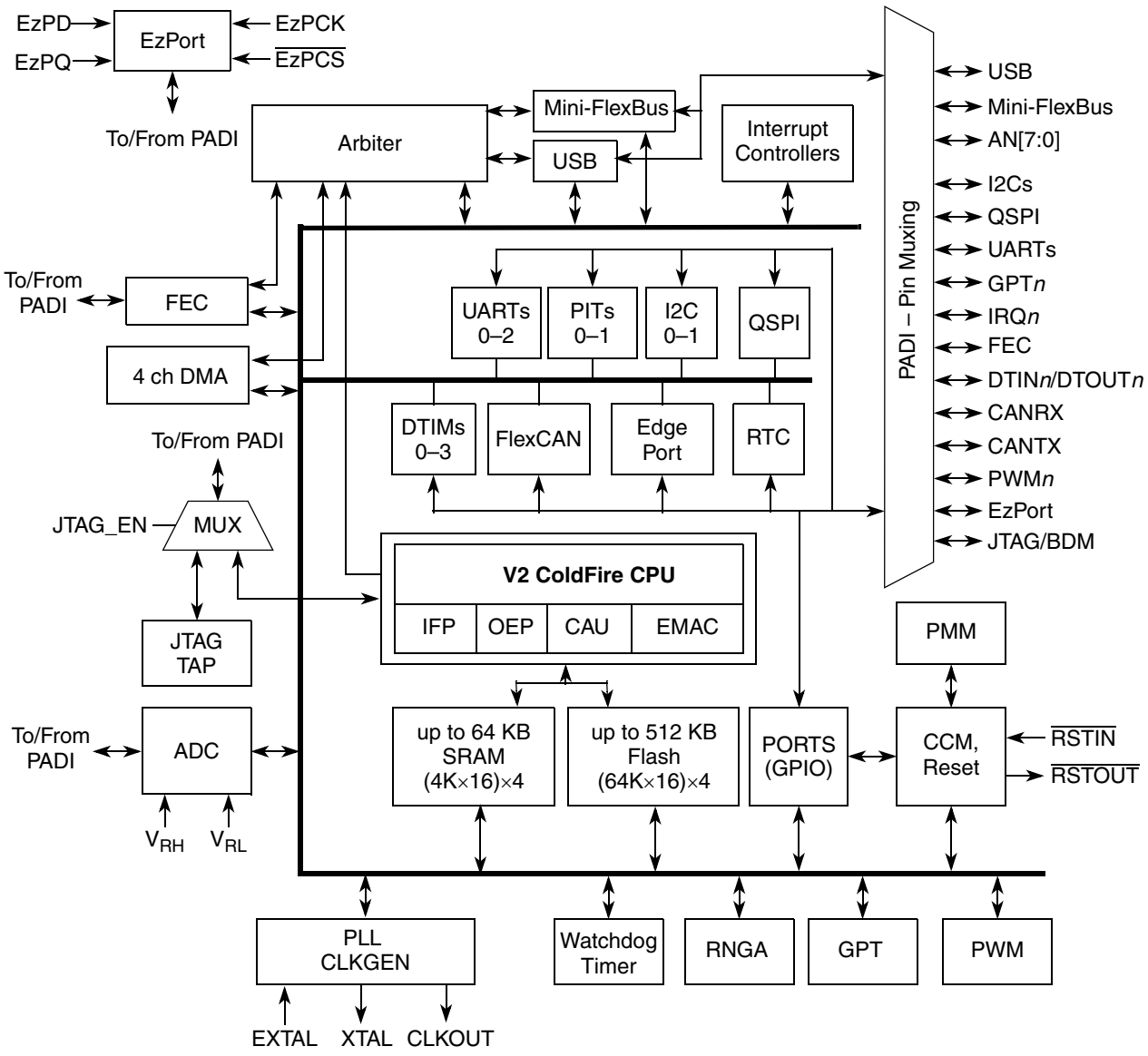



**Figure 1. MCF52259 Block Diagram**

## 1.2 Features

### 1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip

  - Up to 80 MHz processor core frequency
  - 40 MHz or 33 MHz peripheral bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support 16×16 → 32 or 32×32 → 48 operations
  - Cryptographic Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
  - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/s
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points

  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - $2^n$ ($0 \le n \le 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O on 100-pin package
  - Up to 96 bits of general purpose I/O on 144-pin package
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

## 1.2.16 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN*n* signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR*n*). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

## 1.2.17 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

## 1.2.18 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

## 1.2.19 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

## 1.2.20 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The timer supports PCM mode, which results in superior signal quality when compared to that of a conventional PWM. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For

Figure 2 shows the pinout configuration for the 144 LQFP.

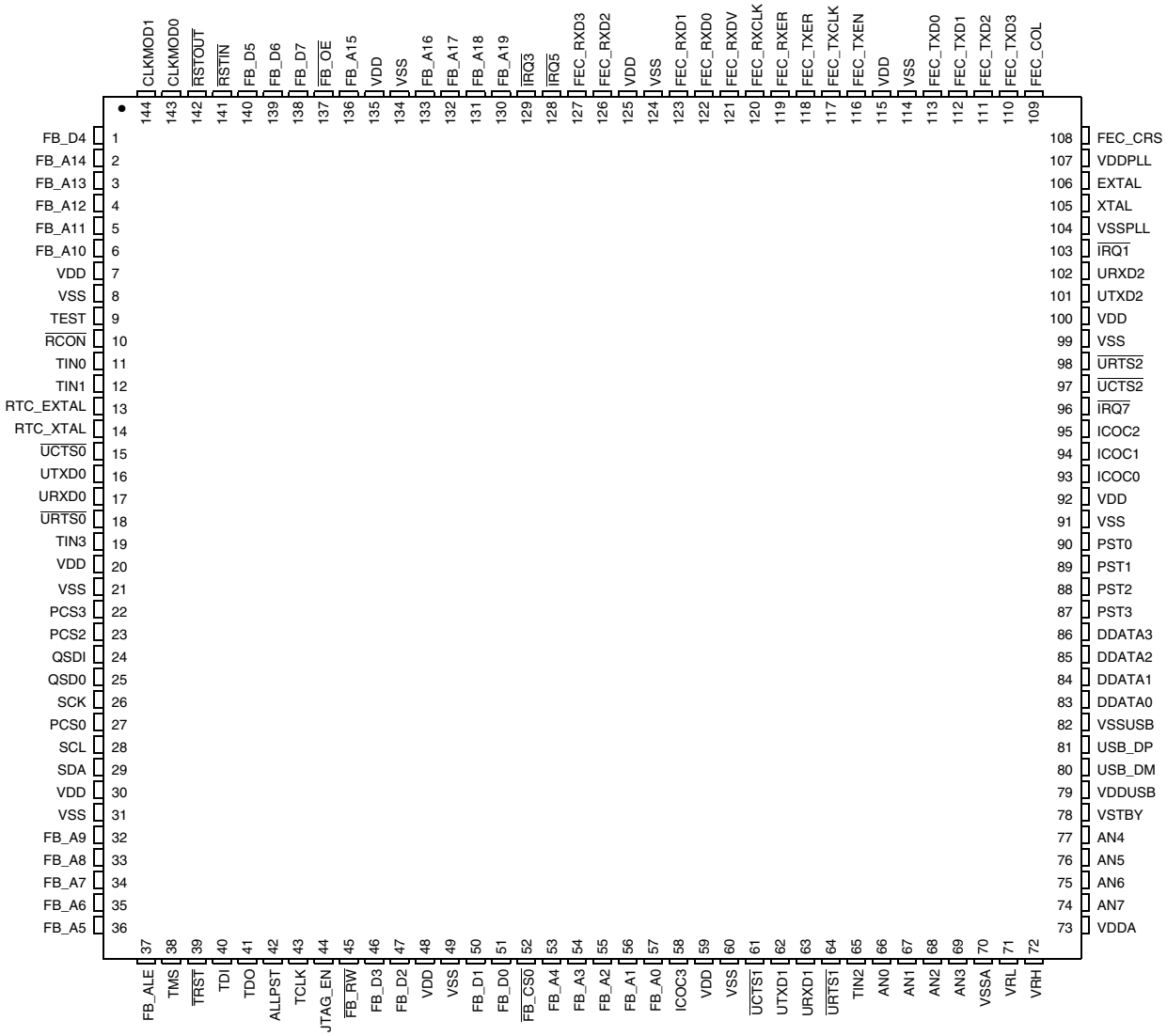



**Figure 2. 144 LQFP Pin Assignment**

Figure 4 shows the pinout configuration for the 144 MAPBGA.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | RSTOUT | RSTIN | FB_D6 | FB_D7 | IRQ3 | IRQ5 | FEC_ RXD0 | FEC_ RXER | FEC_ TXEN | FEC_ TXD3 | VSS | A |
| B | TEST | FB_A14 | FB_D4 | FB_D5 | FB_OE | FB_A19 | FEC_ RXD1 | FEC_ RXCLK | FEC_ TXCLK | FEC_ TXD2 | FEC_COL | FEC_CRS | B |
| C | TIN1 | FB_A12 | FB_A13 | FB_A15 | FB_A16 | FB_A18 | FEC_ RXD2 | FEC_ RXDV | FEC_ TXD1 | URXD2 | VDDPLL | EXTAL | C |
| D | RTC_ EXTAL | TIN0 | FB_A11 | CLKMOD1 | CLKMOD0 | FB_A17 | FEC_ RXD3 | FEC_ TXER | FEC_ TXD0 | UTXD2 | VSSPLL | XTAL | D |
| E | RTC_ XTAL | UCTS0 | FB_A10 | RCON | VDD | VDD | VDD | VDD | IRQ1 | URTS2 | UCTS2 | IRQ7 | E |
| F | UTXD0 | URXD0 | URTS0 | TIN3 | VDD | VSS | VSS | VSS | PST3 | DDATA0 | DDATA1 | ICOC0 | F |
| G | QSDO | QSDI | PCS2 | PCS3 | VDD | VSS | VSS | VSS | DDATA3 | PST2 | PST1 | PST0 | G |
| H | SCL | SDA | SCK | PCS0 | VDD | VDD | VDD | VSS | VSSUSB | DDATA2 | USB_DM | USB_DP | H |
| J | FB_A6 | FB_A7 | FB_A9 | FB_A8 | FB_D0 | FB_A3 | VDD | TIN2 | VDDUSB | ICOC2 | ICOC1 | VSTBY | J |
| K | TMS | TRST | FB_ALE | FB_A5 | FB_D2 | FB_A4 | UCTS1 | UTXD1 | AN3 | AN6 | AN4 | AN5 | K |
| L | TDI | TDO | ALLPST | FB_D3 | FB_D1 | FB_A1 | FB_A0 | URXD1 | AN2 | VRH | VDDA | AN7 | L |
| M | VSS | JTAG_ EN | TCLK | FB_RW | FB_CS0 | FB_A2 | ICOC3 | URTS1 | AN0 | AN1 | VRL | VSSA | M |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |

**Figure 4. Pinout Top View (144 MAPBGA)**

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | Secondary Function (Alt 1) | Tertiary Function (Alt 2) | Quaternary Function (GPIO) | Slew Rate | Drive Strength/Control[1] | Pull-up/ Pull-down[2] | Pin on 144 MAPBGA | Pin on 144 LQFP | Pin on 100 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| Timer 1, 32-bit | DTIN1 | DTOUT1 | PWM2 | PTC1 | PSRR[17] | PDSR[17] | — | C1 | 12 | 6 |
| Timer 0, 32-bit | DTIN0 | DTOUT0 | PWM0 | PTC0 | PSRR[16] | PDSR[16] | — | D2 | 11 | 5 |
| UART 0 | UCTS0 | — | USB_VBUSE | PUA3 | PSRR[11] | PDSR[11] | — | E2 | 15 | 9 |
| | URTS0 | — | USB_VBUSD | PUA2 | PSRR[10] | PDSR[10] | — | F3 | 18 | 12 |
| | URXD0 | — | — | PUA1 | PSRR[9] | PDSR[9] | — | F2 | 17 | 11 |
| | UTXD0 | — | — | PUA0 | PSRR[8] | PDSR[8] | — | F1 | 16 | 10 |
| UART 1 | UCTS1 | SYNCA | URXD2 | PUB3 | PSRR[15] | PDSR[15] | — | K7 | 61 | 38 |
| | URTS1 | SYNCB | UTXD2 | PUB2 | PSRR[14] | PDSR[14] | — | M8 | 64 | 41 |
| | URXD1 | I2C_SDA1 | — | PUB1 | PSRR[13] | PDSR[13] | Pull-Up[6] | L8 | 63 | 40 |
| | UTXD1 | I2C_SCL1 | — | PUB0 | PSRR[12] | PDSR[12] | Pull-Up[6] | K8 | 62 | 39 |
| UART 2 | UCTS2 | I2C_SCL1 | USB_VBUSCHG | PUC3 | PSRR[27] | PDSR[27] | Pull-Up[6] | E11 | 97 | 64 |
| | URTS2 | I2C_SDA1 | USB_VBUSDIS | PUC2 | PSRR[26] | PDSR[26] | Pull-Up[6] | E10 | 98 | 65 |
| | URXD2 | CANRX | — | PUC1 | PSRR[25] | PDSR[25] | — | C10 | 102 | 69 |
| | UTXD2 | CANTX | — | PUC0 | PSRR[24] | PDSR[24] | — | D10 | 101 | 68 |
| USB OTG | USB_DM | — | — | — | N/A | N/A | — | H11 | 80 | 57 |
| | USB_DP | — | — | — | N/A | N/A | — | H12 | 81 | 58 |
| | USB_VDD | — | — | — | N/A | N/A | — | J9 | 79 | 56 |
| | USB_VSS | — | — | — | N/A | N/A | — | H9 | 82 | 59 |

**Table 3. Pin Functions by Primary and Alternate Purpose (continued)**

| Pin Group | Primary Function | Secondary Function (Alt 1) | Tertiary Function (Alt 2) | Quaternary Function (GPIO) | Slew Rate | Drive Strength/Control[1] | Pull-up/ Pull-down[2] | Pin on 144 MAPBGA | Pin on 144 LQFP | Pin on 100 LQFP |
|---|---|---|---|---|---|---|---|---|---|---|
| Mini-FlexBus[9] | FB_ALE | $\overline{\text{FB\_CS1}}$ | — | PAS2 | PSRRL[20] | PDSRL[20] | — | K3 | 37 | — |
| | FB_AD[7:0] | — | — | PTE[7:0] | PSRRL[7:0] | PDSRL[7:0] | — | J2, J1, K4, K6, J6, M6, L6, L7 | 34–36; 53–57 | — |
| | FB_AD[15:8] | — | — | PTF[7:0] | PSRRL[15:8] | PDSRL[15:8] | — | C4, B2, C3, C2, D3, E3, J3, J4 | 136, 2–6, 32–33 | — |
| | FB_AD[19:16] | — | — | PTG[3:0] | PSRRL[19:16] | PDSRL[19:16] | — | B6, C6, D6, C5 | 130–133 | — |
| | $\overline{\text{FB\_CS0}}$ | — | — | PTG5 | PSRRL[21] | PDSRL[21] | — | M5 | 52 | — |
| | FB_R/$\overline{\text{W}}$ | — | — | PTG7 | PSRRL[31] | PDSRL[31] | — | M4 | 45 | — |
| | $\overline{\text{FB\_OE}}$ | — | — | PTG6 | PSRRL[30] | PDSRL[30] | — | B5 | 137 | — |
| | FB_D7 | CANRX | — | PTH5 | PSRRL[29] | PDSRL[29] | — | A5 | 138 | — |
| | FB_D6 | CANTX | — | PTH4 | PSRRL[28] | PDSRL[28] | — | A4 | 139 | — |
| | FB_D5 | I2C_SCL1 | — | PTH3 | PSRRL[27] | PDSRL[27] | Pull-Up[6] | B4 | 140 | — |
| | FB_D4 | I2C_SDA1 | — | PTH2 | PSRRL[26] | PDSRL[26] | Pull-Up[6] | B3 | 1 | — |
| | FB_D3 | USB_ VBUSD | — | PTH1 | PSRRL[25] | PDSRL[25] | — | L4 | 46 | — |
| | FB_D2 | USB_ VBUSE | — | PTH0 | PSRRL[24] | PDSRL[24] | — | K5 | 47 | — |
| | FB_D1 | SYNCA | — | PTH7 | PSRRL[23] | PDSRL[23] | — | L5 | 50 | — |
| | FB_D0 | SYNCB | — | PTH6 | PSRRL[22] | PDSRL[22] | — | J5 | 51 | — |
| Standby Voltage | VSTBY | — | — | — | N/A | N/A | — | J12 | 78 | 55 |
| VDD[10] | VDD | — | — | — | N/A | N/A | — | E5–E8; F5; G5; H5–7; J7 | 7; 20; 30; 48; 59; 92; 100; 115; 125; 135 | 1; 14; 24; 33; 36; 67; 82; 92 |

**Table 8. Thermal Characteristics (continued)**

| | Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| 100 LQFP | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 53[13,14] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 39[1,15] | °C/W |
| | Junction to ambient, (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 42[1,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 33[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 25[16] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 9[17] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[18] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |

1 $\theta_{JA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

7 $\theta_{JA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

8 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

9 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

10 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

11 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

12 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

13 $\theta_{JA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

14 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

15 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

[2] Reprogramming of a flash memory array block prior to erase is not required.

## 2.5 EzPort Electrical Specifications

**Table 11. EzPort Electrical Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| EP1 | EPCK frequency of operation (all commands except READ) | — | $f_{sys}$ / 2 | MHz |
| EP1a | EPCK frequency of operation (READ command) | — | $f_{sys}$ / 8 | MHz |
| EP2 | EPCS_b negation to next EPCS_b assertion | 2 × $T_{cyc}$ | — | ns |
| EP3 | EPCS_B input valid to EPCK high (setup) | 5 | — | ns |
| EP4 | EPCK high to EPCS_B input invalid (hold) | 5 | — | ns |
| EP5 | EPD input valid to EPCK high (setup) | 2 | — | ns |
| EP6 | EPCK high to EPD input invalid (hold) | 5 | — | ns |
| EP7 | EPCK low to EPQ output valid (out setup) | — | 12 | ns |
| EP8 | EPCK low to EPQ output invalid (out hold) | 0 | — | ns |
| EP9 | EPCS_B negation to EPQ tri-state | — | 12 | ns |

## 2.6 ESD Protection

**Table 12. ESD Protection Characteristics[1, 2]**

| Characteristics | Symbol | Value | Units |
|---|---|---|---|
| ESD target for Human Body Model | HBM | 2000 | V |
| ESD target for Machine Model | MM | 200 | V |
| HBM circuit description | $R_{series}$ | 1500 | Ω |
| | C | 100 | pF |
| MM circuit description | $R_{series}$ | 0 | Ω |
| | C | 200 | pF |
| Number of pulses per pin (HBM)<br>• Positive pulses<br>• Negative pulses | <br>—<br>— | <br>1<br>1 | — |
| Number of pulses per pin (MM)<br>• Positive pulses<br>• Negative pulses | <br>—<br>— | <br>3<br>3 | — |
| Interval of pulses | — | 1 | sec |

[1] All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 2.7 DC Electrical Specifications

**Table 13. DC Electrical Specifications [1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.6 | V |
| Standby voltage | $V_{STBY}$ | 1.8 | 3.5 | V |
| Input high voltage | $V_{IH}$ | $0.7 \times V_{DD}$ | 4.0 | V |
| Input low voltage | $V_{IL}$ | $V_{SS} - 0.3$ | $0.35 \times V_{DD}$ | V |
| Input hysteresis[2] | $V_{HYS}$ | $0.06 \times V_{DD}$ | — | mV |
| Low-voltage detect trip voltage ($V_{DD}$ falling) | $V_{LVD}$ | 2.15 | 2.3 | V |
| Low-voltage detect hysteresis ($V_{DD}$ rising) | $V_{LVDHYS}$ | 60 | 120 | mV |
| Input leakage current<br>$V_{in} = V_{DD}$ or $V_{SS}$, digital pins | $I_{in}$ | –1.0 | 1.0 | μA |
| Output high voltage (all input/output and all output pins)<br>$I_{OH}$ = –2.0 mA | $V_{OH}$ | $V_{DD} - 0.5$ | — | V |
| Output low voltage (all input/output and all output pins)<br>$I_{OL}$ = 2.0 mA | $V_{OL}$ | — | 0.5 | V |
| Output high voltage (high drive)<br>$I_{OH}$ = -5 mA | $V_{OH}$ | $V_{DD} - 0.5$ | — | V |
| Output low voltage (high drive)<br>$I_{OL}$ = 5 mA | $V_{OL}$ | — | 0.5 | V |
| Output high voltage (low drive)<br>$I_{OH}$ = -2 mA | $V_{OH}$ | $V_{DD}$ - 0.5 | — | V |
| Output low voltage (low drive)<br>$I_{OL}$ = 2 mA | $V_{OL}$ | — | 0.5 | V |
| Weak internal pull Up device current, tested at $V_{IL}$ Max.[3] | $I_{APU}$ | –10 | –130 | μA |
| Input Capacitance [4]<br>• All input-only pins<br>• All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

1 Refer to Table 14 for additional PLL specifications.

2 Only for pins: IRQ1, IRQ3. IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

3 Refer to Table 3 for pins having internal pull-up devices.

4 This parameter is characterized before qualification rather than 100% tested.

## 2.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

**Table 17. Receive Signal Timing**

| Num | Characteristic | MII Mode | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| — | RXCLK frequency | — | 25 | MHz |
| E1 | RXD[n:0], RXDV, RXER to RXCLK setup[1] | 5 | — | ns |
| E2 | RXCLK to RXD[n:0], RXDV, RXER hold[1] | 5 | — | ns |
| E3 | RXCLK pulse width high | 35% | 65% | RXCLK period |
| E4 | RXCLK pulse width low | 35% | 65% | RXCLK period |

[1] In MII mode, n = 3

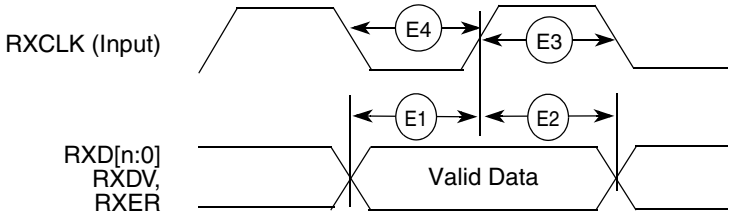



**Figure 7. MII Receive Signal Timing Diagram**

## 2.11.2 Transmit Signal Timing Specifications

**Table 18. Transmit Signal Timing**

| Num | Characteristic | MII Mode | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| — | TXCLK frequency | — | 25 | MHz |
| E5 | TXCLK to TXD[n:0], TXEN, TXER invalid[1] | 5 | — | ns |
| E6 | TXCLK to TXD[n:0], TXEN, TXER valid[1] | — | 25 | ns |
| E7 | TXCLK pulse width high | 35% | 65% | $t_{TXCLK}$ |
| E8 | TXCLK pulse width low | 35% | 65% | $t_{TXCLK}$ |

[1] In MII mode, n = 3

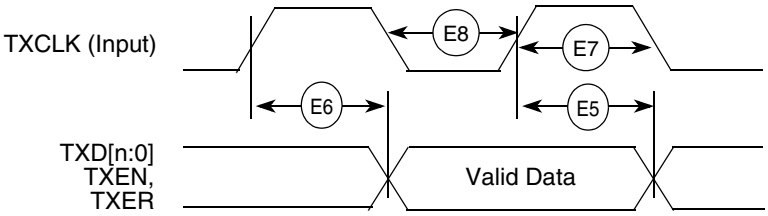



**Figure 8. MII Transmit Signal Timing Diagram**

## 2.11.3 Asynchronous Input Signal Timing Specifications

**Table 19. MII Transmit Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| E9 | CRS, COL minimum pulse width | 1.5 | — | TXCLK period |

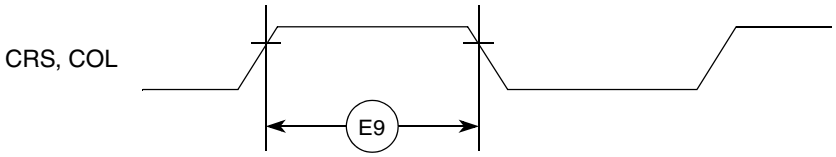



**Figure 9. MII Async Inputs Timing Diagram**

## 2.11.4 MII Serial Management Timing Specifications

**Table 20. MII Serial Management Channel Signal Timing**

| Num | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| E10 | MDC cycle time | $t_{MDC}$ | 400 | — | ns |
| E11 | MDC pulse width | | 40 | 60 | % $t_{MDC}$ |
| E12 | MDC to MDIO output valid | | — | 375 | ns |
| E13 | MDC to MDIO output invalid | | 25 | — | ns |
| E14 | MDIO input to MDC setup | | 10 | — | ns |
| E15 | MDIO input to MDC hold | | 0 | — | ns |

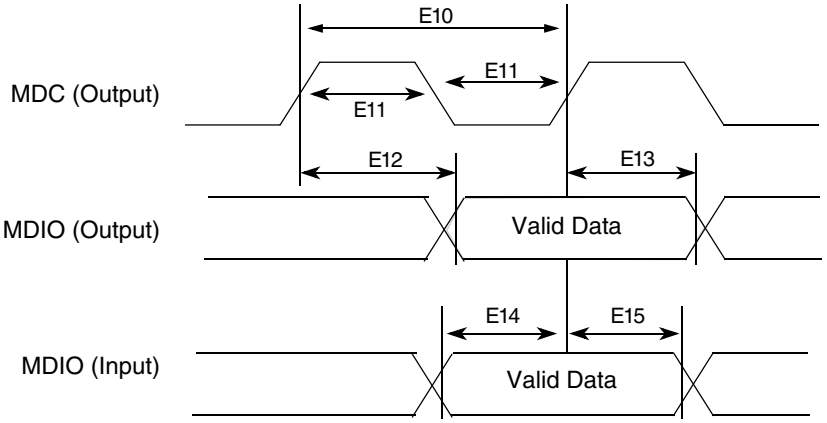



**Figure 10. MII Serial Management Channel TIming Diagram**

## 2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 21 and Figure 11.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

## 2.14 I2C Input/Output Timing Specifications

Table 23 lists specifications for the I2C input timing parameters shown in Figure 13.

**Table 23. I2C Input Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1 | Start condition hold time | $2 \times t_{CYC}$ | — | ns |
| I2 | Clock low period | $8 \times t_{CYC}$ | — | ns |
| I3 | SCL/SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | SCL/SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | $4 \times t_{CYC}$ | — | ns |
| I7 | Data setup time | 0 | — | ns |
| I8 | Start condition setup time (for repeated start condition only) | $2 \times t_{CYC}$ | — | ns |
| I9 | Stop condition setup time | $2 \times t_{CYC}$ | — | ns |

Table 24 lists specifications for the I2C output timing parameters shown in Figure 13.

**Table 24. I2C Output Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1[1] | Start condition hold time | $6 \times t_{CYC}$ | — | ns |
| I2[1] | Clock low period | $10 \times t_{CYC}$ | — | ns |
| I3[2] | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | — | µs |
| I4[1] | Data hold time | $7 \times t_{CYC}$ | — | ns |
| I5[3] | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 3 | ns |
| I6[1] | Clock high time | $10 \times t_{CYC}$ | — | ns |
| I7[1] | Data setup time | $2 \times t_{CYC}$ | — | ns |
| I8[1] | Start condition setup time (for repeated start condition only) | $20 \times t_{CYC}$ | — | ns |
| I9[1] | Stop condition setup time | $10 \times t_{CYC}$ | — | ns |

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The $I^2C$ interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50 pF load.

**Table 25. ADC Parameters[1] (continued)**

| Name | Characteristic | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | — | 62 to 66 | — | dB |
| THD | Total harmonic distortion | — | –75 | — | dB |
| SFDR | Spurious free dynamic range | — | 67 to 70.3 | — | dB |
| SINAD | Signal-to-noise plus distortion | — | 61 to 63.9 | — | dB |
| ENOB | Effective number of bits | 9.1 | 10.6 | — | Bits |

1 All measurements are preliminary pending full characterization, and made at $V_{DD}$ = 3.3 V, $V_{REFH}$ = 3.3 V, and $V_{REFL}$ = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

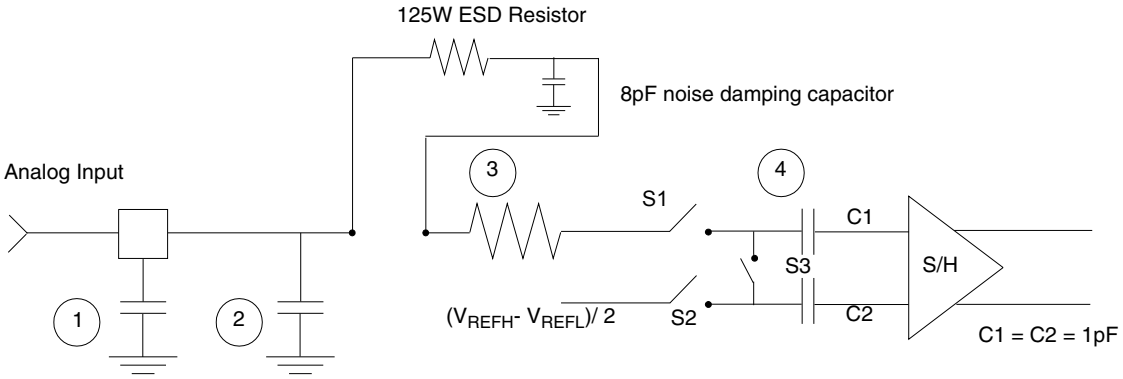
5 Includes power-up of ADC and $V_{REF}$

6 ADC clock cycles

7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

## 2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, $V_{REF}$ and the ADC clock frequency.




1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

**Figure 14. Equivalent Circuit for A/D Loading**

## 2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

**Table 26. Timer Module AC Timing Specifications**

| Name | Characteristic[1] | Min | Max | Unit |
|---|---|---|---|---|
| T1 | DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time | $3 \times t_{CYC}$ | — | ns |
| T2 | DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width | $1 \times t_{CYC}$ | — | ns |

1 All timing references to CLKOUT are given to its rising edge.

## 2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

**Table 27. QSPI Modules AC Timing Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| QS1 | QSPI_CS[3:0] to QSPI_CLK | 1 | 510 | $t_{CYC}$ |
| QS2 | QSPI_CLK high to QSPI_DOUT valid | — | 10 | ns |
| QS3 | QSPI_CLK high to QSPI_DOUT invalid (Output hold) | 2 | — | ns |
| QS4 | QSPI_DIN to QSPI_CLK (Input setup) | 9 | — | ns |
| QS5 | QSPI_DIN to QSPI_CLK (Input hold) | 9 | — | ns |

The values in Table 27 correspond to Figure 15.

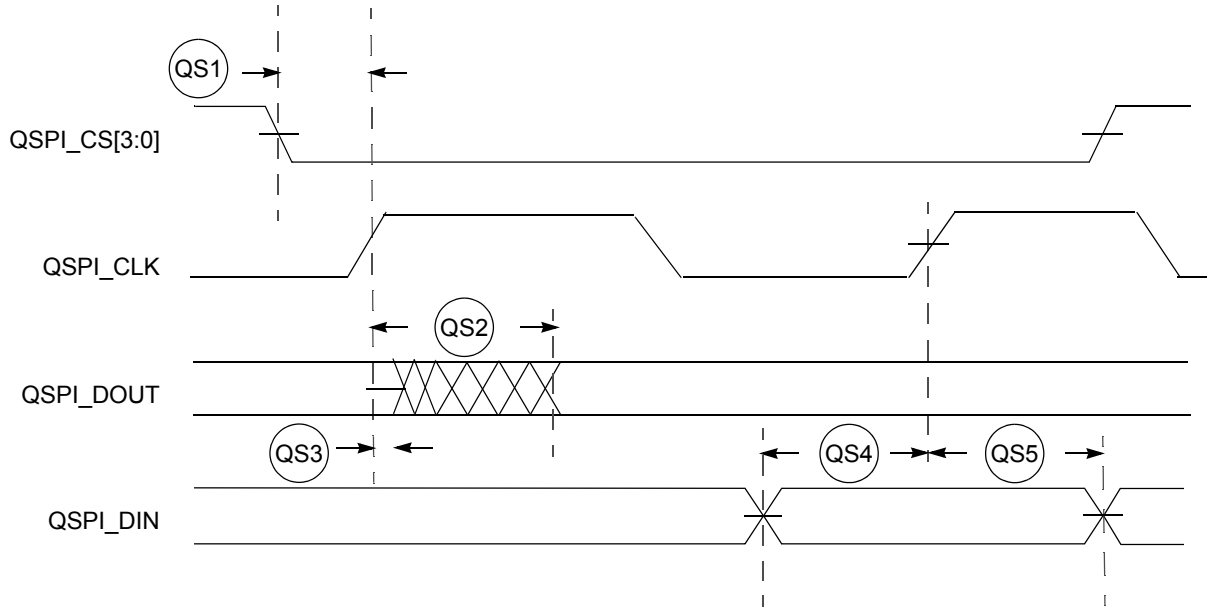



**Figure 15. QSPI Timing**

## 2.19 JTAG and Boundary Scan Timing

**Table 28. JTAG and Boundary Scan Timing**

| Num | Characteristics[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| J1 | TCLK frequency of operation | $f_{JCYC}$ | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK cycle period | $t_{JCYC}$ | $4 \times t_{CYC}$ | — | ns |
| J3 | TCLK clock pulse width | $t_{JCW}$ | 26 | — | ns |
| J4 | TCLK rise and fall times | $t_{JCRF}$ | 0 | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | $t_{BSDST}$ | 4 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | $t_{BSDHT}$ | 26 | — | ns |
| J7 | TCLK low to boundary scan output data valid | $t_{BSDV}$ | 0 | 33 | ns |
| J8 | TCLK low to boundary scan output high Z | $t_{BSDZ}$ | 0 | 33 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | $t_{TAPBST}$ | 4 | — | ns |
| J10 | TMS, TDI Input data hold time after TCLK rise | $t_{TAPBHT}$ | 10 | — | ns |
| J11 | TCLK low to TDO data valid | $t_{TDODV}$ | 0 | 26 | ns |
| J12 | TCLK low to TDO high Z | $t_{TDODZ}$ | 0 | 8 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | $t_{TRSTAT}$ | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | $t_{TRSTST}$ | 10 | — | ns |

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

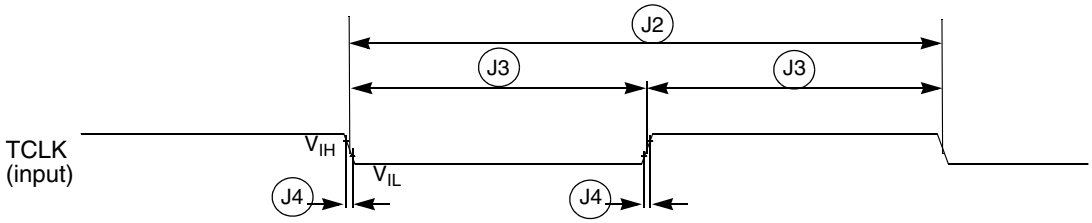



**Figure 16. Test Clock Input Timing**

Figure 21 shows BDM serial port AC timing for the values in Table 29.

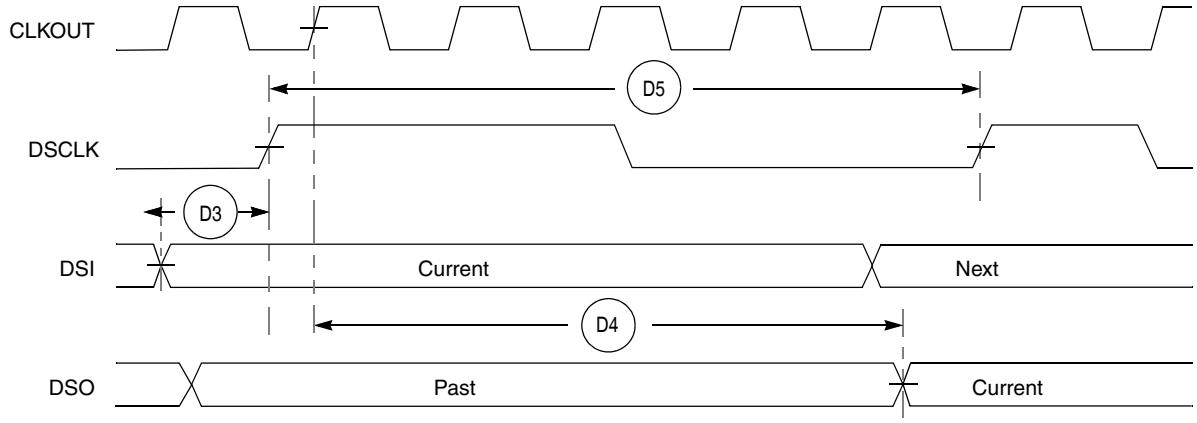



**Figure 21. BDM Serial Port AC Timing**

# 3 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

**Table 30. Package Information**

| Device | Package Type | Case Outline Numbers |
|---|---|---|
| MCF52252 | 100 LQFP | 98ASS23308W |
| MCF52254 | | |
| MCF52255 | | |
| MCF52256 | 144 LQFP or 144 MAPBGA | 98ASS23177W<br>98ASH70694A |
| MCF52258 | | |
| MCF52259 | | |

# 4 Revision History

**Table 31. Revision History**

| Revision | Description |
|---|---|
| 0 | Initial public release. |
| 1 | • Added package dimensions to package diagrams<br>• Added listing of devices for MCF52259 family<br>• Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation”<br>• Updated the figure **Pinout Top View (144 MAPBGA)**<br>• Removed an extraneous instance of the table **Pin Functions by Primary and Alternate Purpose**<br>• In the table **Pin Functions by Primary and Alternate Purpose**, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL”<br>• In the table **SGFM Flash Program and Erase Characteristics**, changed “($V_{DDF}$ = 2.7 to 3.6 V)“ to “($V_{DD}$ = 3.0 to 3.6 V)“<br>• In the table **SGFM Flash Module Life Characteristics**, changed “($V_{DDF}$ = 2.7 to 3.6 V)“ to “($V_{DD}$ = 3.0 to 3.6 V)“<br>• In the table **Oscillator and PLL Specifications**, changed “$V_{DD}$ and $V_{DDPLL}$ = 2.7 to 3.6 V“ to “$V_{DD}$ and $V_{DDPLL}$ = 3.0 to 3.6 V“<br>• In the table **Reset and Configuration Override Timing**, changed “$V_{DD}$ = 2.7 to 3.6 V“ to “$V_{DD}$ = 3.0 to 3.6 V“ |
| 2 | • Added EzPort Electrical Specifications.<br>• Updated Table 2 for part numbers.<br>• In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values,JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP.<br>• Updated Table 14.<br>• Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V).<br>• Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions. |
| 3 | • Updated EzPort Electrical Specifications<br>• Added hysteresis note in the DC electrical table<br>• Clarified pin function table for VSS pins.<br>• Clarified orderable part summary. |
| 4 | • Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, “This value has been update”<br>• Updated crystal frequency value to 25 MHz |
| 5 | • Updated TOC |