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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52258vn80

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1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 64 KB memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64 KB boundary within the 4 GB address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA, FEC, and USB. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 64 KB×16-bit flash memory arrays to generate 512 KB of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Cryptographic Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.24 Interrupt Controllers (INTC_n)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR_n[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

Family Configurations

Figure 2 shows the pinout configuration for the 144 LQFP.

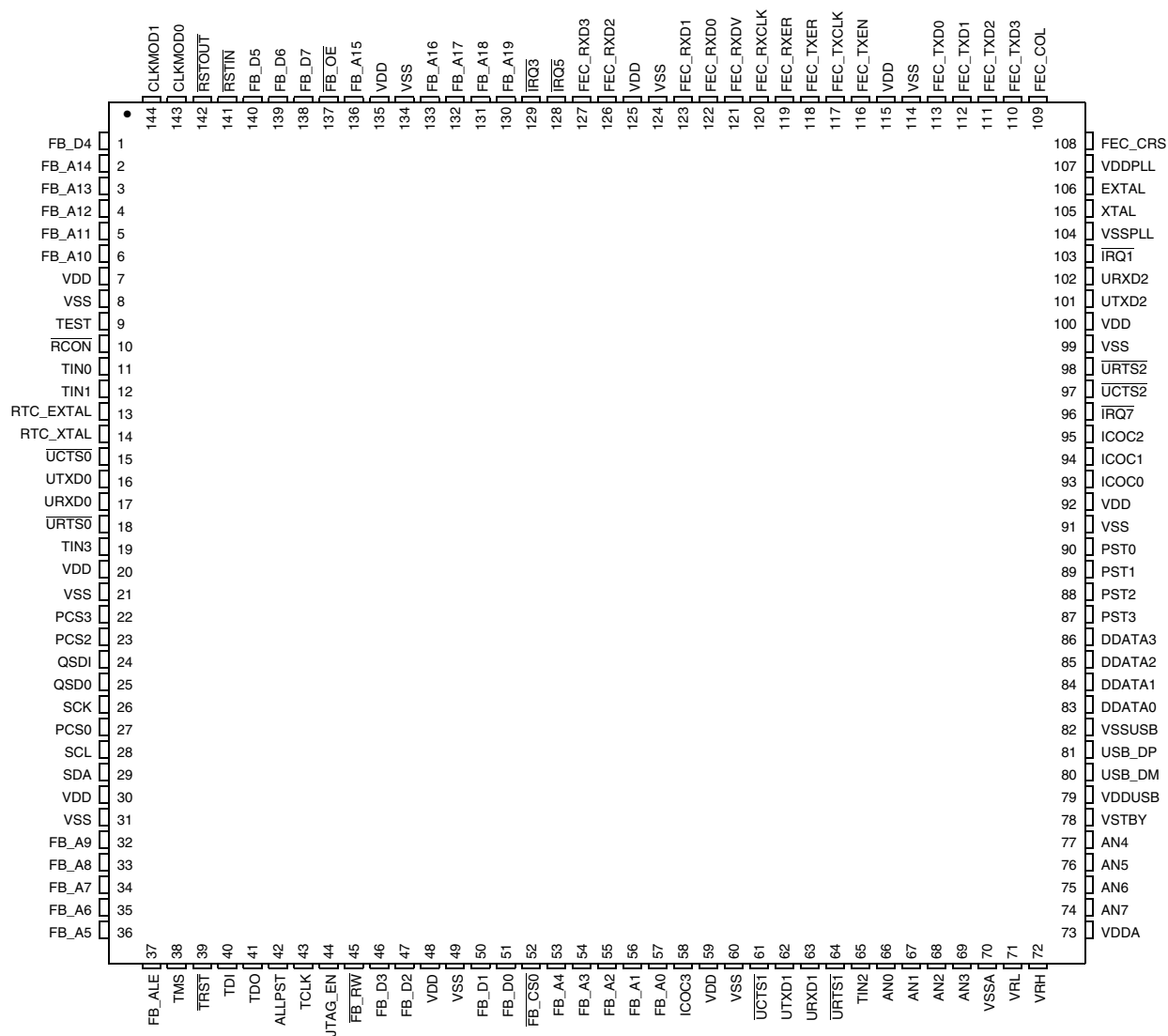


Figure 2. 144 LQFP Pin Assignment

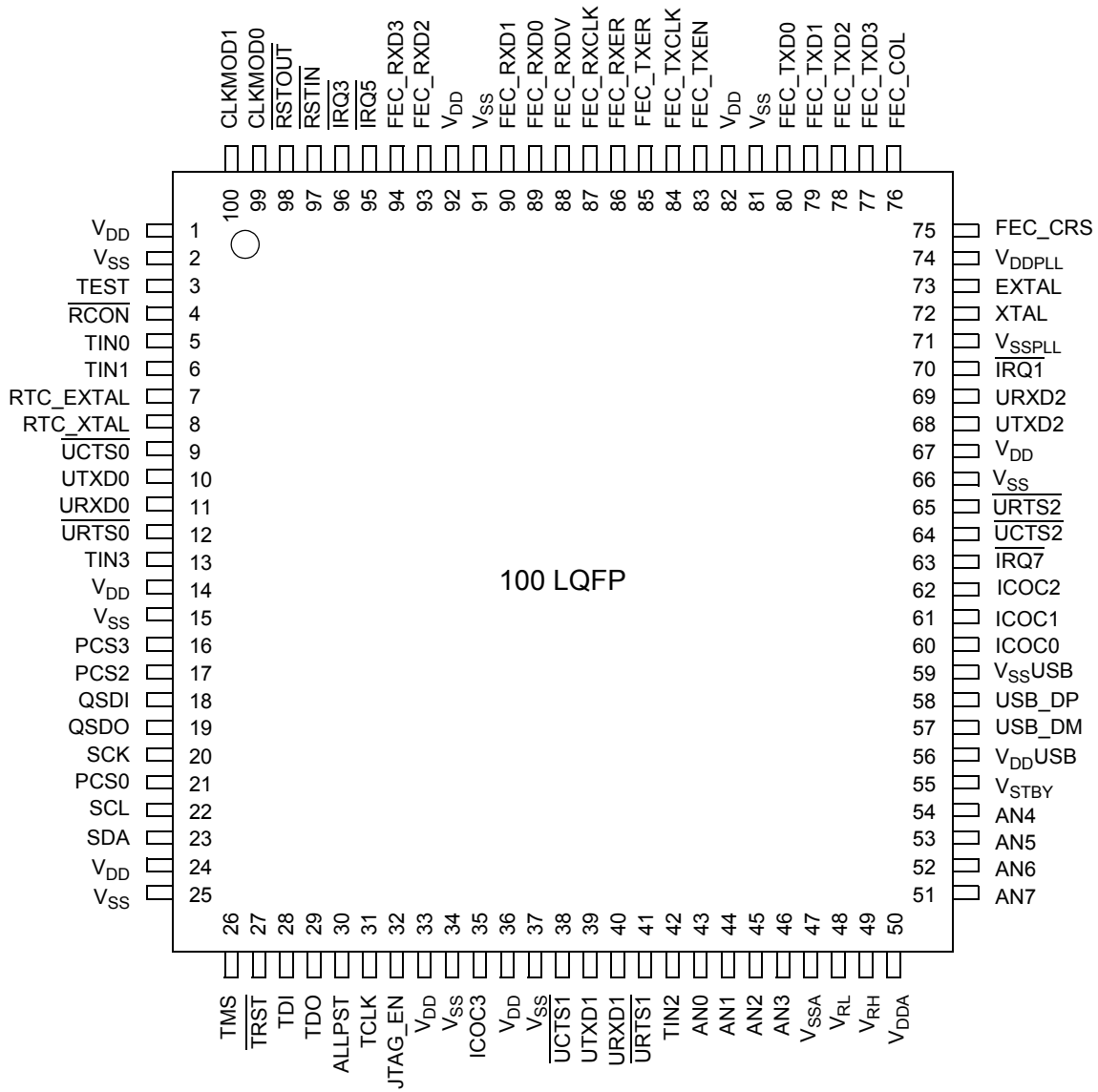


Figure 3. 100 LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 100 LQFP.

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_RXD0	FEC_RXER	FEC_TXEN	FEC_TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_RXD1	FEC_RXCLK	FEC_TXCLK	FEC_TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_RXD2	FEC_RXDV	FEC_TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_RXD3	FEC_TXER	FEC_TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/ Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0 ³	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up ⁴	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up ⁴	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up ⁴	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up ⁴	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up ⁴	A6	129	96
	IRQ1	—	USB_ALT CLK	PNQ1	Low	High	Pull-Up ⁴	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up ⁵	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up ⁵	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/BKPT	—	—	—	N/A	N/A	Pull-Up ⁵	K1	38	26
	TRST/DSCLK	—	—	—	N/A	N/A	Pull-Up ⁵	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control ¹	Pull-up/Pull-down ²	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
VSS	VSS	—	—	—	N/A	N/A	—	A1; A12; F6–8; G6–8; H8; M1	8; 21; 31; 49; 60; 91; 99; 114; 124; 134	2; 15; 25; 34; 37; 66; 81; 91

¹ The PDSR and PSSR registers are part of the GPIO module. All programmable signals default to 2mA drive in normal (single-chip) mode.

² All signals have a pull-up in GPIO mode.

³ I2C1 is multiplexed with specific pins of the QSPI, UART1, UART2, and Mini-FlexBus pin groups.

⁴ For primary and GPIO functions only.

⁵ Only when JTAG mode is enabled.

⁶ For secondary and GPIO functions only.

⁷ RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.

⁸ For GPIO functions, the Primary Function has pull-up control within the GPT module.

⁹ Available on 144-pin packages only.

¹⁰ This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	−0.3 to +4.0	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 or 0 to 70 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see orderable part number summary (Table 2)

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{13,14}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,15}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ¹⁶	°C/W
	Junction to case	—	θ_{JC}	9 ¹⁷	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹⁸	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

¹ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

³ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

⁴ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

⁷ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

⁸ Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

⁹ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

¹⁰ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

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- ¹⁷ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- ¹⁸ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

- T_A = ambient temperature, °C
 Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
 P_D = $P_{INT} + P_{I/O}$
 P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, W
 $P_{I/O}$ = power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in [Table 9](#) and [Table 10](#).

Table 9. SGFM Flash Program and Erase Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{\text{sys(R)}}$	0	—	66.67 or 80 ¹	MHz
System clock (program/erase) ²	$f_{\text{sys(P/E)}}$	0.15	—	66.67 or 80 ¹	MHz

¹ Depending on packaging; see the orderable part number summary ([Table 2](#)).

² Refer to the flash memory section for more information ([Section 2.4, “Flash Memory Characteristics”](#))

Table 10. SGFM Flash Module Life Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2.8 Clock Source Electrical Specifications

Table 14. Oscillator and PLL Specifications

(V_{DD} and V_{DDPLL} = 3.0 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	$f_{crystal}$ f_{ext}	12 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	f_{ref_pll}	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{ref} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	0.1	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4,9}	t_{lpll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK range	f_{UL}	−1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	−0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{sys} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary (Table 2).

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to rellock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

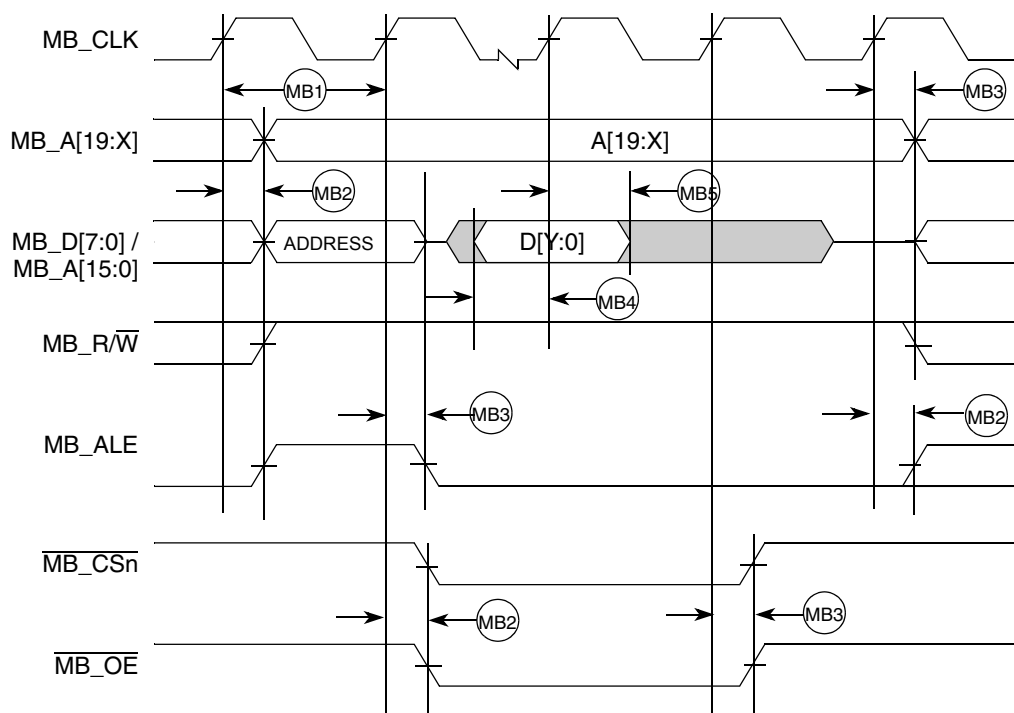


Figure 5. Mini-FlexBus Read Timing

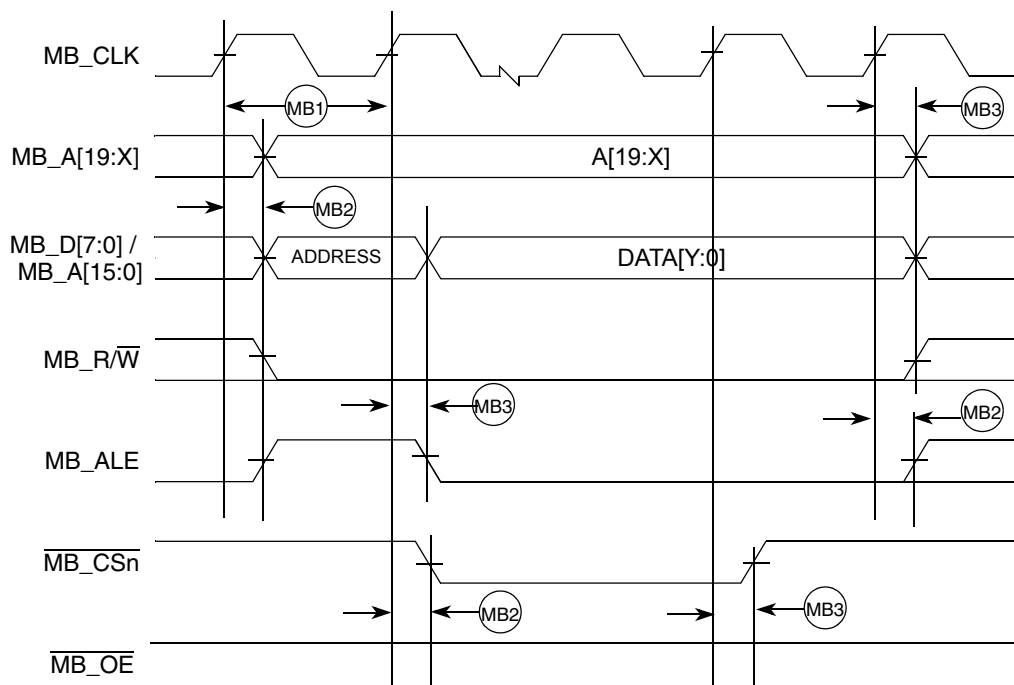


Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

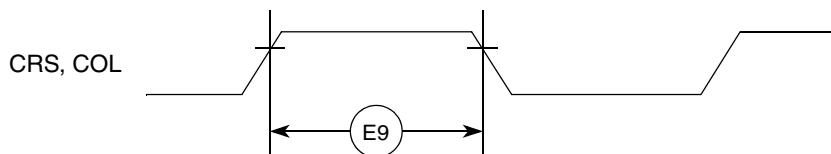


Figure 9. MII Async Inputs Timing Diagram

2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

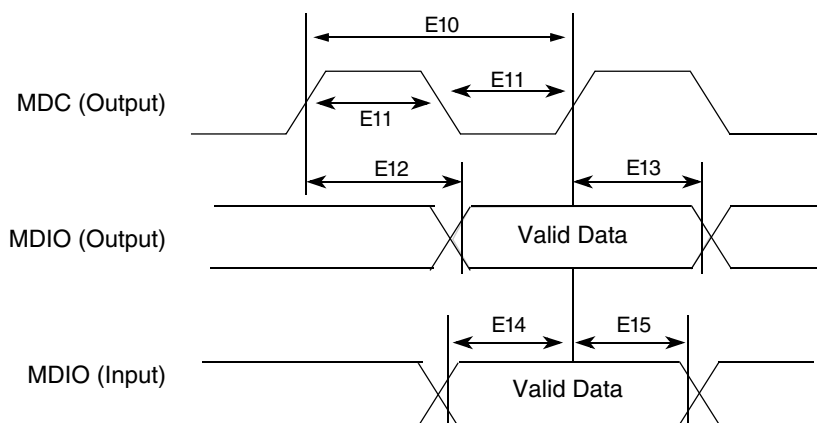


Figure 10. MII Serial Management Channel Timing Diagram

2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in [Table 21](#) and [Figure 11](#).

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

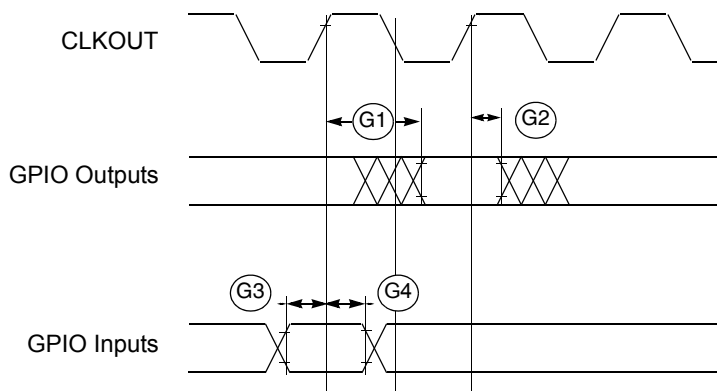


Figure 11. GPIO Timing

2.13 Reset Timing

Table 22. Reset and Configuration Override Timing

($V_{DD} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H)¹

NUM	Characteristic	Symbol	Min	Max	Unit
R1	\overline{RSTI} input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to \overline{RSTI} Input invalid	t_{CHRI}	1.5	—	ns
R3	\overline{RSTI} input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to \overline{RSTO} Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the \overline{RSTI} input are bypassed and \overline{RSTI} is asserted asynchronously to the system. Thus, \overline{RSTI} must be held a minimum of 100 ns.

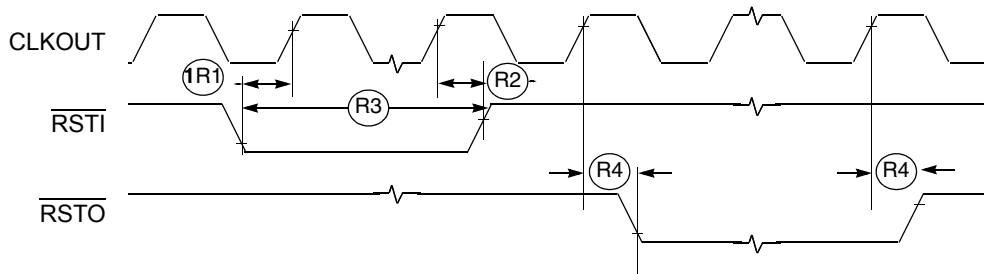
Figure 12. \overline{RSTI} and Configuration Override Timing

Figure 13 shows timing for the values in Table 23 and Table 24.

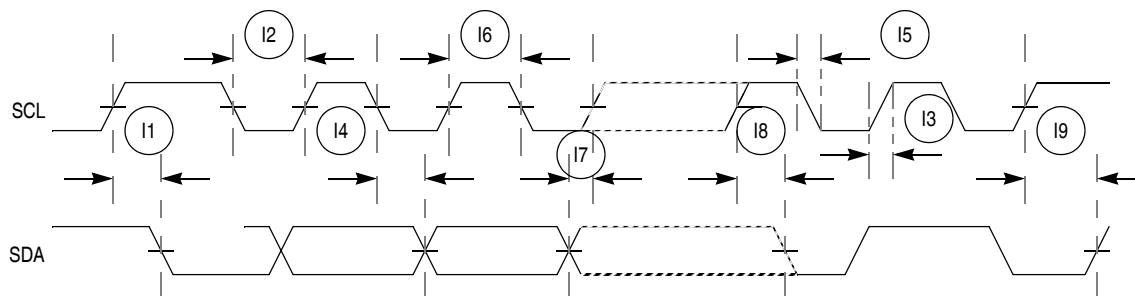


Figure 13. I2C Input/Output Timings

2.15 Analog-to-Digital Converter (ADC) Parameters

Table 25 lists specifications for the analog-to-digital converter.

Table 25. ADC Parameters¹

Name	Characteristic	Min	Typical	Max	Unit
V _{REFL}	Low reference voltage	V _{SSA}	—	V _{SSA} + 50 mV	V
V _{REFH}	High reference voltage	V _{DDA} - 50 mV	—	V _{DDA}	V
V _{DDA}	ADC analog supply voltage	3.1	3.3	3.6	V
V _{ADIN}	Input voltages	V _{REFL}	—	V _{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range) ²	—	±2.5	±3	LSB ³
INL	Integral non-linearity (10% to 90% input signal range) ⁴	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	-1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f _{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R _{AD}	Conversion range	V _{REFL}	—	V _{REFH}	V
t _{ADPU}	ADC power-up time ⁵	—	6	13	t _{AIC} cycles ⁶
t _{REC}	Recovery from auto standby	—	0	1	t _{AIC} cycles
t _{ADC}	Conversion time	—	6	—	t _{AIC} cycles
t _{ADS}	Sample time	—	1	—	t _{AIC} cycles
C _{ADI}	Input capacitance	—	See Figure 14	—	pF
X _{IN}	Input impedance	—	See Figure 14	—	W
I _{ADI}	Input injection current ⁷ , per pin	—	—	3	mA
I _{VREFH}	V _{REFH} current	—	0	—	mA
V _{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E _{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V _{OFFSET}	Offset voltage external reference	—	±3	9	mV

Table 25. ADC Parameters¹ (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

¹ All measurements are preliminary pending full characterization, and made at $V_{DD} = 3.3\text{ V}$, $V_{REFH} = 3.3\text{ V}$, and $V_{REFL} = \text{ground}$

² INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

³ LSB = Least Significant Bit

⁴ INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

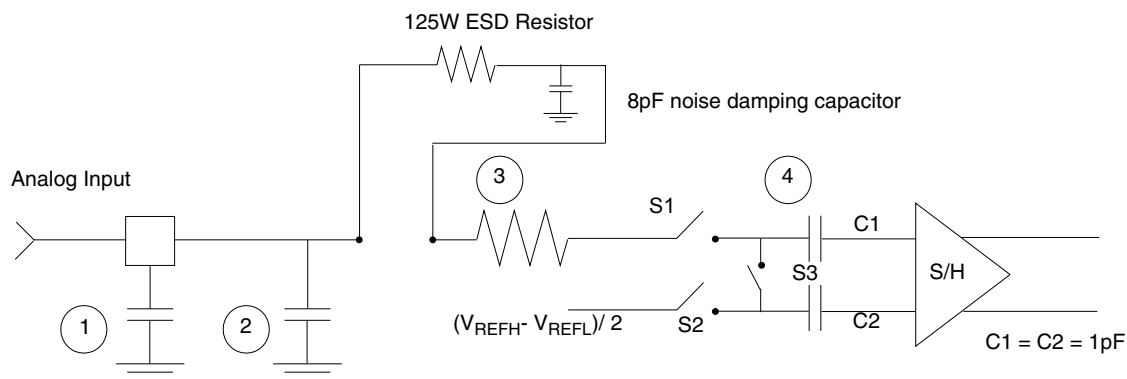
⁵ Includes power-up of ADC and V_{REF}

⁶ ADC clock cycles

⁷ Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH} - V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH} - V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4 \times 10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

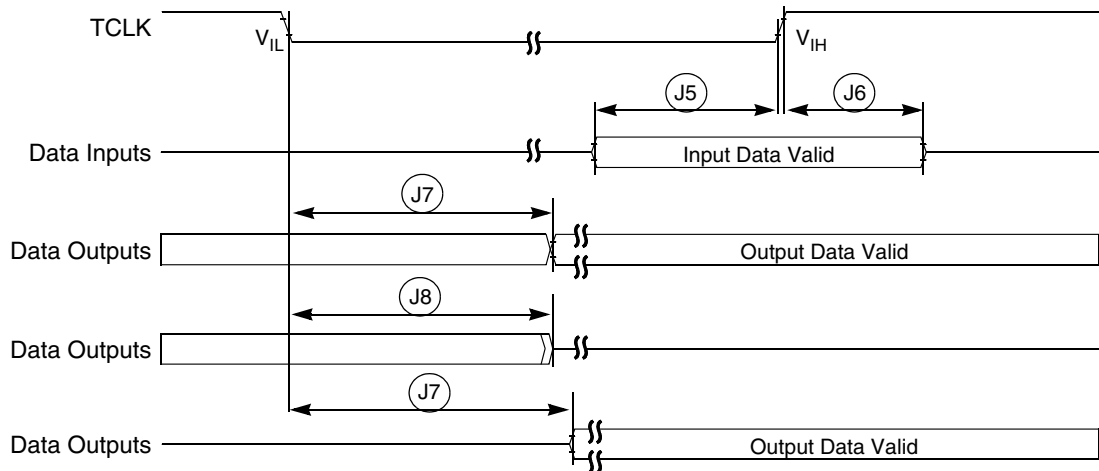


Figure 17. Boundary Scan (JTAG) Timing

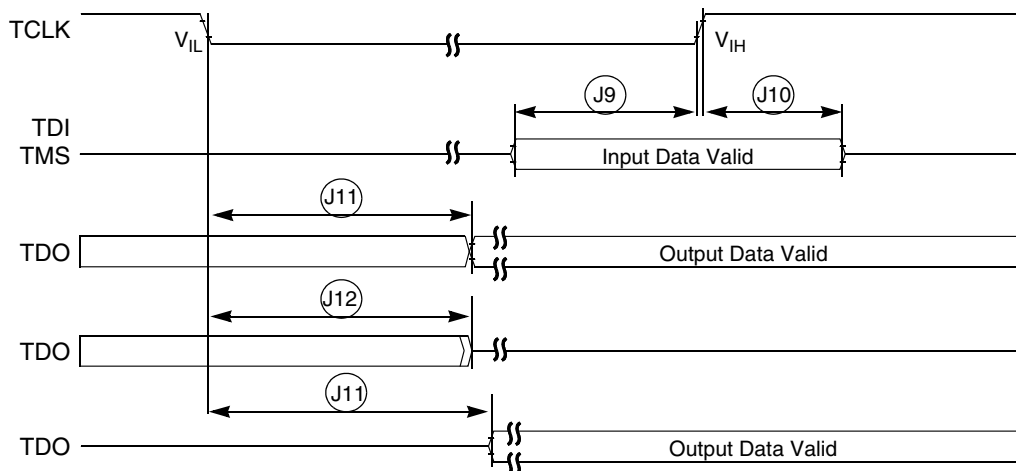
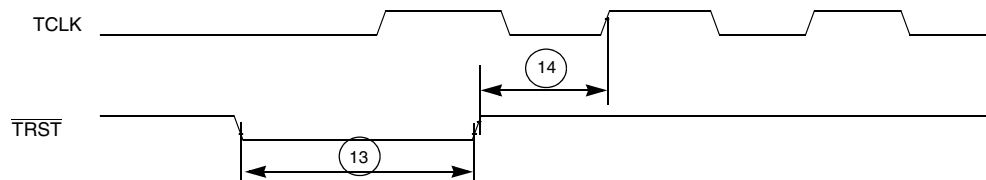


Figure 18. Test Access Port Timing

Figure 19. $\overline{\text{TRST}}$ Timing

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	<ul style="list-style-type: none"> Added package dimensions to package diagrams Added listing of devices for MCF52259 family Changed "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation" to "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation" Updated the figure Pinout Top View (144 MAPBGA) Removed an extraneous instance of the table Pin Functions by Primary and Alternate Purpose In the table Pin Functions by Primary and Alternate Purpose, changed a footnote from "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC" to "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL" In the table SGFM Flash Program and Erase Characteristics, changed "(V_{DDF} = 2.7 to 3.6 V)" to "(V_{DD} = 3.0 to 3.6 V)" In the table SGFM Flash Module Life Characteristics, changed "(V_{DDF} = 2.7 to 3.6 V)" to "(V_{DD} = 3.0 to 3.6 V)" In the table Oscillator and PLL Specifications, changed "V_{DD} and V_{DDPLL} = 2.7 to 3.6 V" to "V_{DD} and V_{DDPLL} = 3.0 to 3.6 V" In the table Reset and Configuration Override Timing, changed "V_{DD} = 2.7 to 3.6 V" to "V_{DD} = 3.0 to 3.6 V"
2	<ul style="list-style-type: none"> Added EzPort Electrical Specifications. Updated Table 2 for part numbers. In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values, JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. Updated Table 14. Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	<ul style="list-style-type: none"> Updated EzPort Electrical Specifications Added hysteresis note in the DC electrical table Clarified pin function table for VSS pins. Clarified orderable part summary.
4	<ul style="list-style-type: none"> Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, "This value has been update" Updated crystal frequency value to 25 MHz
5	<ul style="list-style-type: none"> Updated TOC

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