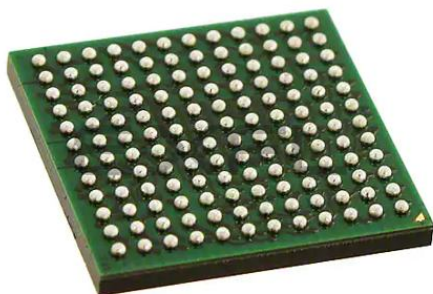


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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52259cvn80j

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

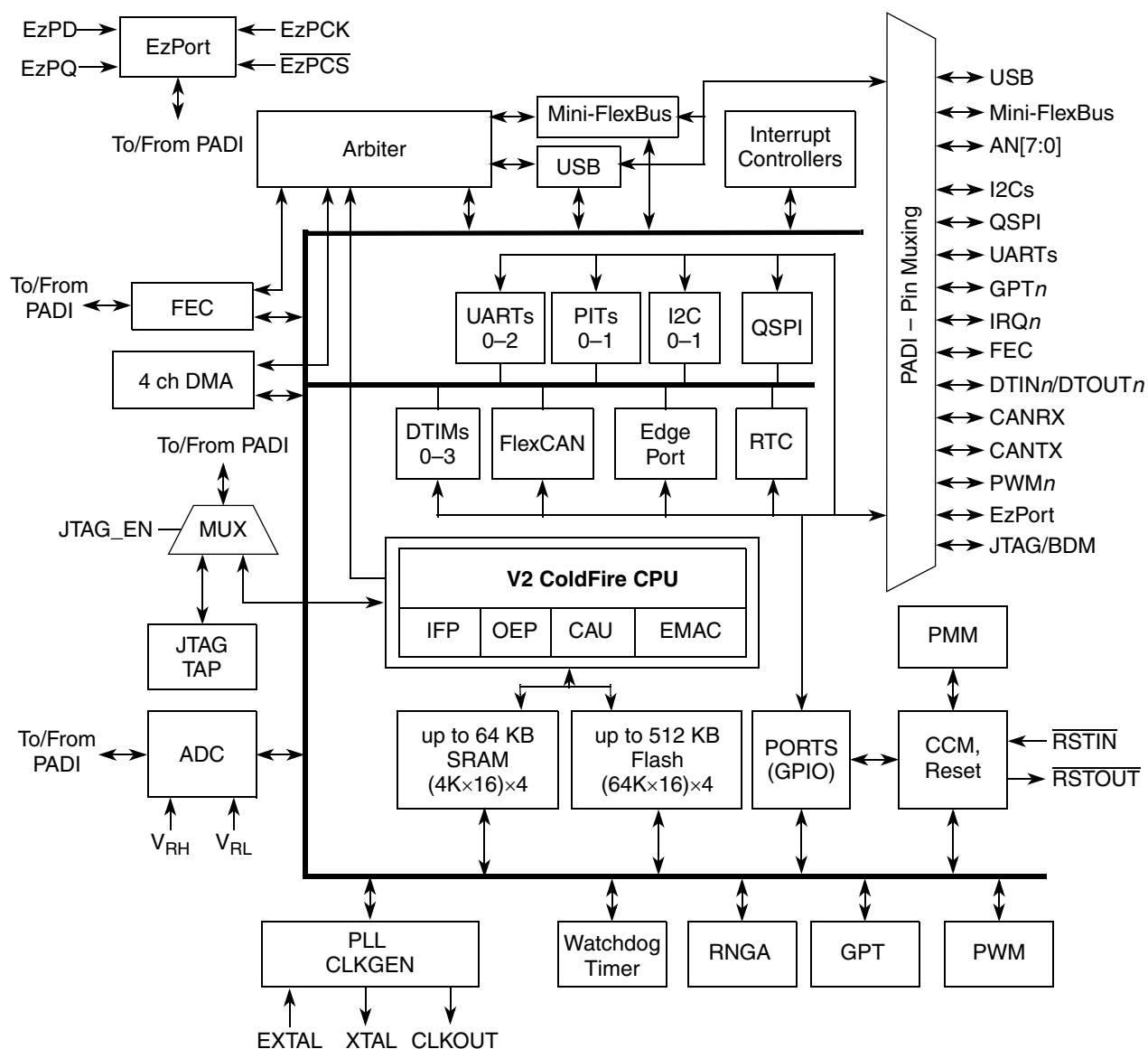


Figure 1. MCF52259 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip

Family Configurations

- Up to 80 MHz processor core frequency
- 40 MHz or 33 MHz peripheral bus frequency
- Sixteen general-purpose, 32-bit data and address registers
- Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
- Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 48$ operations
- Cryptographic Acceleration Unit (CAU)
 - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
 - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
 - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
 - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
 - Based on and includes all existing features of the Freescale TouCAN module
 - Full implementation of the CAN protocol specification version 2.0B
 - Standard data and remote frames (up to 109 bits long)
 - Extended data and remote frames (up to 127 bits long)
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
 - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
 - Unused MB space can be used as general purpose RAM space
 - Listen-only mode capability
 - Content-related addressing
 - No read/write semaphores
 - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
 - Programmable transmit-first scheme: lowest ID or lowest buffer number
 - Time stamp based on 16-bit free-running timer
 - Global network time, synchronized by a specific message
 - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
 - Full-speed / low-speed host controller
 - USB 1.1 and 2.0 compliant full-speed / low speed device controller
 - 16 bidirectional end points

- Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
- System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
- Low power modes supported
- 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
 - Uniquely programmable vectors for all interrupt sources
 - Fully programmable level and priority for all peripheral interrupt sources
 - Seven external interrupt signals with fixed level and priority
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low-power modes
- DMA controller
 - Four fully programmable channels
 - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
 - Source/destination address pointers that can increment or remain constant
 - 24-bit byte transfer counter per channel
 - Auto-alignment transfers supported for efficient block movement
 - Bursting and cycle-steal support
 - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
 - Channel linking support
- Reset
 - Separate reset in and reset out signals
 - Seven sources of reset:
 - Power-on reset (POR)
 - External
 - Software
 - Watchdog
 - Loss of clock / loss of lock
 - Low-voltage detection (LVD)
 - JTAG
 - Status flag indication of source of last reset
- Chip configuration module (CCM)
 - System configuration during reset
 - Selects one of six clock modes
 - Configures output pad drive strength
 - Unique part identification number and part revision number
- General purpose I/O interface
 - Up to 56 bits of general purpose I/O on 100-pin package
 - Up to 96 bits of general purpose I/O on 144-pin package
 - Bit manipulation supported via set/clear functions
 - Programmable drive strengths
 - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.9 Mini-FlexBus

A multi-function external bus interface called the Mini-FlexBus is provided on the device with basic functionality of interfacing to slave-only devices with a maximum slave bus frequency up to 40 MHz in 1:2 mode and 80 MHz in 1:1 mode. It can be directly connected to the following asynchronous or synchronous devices with little or no additional circuitry:

- External ROMs
- Flash memories
- Programmable logic devices
- Other simple target (slave) devices

The Mini-FlexBus is a subset of the FlexBus module found on higher-end ColdFire microprocessors. The Mini-FlexBus minimizes package pin-outs while maintaining a high level of configurability and functionality.

1.2.10 USB On-The-Go Controller

The device includes a Universal Serial Bus On-The-Go (USB OTG) dual-mode controller. USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and handheld computers to host PCs. The OTG supplement to the USB specification extends USB to peer-to-peer application, enabling devices to connect directly to each other without the need for a PC. The dual-mode controller on the device can act as a USB OTG host and as a USB device. It also supports full-speed and low-speed modes.

1.2.11 Fast Ethernet Controller (FEC)

The Ethernet media access controller (MAC) supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FECs supports the 10/100 Mbps MII, and the 10 Mbps-only 7-wire interface.

1.2.12 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.13 I2C Bus

The processor includes two I2C modules. The I2C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.14 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.15 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing. Signals on the SYNCA and SYNCA pins initiate an ADC conversion.

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.24 Interrupt Controllers (INTC_n)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR_n[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.2.27 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

1.2.28 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable part number summary

Freescall Part Number	FlexCAN	Encryption	Speed (MHz)	Flash (KB)	SRAM (KB)	Package	Temp range (°C)
MCF52252AF80	—	—	80	256	32	100 LQFP	0 to +70
MCF52252CAF66	•	—	66				-40 to +85
MCF52254AF80	—	—	80	512	64	100 LQFP	0 to +70
MCF52254CAF66	•	—	66				-40 to +85
MCF52255CAF80	•	•	80	512	64	100 LQFP	-40 to +85
MCF52256AG80	—	—	80	256	32	144 LQFP	0 to +70
MCF52256CAG66	•	—	66		64		-40 to +85
MCF52256CVN66	•	—	66		64	144 MAPBGA	-40 to +85
MCF52256VN80	—	—	80		32		0 to +70
MCF52258AG80	—	—	80	512	64	144 LQFP	0 to +70
MCF52258CAG66	•	—	66				-40 to +85
MCF52258CVN66	•	—	66			144 MAPBGA	-40 to +85
MCF52258VN80	—	—	80				0 to +70
MCF52259CAG80	•	•	80	512	64	144 LQFP	-40 to +85
MCF52259CVN80	•	•				144 MAPBGA	-40 to +85

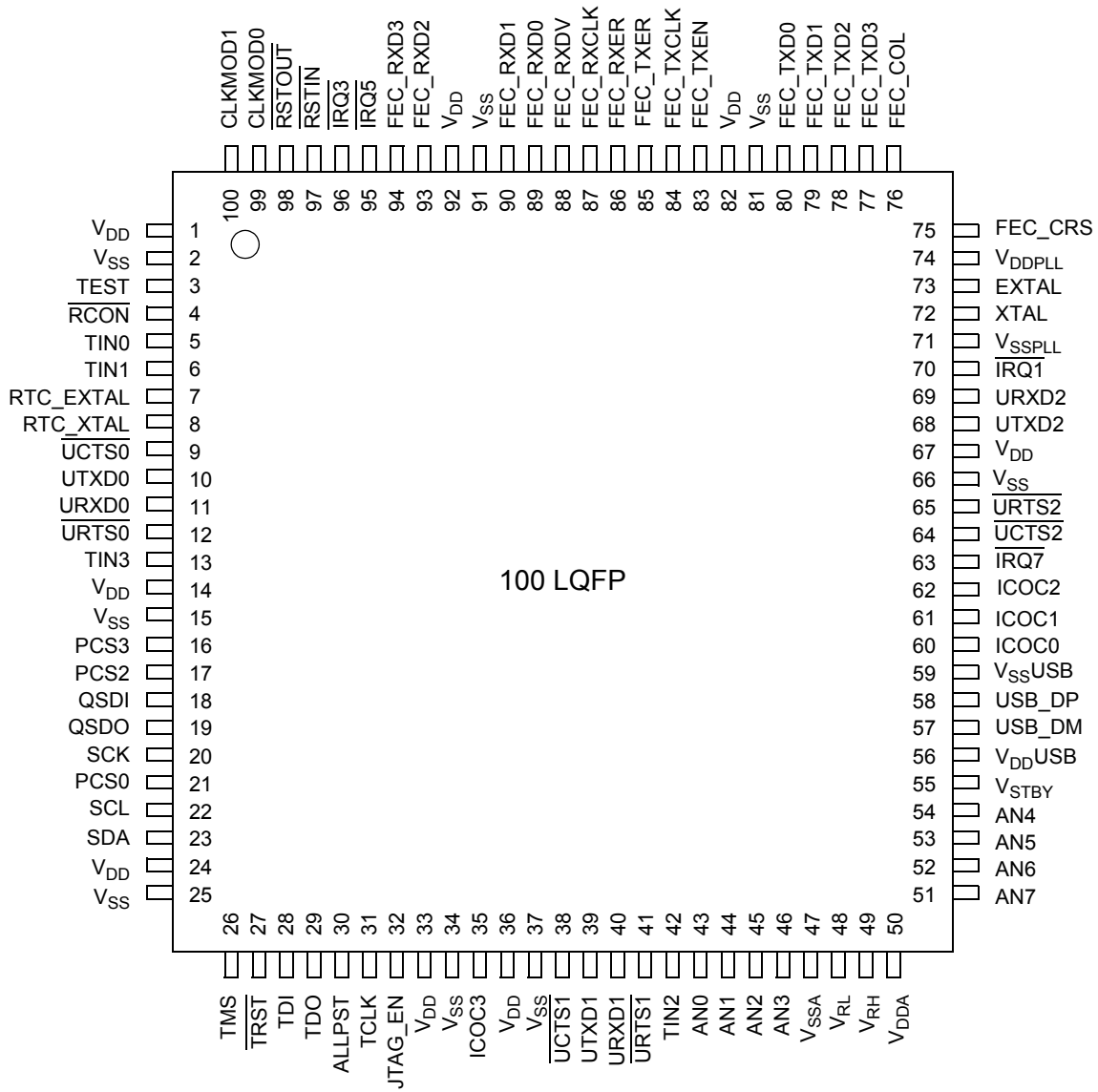


Figure 3. 100 LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 100 LQFP.

Figure 4 shows the pinout configuration for the 144 MAPBGA.

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VSS	RSTOUT	RSTIN	FB_D6	FB_D7	IRQ3	IRQ5	FEC_RXD0	FEC_RXER	FEC_TXEN	FEC_TXD3	VSS	A
B	TEST	FB_A14	FB_D4	FB_D5	FB_OE	FB_A19	FEC_RXD1	FEC_RXCLK	FEC_TXCLK	FEC_TXD2	FEC_COL	FEC_CRS	B
C	TIN1	FB_A12	FB_A13	FB_A15	FB_A16	FB_A18	FEC_RXD2	FEC_RXDV	FEC_TXD1	URXD2	VDDPLL	EXTAL	C
D	RTC_EXTAL	TIN0	FB_A11	CLKMOD1	CLKMOD0	FB_A17	FEC_RXD3	FEC_TXER	FEC_TXD0	UTXD2	VSSPLL	XTAL	D
E	RTC_XTAL	UCTS0	FB_A10	RCON	VDD	VDD	VDD	VDD	IRQ1	URTS2	UCTS2	IRQ7	E
F	UTXD0	URXD0	URTS0	TIN3	VDD	VSS	VSS	VSS	PST3	DDATA0	DDATA1	ICOC0	F
G	QSDO	QSDI	PCS2	PCS3	VDD	VSS	VSS	VSS	DDATA3	PST2	PST1	PST0	G
H	SCL	SDA	SCK	PCS0	VDD	VDD	VDD	VSS	VSSUSB	DDATA2	USB_DM	USB_DP	H
J	FB_A6	FB_A7	FB_A9	FB_A8	FB_D0	FB_A3	VDD	TIN2	VDDUSB	ICOC2	ICOC1	VSTBY	J
K	TMS	TRST	FB_ALE	FB_A5	FB_D2	FB_A4	UCTS1	UTXD1	AN3	AN6	AN4	AN5	K
L	TDI	TDO	ALLPST	FB_D3	FB_D1	FB_A1	FB_A0	URXD1	AN2	VRH	VDDA	AN7	L
M	VSS	JTAG_EN	TCLK	FB_RW	FB_CS0	FB_A2	ICOC3	URTS1	AN0	AN1	VRL	VSSA	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 4. Pinout Top View (144 MAPBGA)

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 4. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	+1.8 to 3.5	V
USB standby supply voltage	V_{DDUSB}	−0.3 to +4.0	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 or 0 to 70 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see orderable part number summary (Table 2)

Table 7. Current Consumption in Low-Power Mode, Code From SRAM^{1,2,3}

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11) ⁴	0.090				mA	I _{DD}
Stop mode 2 (Stop 10) ⁴	7					
Stop mode 1 (Stop 01) ^{4,5}	9	10	15	17		
Stop mode 0 (Stop 00) ⁵	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

¹ All values are measured with a 3.3 V power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.

³ CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.

⁴ See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.

⁵ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

Table 8. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	30 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	43 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	26 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	16 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	44 ^{7,8}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{1,9}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	35 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	23 ¹⁰	°C/W
	Junction to case	—	θ_{JC}	7 ¹¹	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ¹²	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

- ¹⁶ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ¹⁷ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- ¹⁸ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

- T_A = ambient temperature, °C
 Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
 P_D = $P_{INT} + P_{I/O}$
 P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, W
 $P_{I/O}$ = power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in [Table 9](#) and [Table 10](#).

Table 9. SGFM Flash Program and Erase Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{\text{sys(R)}}$	0	—	66.67 or 80 ¹	MHz
System clock (program/erase) ²	$f_{\text{sys(P/E)}}$	0.15	—	66.67 or 80 ¹	MHz

¹ Depending on packaging; see the orderable part number summary ([Table 2](#)).

² Refer to the flash memory section for more information ([Section 2.4, “Flash Memory Characteristics”](#))

Table 10. SGFM Flash Module Life Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

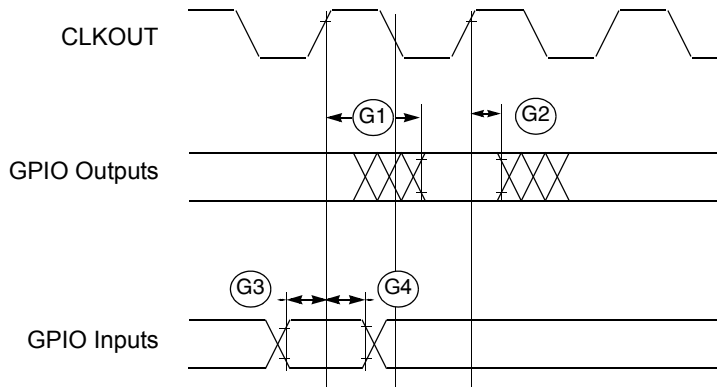


Figure 11. GPIO Timing

2.13 Reset Timing

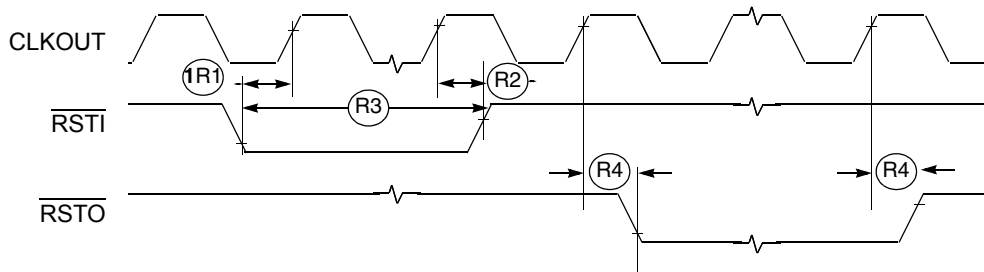
Table 22. Reset and Configuration Override Timing

($V_{DD} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H)¹

NUM	Characteristic	Symbol	Min	Max	Unit
R1	\overline{RSTI} input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to \overline{RSTI} Input invalid	t_{CHRI}	1.5	—	ns
R3	\overline{RSTI} input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to \overline{RSTO} Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the \overline{RSTI} input are bypassed and \overline{RSTI} is asserted asynchronously to the system. Thus, \overline{RSTI} must be held a minimum of 100 ns.

Figure 12. \overline{RSTI} and Configuration Override Timing

2.14 I2C Input/Output Timing Specifications

Table 23 lists specifications for the I2C input timing parameters shown in Figure 13.

Table 23. I2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 24 lists specifications for the I2C output timing parameters shown in Figure 13.

Table 24. I2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1 ¹	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2 ¹	Clock low period	$10 \times t_{CYC}$	—	ns
I3 ²	I2C_SCL/I2C_SDA rise time ($V_{IL} = 0.5 \text{ V}$ to $V_{IH} = 2.4 \text{ V}$)	—	—	μs
I4 ¹	Data hold time	$7 \times t_{CYC}$	—	ns
I5 ³	I2C_SCL/I2C_SDA fall time ($V_{IH} = 2.4 \text{ V}$ to $V_{IL} = 0.5 \text{ V}$)	—	3	ns
I6 ¹	Clock high time	$10 \times t_{CYC}$	—	ns
I7 ¹	Data setup time	$2 \times t_{CYC}$	—	ns
I8 ¹	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9 ¹	Stop condition setup time	$10 \times t_{CYC}$	—	ns

¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

³ Specified at a nominal 50 pF load.

Figure 13 shows timing for the values in Table 23 and Table 24.

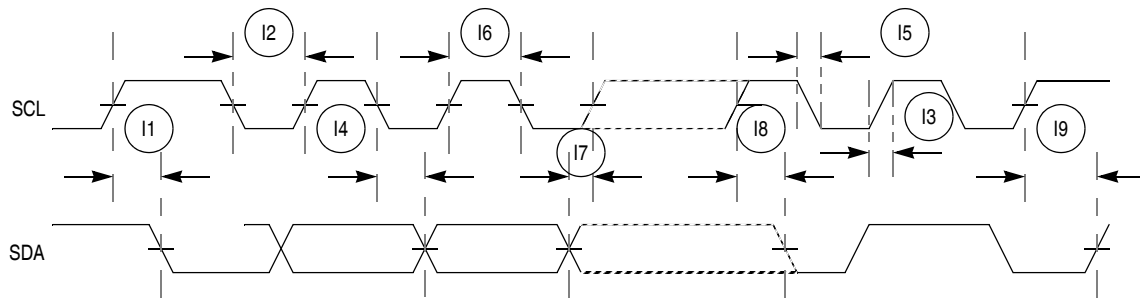


Figure 13. I2C Input/Output Timings

2.15 Analog-to-Digital Converter (ADC) Parameters

Table 25 lists specifications for the analog-to-digital converter.

Table 25. ADC Parameters¹

Name	Characteristic	Min	Typical	Max	Unit
V _{REFL}	Low reference voltage	V _{SSA}	—	V _{SSA} + 50 mV	V
V _{REFH}	High reference voltage	V _{DDA} - 50 mV	—	V _{DDA}	V
V _{DDA}	ADC analog supply voltage	3.1	3.3	3.6	V
V _{ADIN}	Input voltages	V _{REFL}	—	V _{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range) ²	—	±2.5	±3	LSB ³
INL	Integral non-linearity (10% to 90% input signal range) ⁴	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	-1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f _{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R _{AD}	Conversion range	V _{REFL}	—	V _{REFH}	V
t _{ADPU}	ADC power-up time ⁵	—	6	13	t _{AIC} cycles ⁶
t _{REC}	Recovery from auto standby	—	0	1	t _{AIC} cycles
t _{ADC}	Conversion time	—	6	—	t _{AIC} cycles
t _{ADS}	Sample time	—	1	—	t _{AIC} cycles
C _{ADI}	Input capacitance	—	See Figure 14	—	pF
X _{IN}	Input impedance	—	See Figure 14	—	W
I _{ADI}	Input injection current ⁷ , per pin	—	—	3	mA
I _{VREFH}	V _{REFH} current	—	0	—	mA
V _{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E _{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V _{OFFSET}	Offset voltage external reference	—	±3	9	mV

Table 25. ADC Parameters¹ (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

¹ All measurements are preliminary pending full characterization, and made at $V_{DD} = 3.3\text{ V}$, $V_{REFH} = 3.3\text{ V}$, and $V_{REFL} = \text{ground}$

² INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

³ LSB = Least Significant Bit

⁴ INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

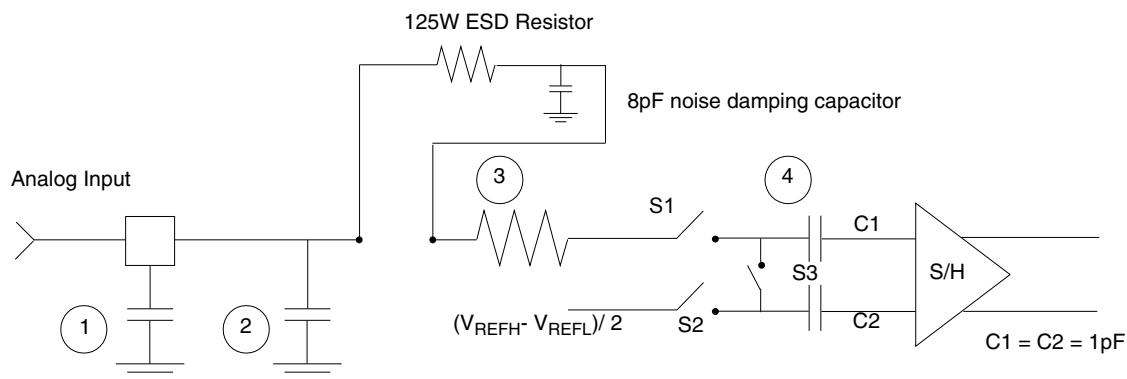
⁵ Includes power-up of ADC and V_{REF}

⁶ ADC clock cycles

⁷ Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH} - V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH} - V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4 \times 10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

Table 26. Timer Module AC Timing Specifications

Name	Characteristic ¹	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

¹ All timing references to CLKOUT are given to its rising edge.

2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

Table 27. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.

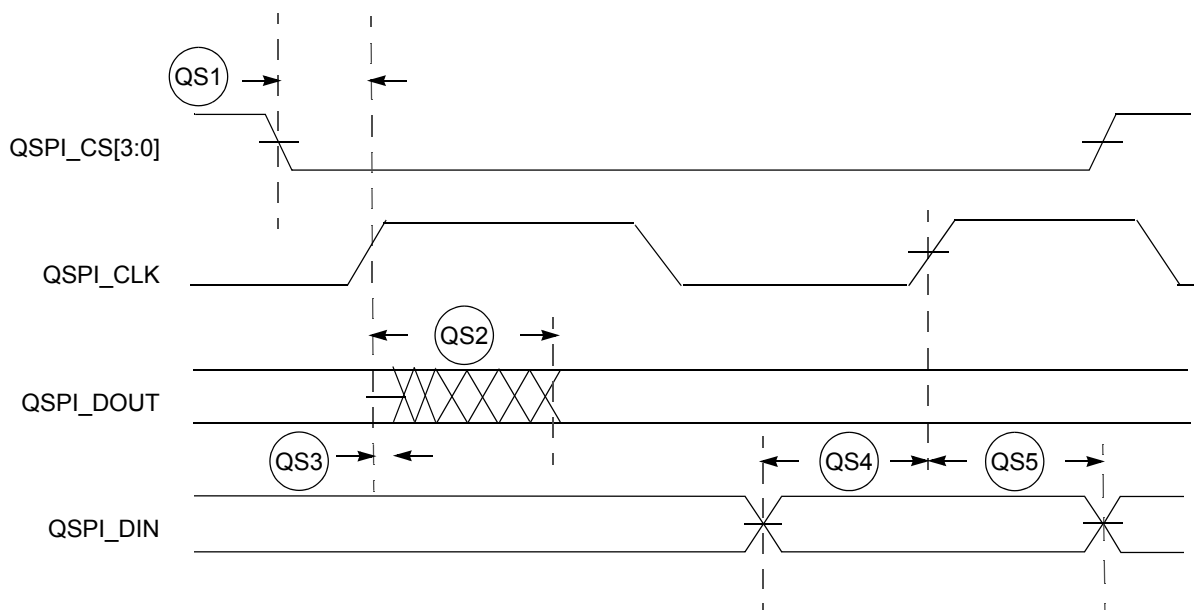


Figure 15. QSPI Timing

2.19 JTAG and Boundary Scan Timing

Table 28. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{\text{sys}}/2$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{\text{CYC}}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

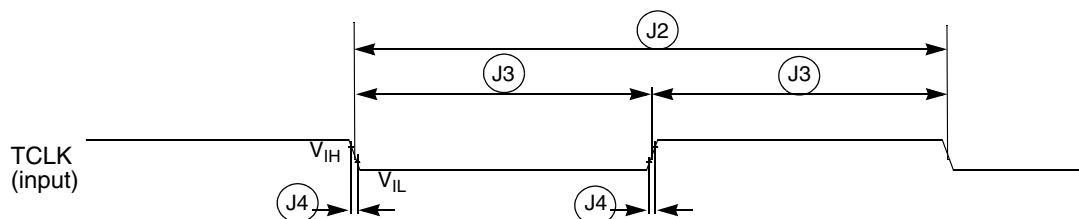


Figure 16. Test Clock Input Timing

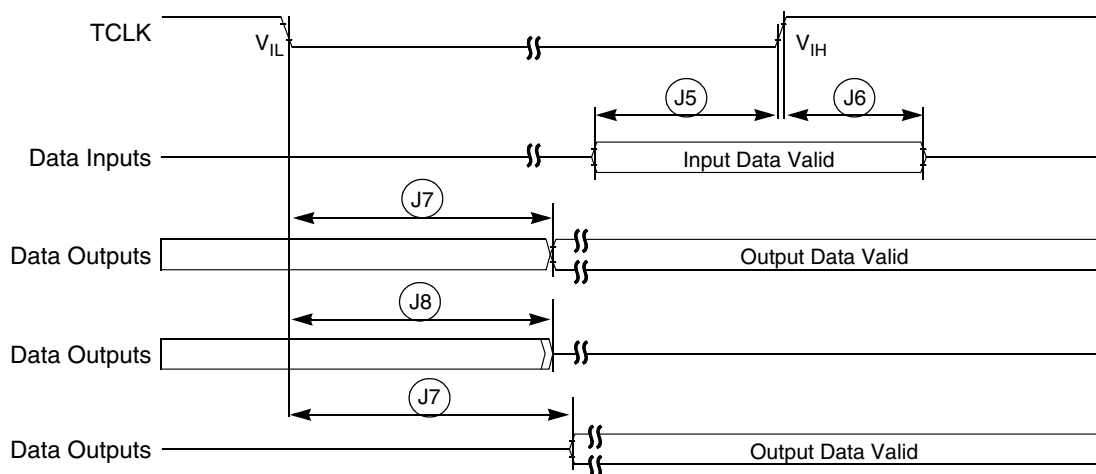


Figure 17. Boundary Scan (JTAG) Timing

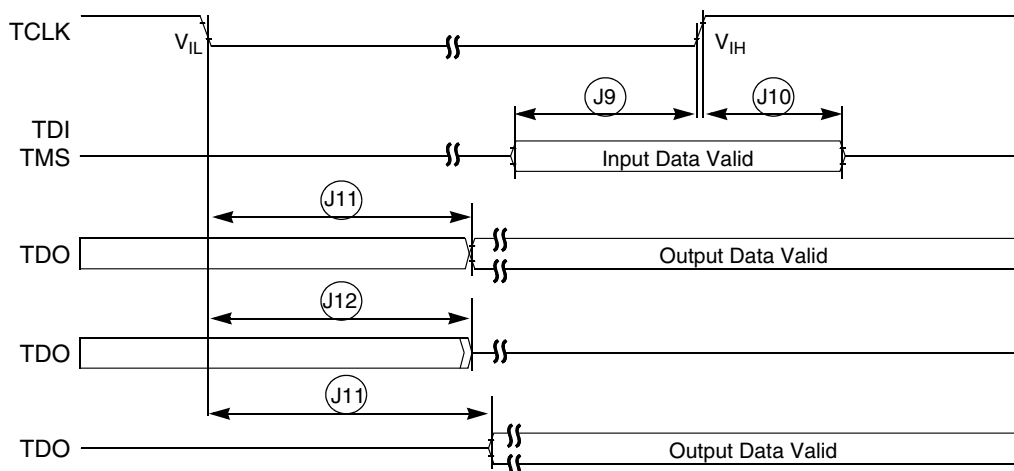
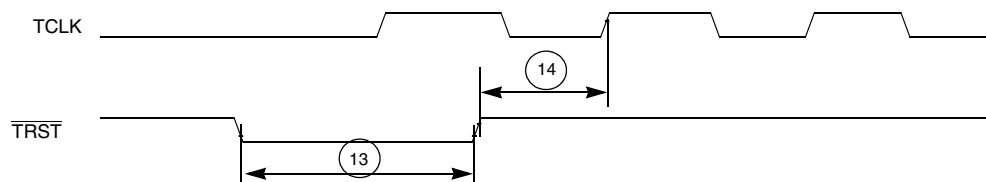


Figure 18. Test Access Port Timing

Figure 19. $\overline{\text{TRST}}$ Timing

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	<ul style="list-style-type: none"> Added package dimensions to package diagrams Added listing of devices for MCF52259 family Changed "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation" to "Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation" Updated the figure Pinout Top View (144 MAPBGA) Removed an extraneous instance of the table Pin Functions by Primary and Alternate Purpose In the table Pin Functions by Primary and Alternate Purpose, changed a footnote from "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC" to "This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL" In the table SGFM Flash Program and Erase Characteristics, changed "(V_{DDF} = 2.7 to 3.6 V)" to "(V_{DD} = 3.0 to 3.6 V)" In the table SGFM Flash Module Life Characteristics, changed "(V_{DDF} = 2.7 to 3.6 V)" to "(V_{DD} = 3.0 to 3.6 V)" In the table Oscillator and PLL Specifications, changed "V_{DD} and V_{DDPLL} = 2.7 to 3.6 V" to "V_{DD} and V_{DDPLL} = 3.0 to 3.6 V" In the table Reset and Configuration Override Timing, changed "V_{DD} = 2.7 to 3.6 V" to "V_{DD} = 3.0 to 3.6 V"
2	<ul style="list-style-type: none"> Added EzPort Electrical Specifications. Updated Table 2 for part numbers. In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values, JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. Updated Table 14. Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	<ul style="list-style-type: none"> Updated EzPort Electrical Specifications Added hysteresis note in the DC electrical table Clarified pin function table for VSS pins. Clarified orderable part summary.
4	<ul style="list-style-type: none"> Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, "This value has been update" Updated crystal frequency value to 25 MHz
5	<ul style="list-style-type: none"> Updated TOC