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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf52252af80

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  - Up to 80 MHz processor core frequency
  - 40 MHz or 33 MHz peripheral bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support 16×16 → 32 or 32×32 → 48 operations
  - Cryptographic Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
  - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/s
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate (EMAC) unit for improved signal processing capabilities. The EMAC implements a three-stage arithmetic pipeline, optimized for 32x32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The EMAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 144-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 144-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 64 KB memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64 KB boundary within the 4 GB address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA, FEC, and USB. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor’s high-speed local bus. The CFM is constructed with four banks of 64 KB×16-bit flash memory arrays to generate 512 KB of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Cryptographic Acceleration Unit

The MCF52235 device incorporates two hardware accelerators for cryptographic functions. First, the CAU is a coprocessor tightly-coupled to the V2 ColdFire core that implements a set of specialized operations to increase the throughput of software-based encryption and message digest functions, specifically the DES, 3DES, AES, MD5 and SHA-1 algorithms. Second, a random number generator provides FIPS-140 compliant 32-bit values to security processing routines. Both modules supply critical acceleration to software-based cryptographic algorithms at a minimal hardware cost.

1.2.7 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.8 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.9 Mini-FlexBus

A multi-function external bus interface called the Mini-FlexBus is provided on the device with basic functionality of interfacing to slave-only devices with a maximum slave bus frequency up to 40 MHz in 1:2 mode and 80 MHz in 1:1 mode. It can be directly connected to the following asynchronous or synchronous devices with little or no additional circuitry:

- External ROMs
- Flash memories
- Programmable logic devices
- Other simple target (slave) devices

The Mini-FlexBus is a subset of the FlexBus module found on higher-end ColdFire microprocessors. The Mini-FlexBus minimizes package pin-outs while maintaining a high level of configurability and functionality.

1.2.10 USB On-The-Go Controller

The device includes a Universal Serial Bus On-The-Go (USB OTG) dual-mode controller. USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and handheld computers to host PCs. The OTG supplement to the USB specification extends USB to peer-to-peer application, enabling devices to connect directly to each other without the need for a PC. The dual-mode controller on the device can act as a USB OTG host and as a USB device. It also supports full-speed and low-speed modes.

1.2.11 Fast Ethernet Controller (FEC)

The Ethernet media access controller (MAC) supports 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver. The FECs supports the 10/100 Mbps MII, and the 10 Mbps-only 7-wire interface.

1.2.12 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.13 I2C Bus

The processor includes two I2C modules. The I2C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.14 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.15 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing. Signals on the SYNCA and SYNCB pins initiate an ADC conversion.

Figure 2 shows the pinout configuration for the 144 LQFP.

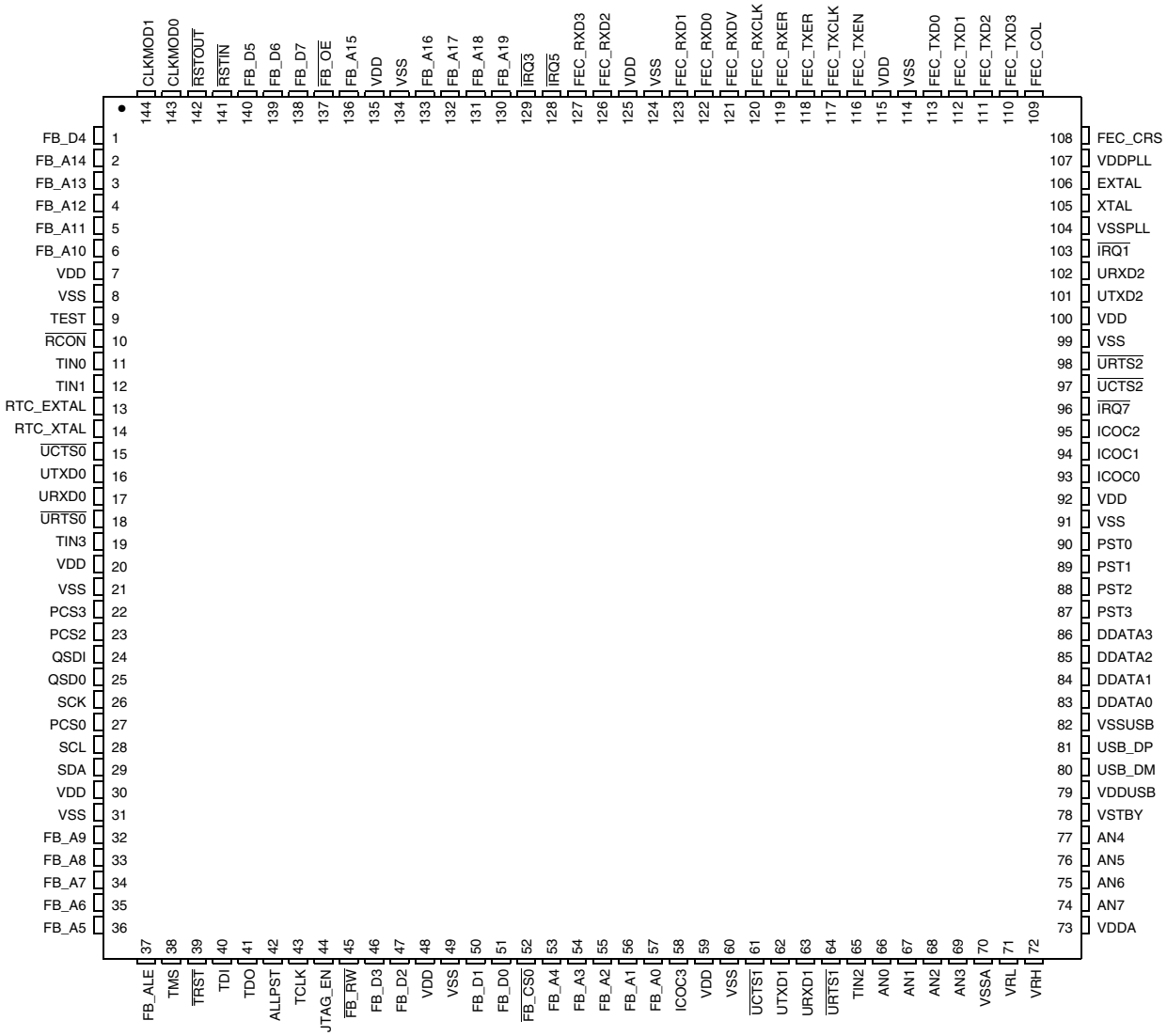


Figure 2. 144 LQFP Pin Assignment

Figure 3 shows the pinout configuration for the 100 LQFP.

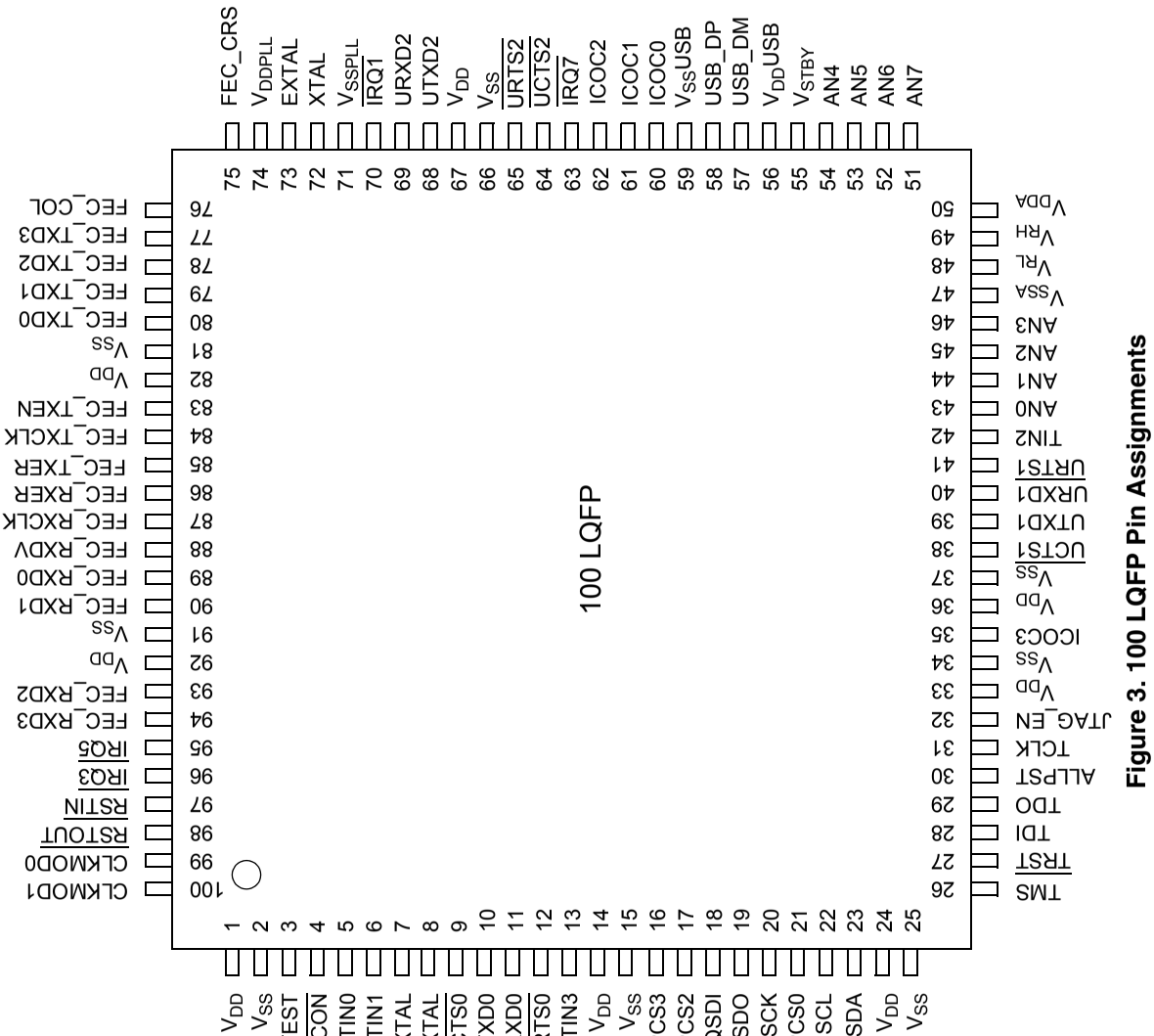


Figure 3. 100 LQFP Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
FEC	FEC_COL	—	—	PTI0	PSRRH[0]	PDSRH[0]	—	B11	109	76
	FEC_CRS	—	—	PTI1	PSRRH[1]	PDSRH[1]	—	B12	108	75
	FEC_RXCLK	—	—	PTI2	PSRRH[2]	PDSRH[2]	—	B8	120	87
	FEC_RXD[3:0]	—	—	PTI[6:3]	PSRRH[6:3]	PDSRH[6:3]	—	D7, C7, B7, A8	127, 126, 123, 122	94, 93, 90, 89
	FEC_RXDV	—	—	PTI7	PSRRH[7]	PDSRH[7]	—	C8	121	88
	FEC_RXER	—	—	PTJ0	PSRRH[8]	PDSRH[8]	—	A9	119	86
	FEC_TXCLK	—	—	PTJ1	PSRRH[9]	PDSRH[9]	—	B9	117	84
	FEC_TXD[3:0]	—	—	PTJ[5:2]	PSRRH[13:10]	PDSRH[13:10]	—	A11, B10, C9, D9	110–113	77, 78, 79, 80
FEC	FEC_TXEN	—	—	PTJ6	PSRRH[14]	PDSRH[14]	—	A10	116	83
	FEC_TXER	—	—	PTJ7	PSRRH[15]	PDSRH[15]	—	D8	118	85
I2C0[3]	I2C_SCL0	—	UTXD2	PAS0	PSRR[0]	PDSR[0]	Pull-Up[4]	H1	28	22
	I2C_SDA0	—	URXD2	PAS1	PSRR[0]	PDSR[0]	Pull-Up[4]	H2	29	23
Interrupts	IRQ7	—	—	PNQ7	Low	Low	Pull-Up[4]	E12	96	63
	IRQ5	FEC_MDC	—	PNQ5	Low	Low	Pull-Up[4]	A7	128	95
	IRQ3	FEC_MDIO	—	PNQ3	Low	Low	Pull-Up[4]	A6	129	96
	IRQ1	—	USB_ALTCLK	PNQ1	Low	High	Pull-Up[4]	E9	103	70
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	Pull-Down	M2	44	32
	TCLK/ PSTCLK/ CLKOUT	—	FB_CLK	—	Low	Low	Pull-Up[5]	M3	43	31
	TDI/DSI	—	—	—	N/A	N/A	Pull-Up[5]	L1	40	28
	TDO/DSO	—	—	—	Low	Low	—	L2	41	29
	TMS/$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	Pull-Up[5]	K1	38	26
	$\overline{\text{TRST}}$/DSCLK	—	—	—	N/A	N/A	Pull-Up[5]	K2	39	27

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mode Selection	$\overline{\text{RCON}}$/$\overline{\text{EZPCS}}$	—	—	—	N/A	N/A	Pull-Up	E4	10	4
	CLKMOD[1:0]	—	—	—	N/A	N/A	Pull-Down	D4, D5	144, 143	100, 99
QSPI	QSPI_CS3	SYNCA	USB_DP_PDOWN	PQS6	PSRR[7]	PDSR[7]	—	G4	22	16
	QSPI_CS2	SYNCB	USB_DM_PDOWN	PQS5	PSRR[6]	PDSR[6]	—	G3	23	17
	QSPI_CS0	I2C_SDA0	UCTS1	PQS3	PSRR[4]	PDSR[4]	Pull-Up[6]	H4	27	21
	QSPI_CLK/ EZPCK	I2C_SCL0	URTS1	PQS2	PSRR[3]	PDSR[3]	Pull-Up[6]	H3	26	20
QSPI	QSPI_DIN/ EZPD	I2C_SDA1	URXD1	PQS1	PSRR[2]	PDSR[2]	Pull-Up[6]	G2	24	18
	QSPI_DOUT/EZPQ	I2C_SCL1	UTXD1	PQS0	PSRR[1]	PDSR[1]	Pull-Up[6]	G1	25	19
Reset[7]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	Pull-Up[7]	A3	141	97
	$\overline{\text{RSTO}}$	—	—	—	Low	High	—	A2	142	98
Test	TEST	—	—	—	N/A	N/A	Pull-Down	B1	9	3
Timer 3, 16-bit	GPT3	—	PWM7	PTA3	PSRR[23]	PDSR[23]	Pull-Up[8]	M7	58	35
Timer 2, 16-bit	GPT2	—	PWM5	PTA2	PSRR[22]	PDSR[22]	Pull-Up[8]	J10	95	62
Timer 1, 16-bit	GPT1	—	PWM3	PTA1	PSRR[21]	PDSR[21]	Pull-Up[8]	J11	94	61
Timer 0, 16-bit	GPT0	—	PWM1	PTA0	PSRR[20]	PDSR[20]	Pull-Up[8]	F12	93	60
Timer 3, 32-bit	DTIN3	DTOUT3	PWM6	PTC3	PSRR[19]	PDSR[19]	—	F4	19	13
Timer 2, 32-bit	DTIN2	DTOUT2	PWM4	PTC2	PSRR[18]	PDSR[18]	—	J8	65	42

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Timer 1, 32-bit	DTIN1	DTOUT1	PWM2	PTC1	PSRR[17]	PDSR[17]	—	C1	12	6
Timer 0, 32-bit	DTIN0	DTOUT0	PWM0	PTC0	PSRR[16]	PDSR[16]	—	D2	11	5
UART 0	UCTS0	—	USB_VBUSE	PUA3	PSRR[11]	PDSR[11]	—	E2	15	9
	URTS0	—	USB_VBUSD	PUA2	PSRR[10]	PDSR[10]	—	F3	18	12
	URXD0	—	—	PUA1	PSRR[9]	PDSR[9]	—	F2	17	11
	UTXD0	—	—	PUA0	PSRR[8]	PDSR[8]	—	F1	16	10
UART 1	UCTS1	SYNCA	URXD2	PUB3	PSRR[15]	PDSR[15]	—	K7	61	38
	URTS1	SYNCB	UTXD2	PUB2	PSRR[14]	PDSR[14]	—	M8	64	41
	URXD1	I2C_SDA1	—	PUB1	PSRR[13]	PDSR[13]	Pull-Up[6]	L8	63	40
	UTXD1	I2C_SCL1	—	PUB0	PSRR[12]	PDSR[12]	Pull-Up[6]	K8	62	39
UART 2	UCTS2	I2C_SCL1	USB_VBUSCHG	PUC3	PSRR[27]	PDSR[27]	Pull-Up[6]	E11	97	64
	URTS2	I2C_SDA1	USB_VBUSDIS	PUC2	PSRR[26]	PDSR[26]	Pull-Up[6]	E10	98	65
	URXD2	CANRX	—	PUC1	PSRR[25]	PDSR[25]	—	C10	102	69
	UTXD2	CANTX	—	PUC0	PSRR[24]	PDSR[24]	—	D10	101	68
USB OTG	USB_DM	—	—	—	N/A	N/A	—	H11	80	57
	USB_DP	—	—	—	N/A	N/A	—	H12	81	58
	USB_VDD	—	—	—	N/A	N/A	—	J9	79	56
	USB_VSS	—	—	—	N/A	N/A	—	H9	82	59

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mini-FlexBus[9]	FB_ALE	$\overline{\text{FB\_CS1}}$	—	PAS2	PSRRL[20]	PDSRL[20]	—	K3	37	—
	FB_AD[7:0]	—	—	PTE[7:0]	PSRRL[7:0]	PDSRL[7:0]	—	J2, J1, K4, K6, J6, M6, L6, L7	34–36; 53–57	—
	FB_AD[15:8]	—	—	PTF[7:0]	PSRRL[15:8]	PDSRL[15:8]	—	C4, B2, C3, C2, D3, E3, J3, J4	136, 2–6, 32–33	—
	FB_AD[19:16]	—	—	PTG[3:0]	PSRRL[19:16]	PDSRL[19:16]	—	B6, C6, D6, C5	130–133	—
	$\overline{\text{FB\_CS0}}$	—	—	PTG5	PSRRL[21]	PDSRL[21]	—	M5	52	—
	FB_R/$\overline{\text{W}}$	—	—	PTG7	PSRRL[31]	PDSRL[31]	—	M4	45	—
	$\overline{\text{FB\_OE}}$	—	—	PTG6	PSRRL[30]	PDSRL[30]	—	B5	137	—
	FB_D7	CANRX	—	PTH5	PSRRL[29]	PDSRL[29]	—	A5	138	—
	FB_D6	CANTX	—	PTH4	PSRRL[28]	PDSRL[28]	—	A4	139	—
	FB_D5	I2C_SCL1	—	PTH3	PSRRL[27]	PDSRL[27]	Pull-Up[6]	B4	140	—
	FB_D4	I2C_SDA1	—	PTH2	PSRRL[26]	PDSRL[26]	Pull-Up[6]	B3	1	—
	FB_D3	USB_ VBUSD	—	PTH1	PSRRL[25]	PDSRL[25]	—	L4	46	—
	FB_D2	USB_ VBUSE	—	PTH0	PSRRL[24]	PDSRL[24]	—	K5	47	—
	FB_D1	SYNCA	—	PTH7	PSRRL[23]	PDSRL[23]	—	L5	50	—
	FB_D0	SYNCB	—	PTH6	PSRRL[22]	PDSRL[22]	—	J5	51	—
Standby Voltage	VSTBY	—	—	—	N/A	N/A	—	J12	78	55
VDD[10]	VDD	—	—	—	N/A	N/A	—	E5–E8; F5; G5; H5–7; J7	7; 20; 30; 48; 59; 92; 100; 115; 125; 135	1; 14; 24; 33; 36; 67; 82; 92

Table 7. Current Consumption in Low-Power Mode, Code From SRAM[1,2,3]

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Unit	Symbol
Stop mode 3 (Stop 11)[4]	0.090				mA	I_{DD}
Stop mode 2 (Stop 10)[4]	7					
Stop mode 1 (Stop 01)[4,5]	9	10	15	17		
Stop mode 0 (Stop 00)[5]	9	10	15	17		
Wait / Doze	13	18	42	50		
Run	16	21	55	65		

1 All values are measured with a 3.3 V power supply. Tests performed at room temperature.
2 Refer to the Power Management chapter in the *MCF52259 Reference Manual* for more information on low-power modes.
3 CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.
4 See the description of the Low-Power Control Register (LPCR) in the *MCF52259 Reference Manual* for more information on stop modes 0–3.
5 Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

2.3 Thermal Characteristics

Table 8 lists thermal resistance values.

Table 8. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
144 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	30[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	43[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	26[1,3]	°C/W
	Junction to board	—	θ_{JB}	16[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
144 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	44[7,8]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35[1,9]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	35[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,3]	°C/W
	Junction to board	—	θ_{JB}	23[10]	°C/W
	Junction to case	—	θ_{JC}	7[11]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[12]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis[2]	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, digital pins	I_{in}	–1.0	1.0	μA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Output high voltage (high drive) I_{OH} = -5 mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) I_{OL} = 5 mA	V_{OL}	—	0.5	V
Output high voltage (low drive) I_{OH} = -2 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) I_{OL} = 2 mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[3]	I_{APU}	–10	–130	μA
Input Capacitance [4] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to Table 14 for additional PLL specifications.

2 Only for pins: IRQ1, IRQ3. IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

3 Refer to Table 3 for pins having internal pull-up devices.

4 This parameter is characterized before qualification rather than 100% tested.

2.9 USB Operation

Table 15. USB Operation Specifications

Characteristic	Symbol	Value	Unit
Minimum core speed for USB operation	$f_{sys\_USB\_min}$	16	MHz

2.10 Mini-FlexBus External Interface Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 16. Mini-FlexBus AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
	Frequency of Operation	—	80	MHz	
MB1	Clock Period	12.5	—	ns	
MB2	Output Valid	—	8	ns	[1]
MB3	Output Hold	2	—	ns	[1]
MB4	Input Setup	6	—	ns	[2]
MB5	Input Hold	0	—	ns	[2]

[1] Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

[2] Specification is valid for all MB_D[7:0].

2.11.3 Asynchronous Input Signal Timing Specifications

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
E9	CRS, COL minimum pulse width	1.5	—	TXCLK period

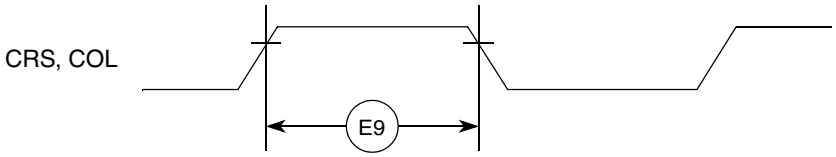


Figure 9. MII Async Inputs Timing Diagram

2.11.4 MII Serial Management Timing Specifications

Table 20. MII Serial Management Channel Signal Timing

Num	Characteristic	Symbol	Min	Max	Unit
E10	MDC cycle time	t_{MDC}	400	—	ns
E11	MDC pulse width		40	60	% t_{MDC}
E12	MDC to MDIO output valid		—	375	ns
E13	MDC to MDIO output invalid		25	—	ns
E14	MDIO input to MDC setup		10	—	ns
E15	MDIO input to MDC hold		0	—	ns

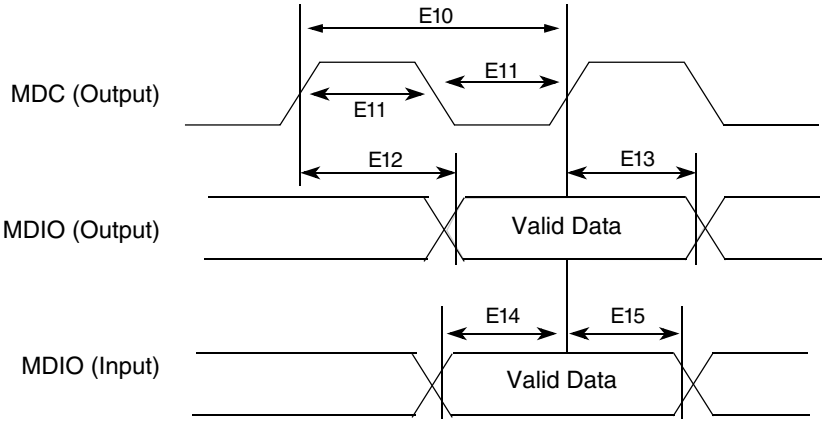


Figure 10. MII Serial Management Channel TIming Diagram

2.12 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 21 and Figure 11.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

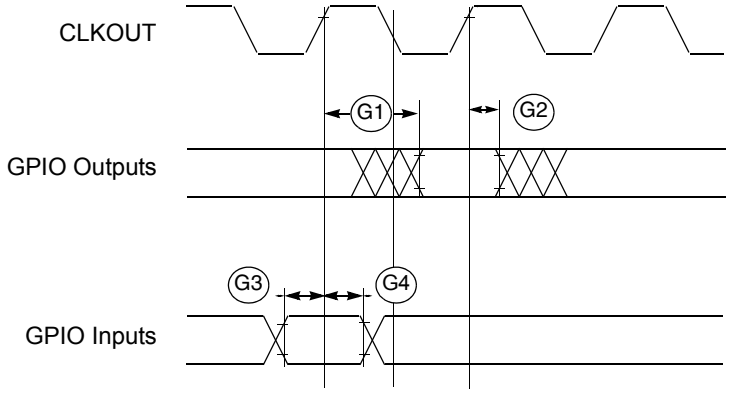


Figure 11. GPIO Timing

2.13 Reset Timing

Table 22. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

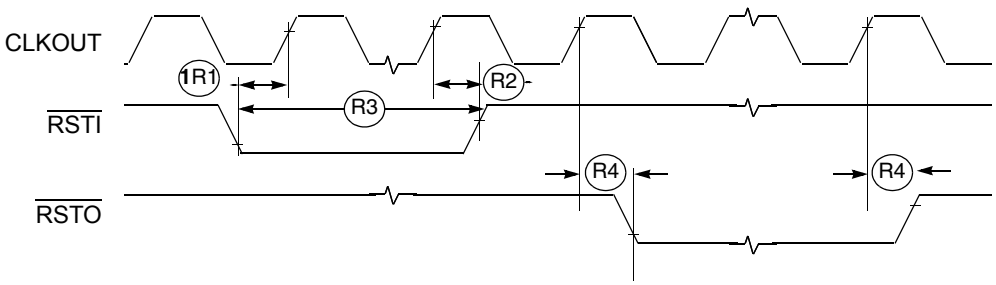


Figure 12. $\overline{RSTI}$ and Configuration Override Timing

Table 25. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

1 All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3 V, V_{REFH} = 3.3 V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

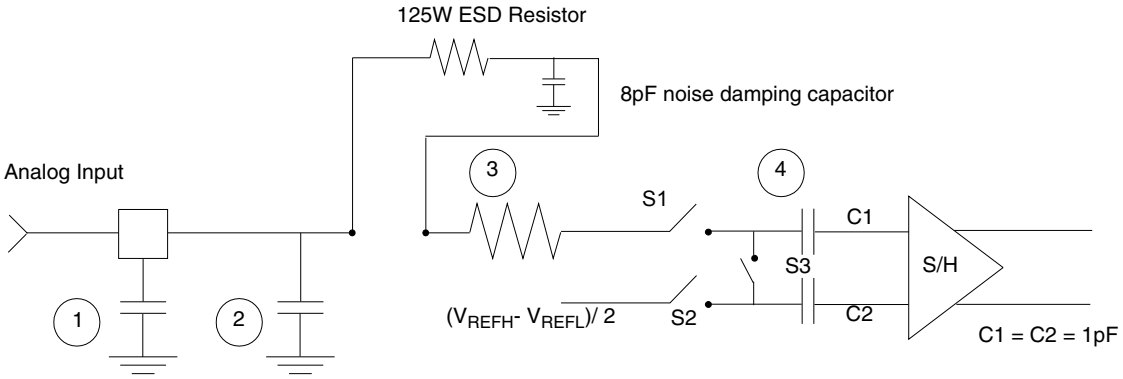
5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

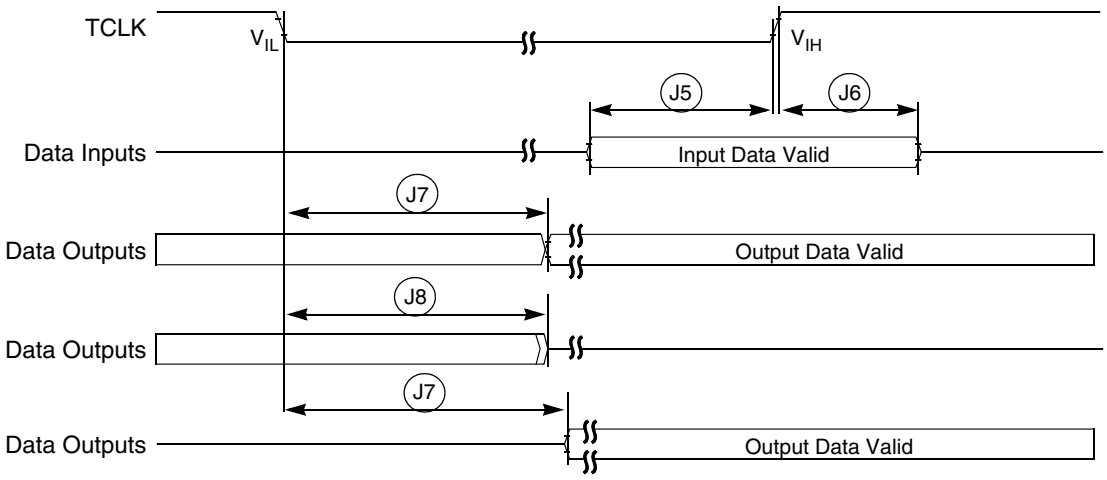


Figure 17. Boundary Scan (JTAG) Timing

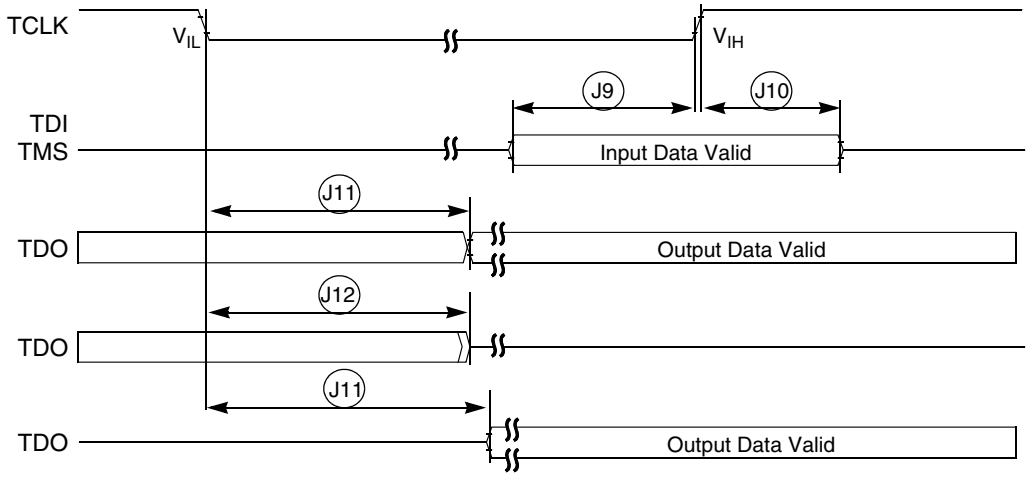


Figure 18. Test Access Port Timing

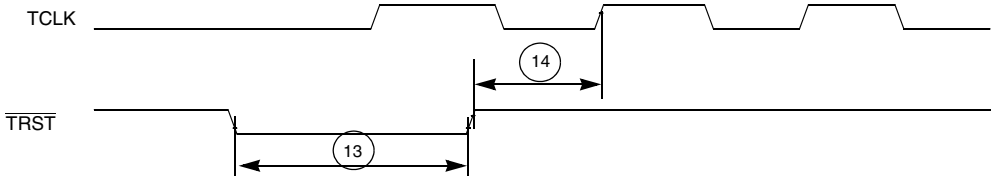


Figure 19. $\overline{TRST}$ Timing

2.20 Debug AC Timing Specifications

Table 29 lists specifications for the debug AC timing parameters shown in Figure 21.

Table 29. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4[1]	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{\text{BKPT}}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0.0	10.0	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 20 shows real-time trace timing for the values in Table 29.

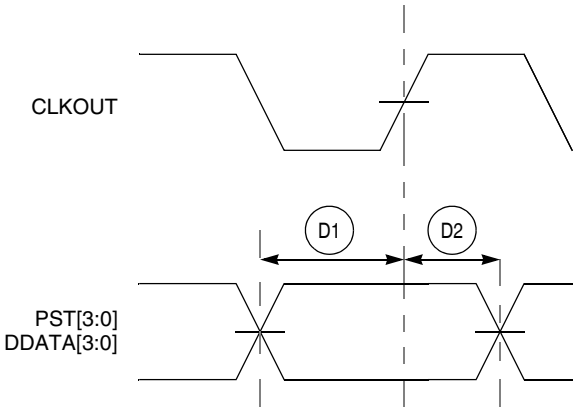


Figure 20. Real-Time Trace AC Timing

4 Revision History

Table 31. Revision History

Revision	Description
0	Initial public release.
1	• Added package dimensions to package diagrams • Added listing of devices for MCF52259 family • Changed “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation” to “Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), pulse-code modulation (PCM), and pulse accumulation” • Updated the figure **Pinout Top View (144 MAPBGA)** • Removed an extraneous instance of the table **Pin Functions by Primary and Alternate Purpose** • In the table **Pin Functions by Primary and Alternate Purpose**, changed a footnote from “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC” to “This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL” • In the table **SGFM Flash Program and Erase Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **SGFM Flash Module Life Characteristics**, changed “(V_{DDF} = 2.7 to 3.6 V)“ to “(V_{DD} = 3.0 to 3.6 V)“ • In the table **Oscillator and PLL Specifications**, changed “V_{DD} and V_{DDPLL} = 2.7 to 3.6 V“ to “V_{DD} and V_{DDPLL} = 3.0 to 3.6 V“ • In the table **Reset and Configuration Override Timing**, changed “V_{DD} = 2.7 to 3.6 V“ to “V_{DD} = 3.0 to 3.6 V“
2	• Added EzPort Electrical Specifications. • Updated Table 2 for part numbers. • In Table 13, added slew rate column, updated derive strength, pull-up/pull-down values,JTAG pin alternate functions, removed Wired/OR control column, and reordered AN[7:0] list of pin numbers for 144 LQFP and 100 LQFP. • Updated Table 14. • Updated Table 13, to change MIN voltage spec for Standby Voltage (VSTBY) to 1.8V (from 3.0V). • Updated Figure 2 for RTC_EXTAL and RTC_XTAL pin positions.
3	• Updated EzPort Electrical Specifications • Added hysteresis note in the DC electrical table • Clarified pin function table for VSS pins. • Clarified orderable part summary.
4	• Updated EXTAL input high voltage (External reference) Maximum to "3.0V" (Instead of "VDD"). Also, added a footnote saying, “This value has been update” • Updated crystal frequency value to 25 MHz
5	• Updated TOC