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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, Ethernet, I²C, QSPI, UART/USART, USB OTG
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf52254caf66

Table of Contents

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

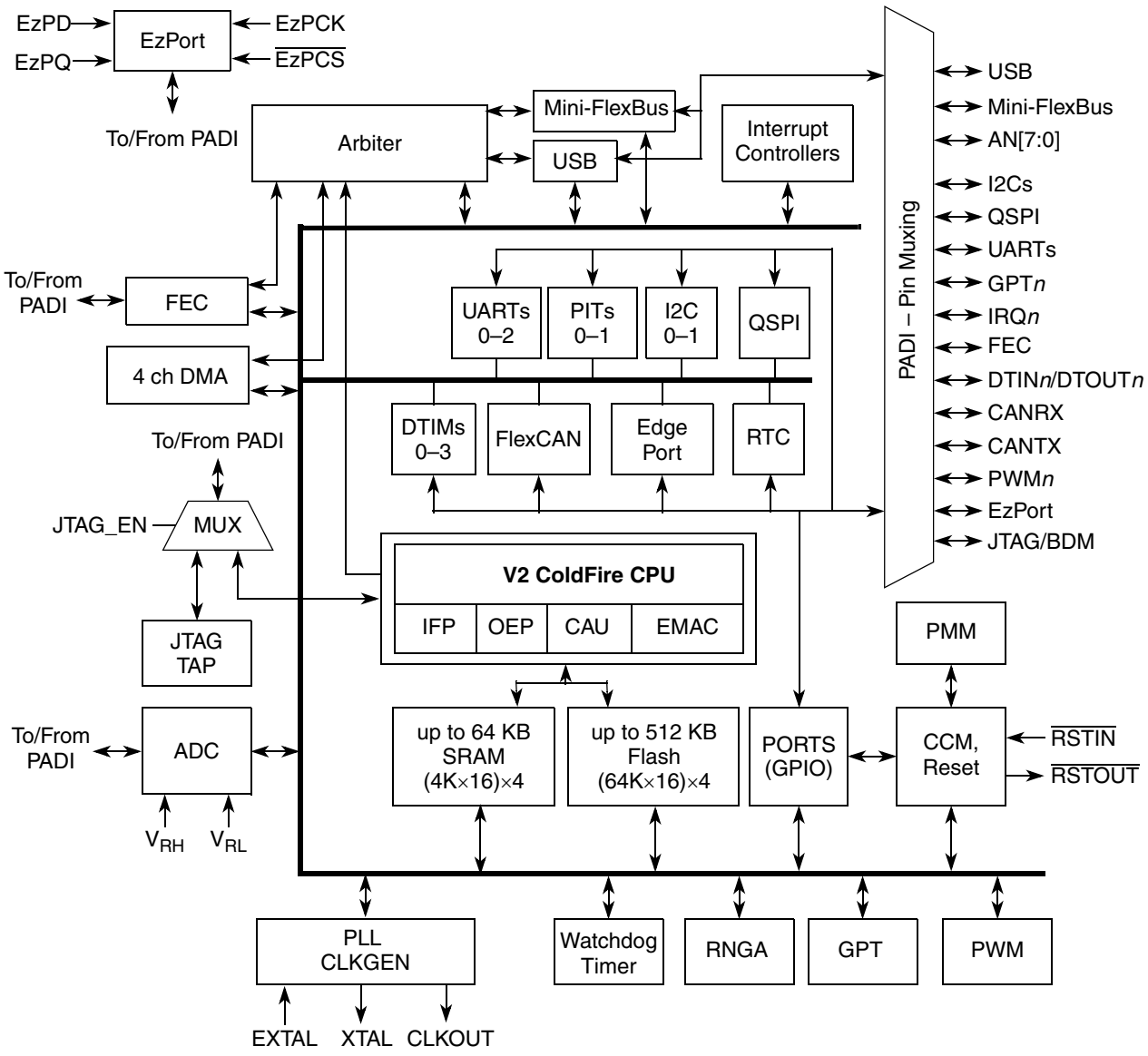

Figure 1. MCF52259 Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52259 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip

  - Up to 80 MHz processor core frequency
  - 40 MHz or 33 MHz peripheral bus frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Enhanced Multiply-Accumulate (EMAC) unit with four 32-bit accumulators to support 16×16 → 32 or 32×32 → 48 operations
  - Cryptographic Acceleration Unit (CAU)
    - Tightly-coupled coprocessor to accelerate software-based encryption and message digest functions
    - Support for DES, 3DES, AES, MD5, and SHA-1 algorithms
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - Up to 64 KB dual-ported SRAM on CPU internal bus, supporting core, DMA, and USB access with standby power supply support for the first 16 KB
  - Up to 512 KB of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used (except backup watchdog timer)
  - Software controlled disable of external clock output for low-power consumption
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/s
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0–13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
  - Full-speed / low-speed host controller
  - USB 1.1 and 2.0 compliant full-speed / low speed device controller
  - 16 bidirectional end points

  - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
  - 12.5 ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse-widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Support for PCM mode (resulting in superior signal quality compared to conventional PWM)
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Real-Time Clock (RTC)
  - Maintains system time-of-day clock
  - Provides stopwatch and alarm interrupt functions
  - Standby power supply (Vstby) keeps the RTC running when the system is shut down
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Backup watchdog timer (BWT)
  - Independent timer that can be used to help software recover from runaway code
  - 16-bit counter
  - Low-power mode support
- Clock generation features
  - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator

  - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($0 \le n \le 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle-steal support
  - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
  - Channel linking support
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock / loss of lock
    - Low-voltage detection (LVD)
    - JTAG
  - Status flag indication of source of last reset
- Chip configuration module (CCM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O on 100-pin package
  - Up to 96 bits of general purpose I/O on 144-pin package
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.21 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.22 Backup Watchdog Timer

The backup watchdog timer is an independent 16-bit timer that, like the software watchdog timer, facilitates recovery from runaway code. This timer is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown. The backup watchdog timer can be clocked by either the relaxation oscillator or the system clock.

1.2.23 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.24 Interrupt Controllers (INTC*n*)

The device has two interrupt controllers that supports up to 128 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.25 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCR*n*[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.26 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock / loss of clock
- Software
- Low-voltage detector (LVD)
- JTAG

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

Figure 2 shows the pinout configuration for the 144 LQFP.

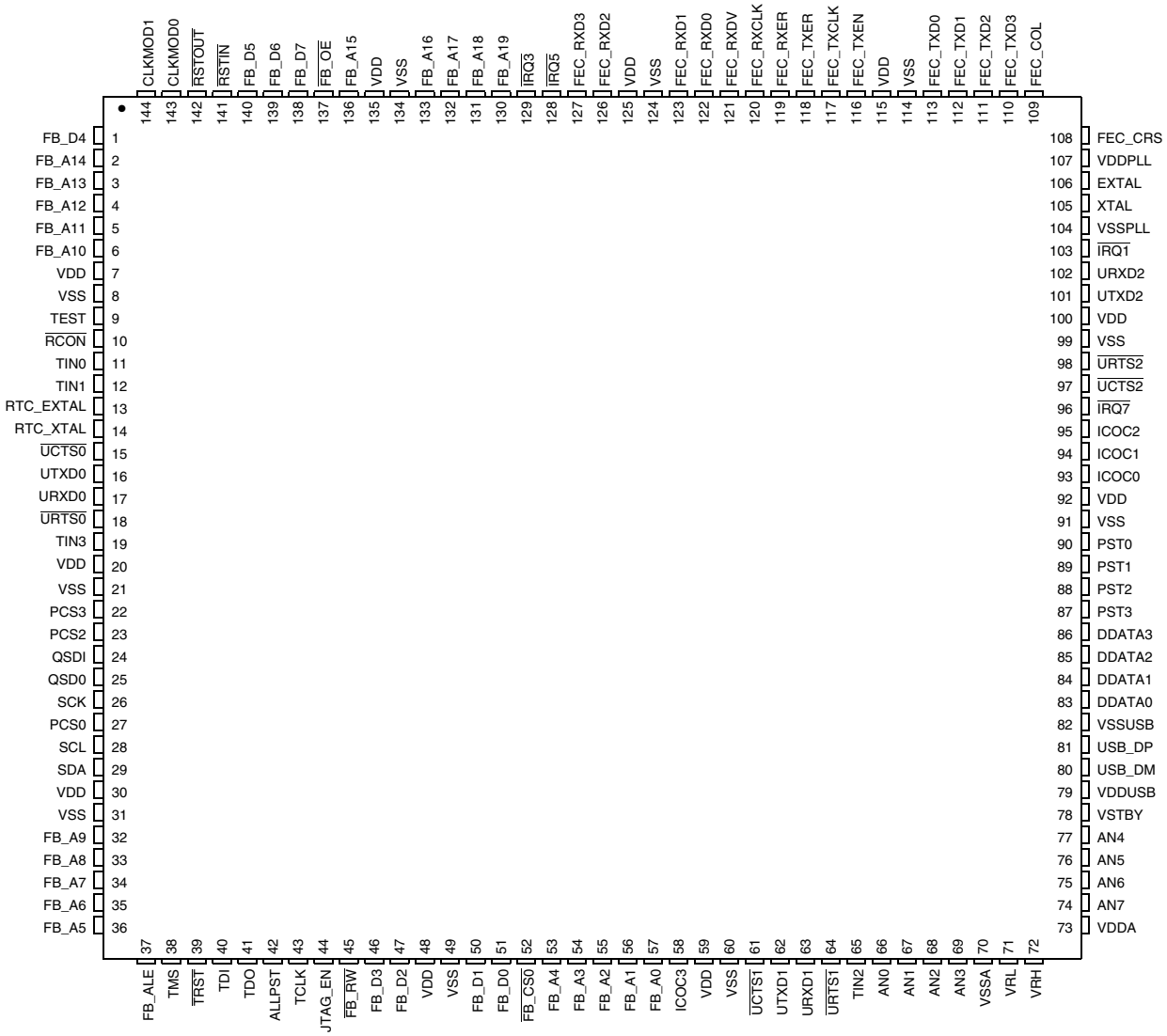

Figure 2. 144 LQFP Pin Assignment

Figure 3 shows the pinout configuration for the 100 LQFP.

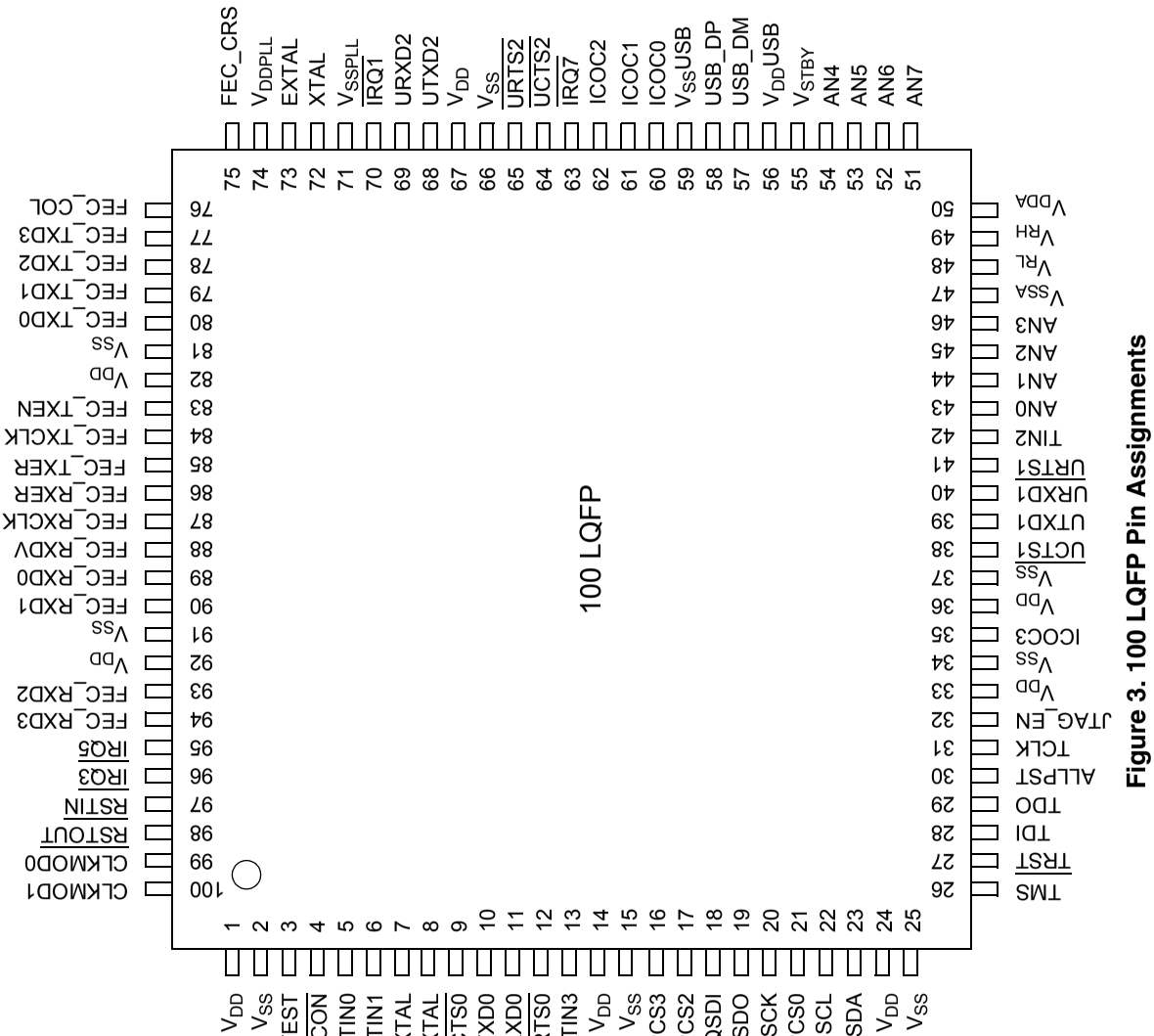

Figure 3. 100 LQFP Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
Mode Selection	$\overline{\text{RCON}}$/$\overline{\text{EZPCS}}$	—	—	—	N/A	N/A	Pull-Up	E4	10	4
	CLKMOD[1:0]	—	—	—	N/A	N/A	Pull-Down	D4, D5	144, 143	100, 99
QSPI	QSPI_CS3	SYNCA	USB_DP_PDOWN	PQS6	PSRR[7]	PDSR[7]	—	G4	22	16
	QSPI_CS2	SYNCB	USB_DM_PDOWN	PQS5	PSRR[6]	PDSR[6]	—	G3	23	17
	QSPI_CS0	I2C_SDA0	UCTS1	PQS3	PSRR[4]	PDSR[4]	Pull-Up[6]	H4	27	21
	QSPI_CLK/ EZPCK	I2C_SCL0	URTS1	PQS2	PSRR[3]	PDSR[3]	Pull-Up[6]	H3	26	20
QSPI	QSPI_DIN/ EZPD	I2C_SDA1	URXD1	PQS1	PSRR[2]	PDSR[2]	Pull-Up[6]	G2	24	18
	QSPI_DOUT/EZPQ	I2C_SCL1	UTXD1	PQS0	PSRR[1]	PDSR[1]	Pull-Up[6]	G1	25	19
Reset[7]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	Pull-Up[7]	A3	141	97
	$\overline{\text{RSTO}}$	—	—	—	Low	High	—	A2	142	98
Test	TEST	—	—	—	N/A	N/A	Pull-Down	B1	9	3
Timer 3, 16-bit	GPT3	—	PWM7	PTA3	PSRR[23]	PDSR[23]	Pull-Up[8]	M7	58	35
Timer 2, 16-bit	GPT2	—	PWM5	PTA2	PSRR[22]	PDSR[22]	Pull-Up[8]	J10	95	62
Timer 1, 16-bit	GPT1	—	PWM3	PTA1	PSRR[21]	PDSR[21]	Pull-Up[8]	J11	94	61
Timer 0, 16-bit	GPT0	—	PWM1	PTA0	PSRR[20]	PDSR[20]	Pull-Up[8]	F12	93	60
Timer 3, 32-bit	DTIN3	DTOUT3	PWM6	PTC3	PSRR[19]	PDSR[19]	—	F4	19	13
Timer 2, 32-bit	DTIN2	DTOUT2	PWM4	PTC2	PSRR[18]	PDSR[18]	—	J8	65	42

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function (Alt 1)	Tertiary Function (Alt 2)	Quaternary Function (GPIO)	Slew Rate	Drive Strength/Control[1]	Pull-up/ Pull-down[2]	Pin on 144 MAPBGA	Pin on 144 LQFP	Pin on 100 LQFP
VSS	VSS	—	—	—	N/A	N/A	—	A1; A12; F6–8; G6–8; H8; M1	8; 21; 31; 49; 60; 91; 99; 114; 124; 134	2; 15; 25; 34; 37; 66; 81; 91

1 The PDSR and PSSR registers are part of the GPIO module. All programmable signals default to 2mA drive in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 I2C1 is multiplexed with specific pins of the QSPI, UART1, UART2, and Mini-FlexBus pin groups.
4 For primary and GPIO functions only.
5 Only when JTAG mode is enabled.
6 For secondary and GPIO functions only.
7 RSTI has an internal pull-up resistor; however, the use of an external resistor is strongly recommended.
8 For GPIO functions, the Primary Function has pull-up control within the GPT module.
9 Available on 144-pin packages only.
10 This list for power and ground does not include those dedicated power/ground pins included elsewhere, such as in the ADC, USB, and PLL.

Table 8. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[13,14]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,15]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board	—	θ_{JB}	25[16]	°C/W
	Junction to case	—	θ_{JC}	9[17]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[18]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

7 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

8 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

9 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

10 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

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14 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

15 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

[16] Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[17] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

[18] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, W

$P_{I/O}$ = power dissipation on input and output pins — user determined, W

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 9 and Table 10.

Table 9. SGFM Flash Program and Erase Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

1 Depending on packaging; see the orderable part number summary (Table 2).

2 Refer to the flash memory section for more information (Section 2.4, “Flash Memory Characteristics”)

Table 10. SGFM Flash Module Life Characteristics

(V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2.7 DC Electrical Specifications

Table 13. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.5	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis[2]	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS}, digital pins	I_{in}	–1.0	1.0	μA
Output high voltage (all input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) I_{OL} = 2.0 mA	V_{OL}	—	0.5	V
Output high voltage (high drive) I_{OH} = -5 mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) I_{OL} = 5 mA	V_{OL}	—	0.5	V
Output high voltage (low drive) I_{OH} = -2 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) I_{OL} = 2 mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[3]	I_{APU}	–10	–130	μA
Input Capacitance [4] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to Table 14 for additional PLL specifications.

2 Only for pins: IRQ1, IRQ3. IRQ5, IRQ7, RSTIN_B, TEST, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

3 Refer to Table 3 for pins having internal pull-up devices.

4 This parameter is characterized before qualification rather than 100% tested.

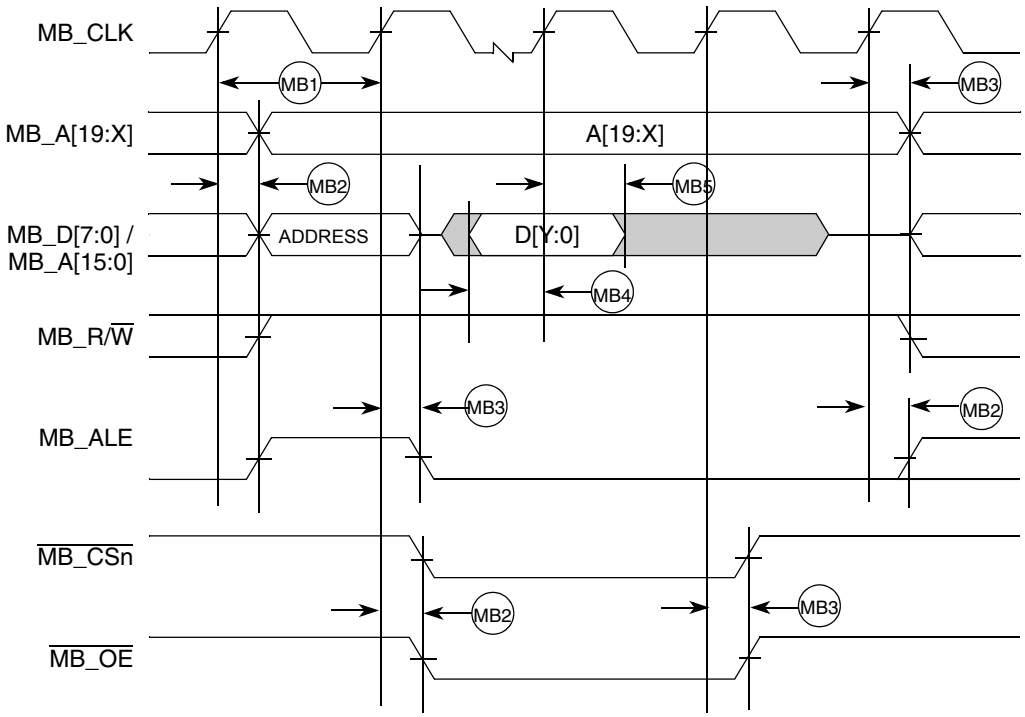


Figure 5. Mini-FlexBus Read Timing

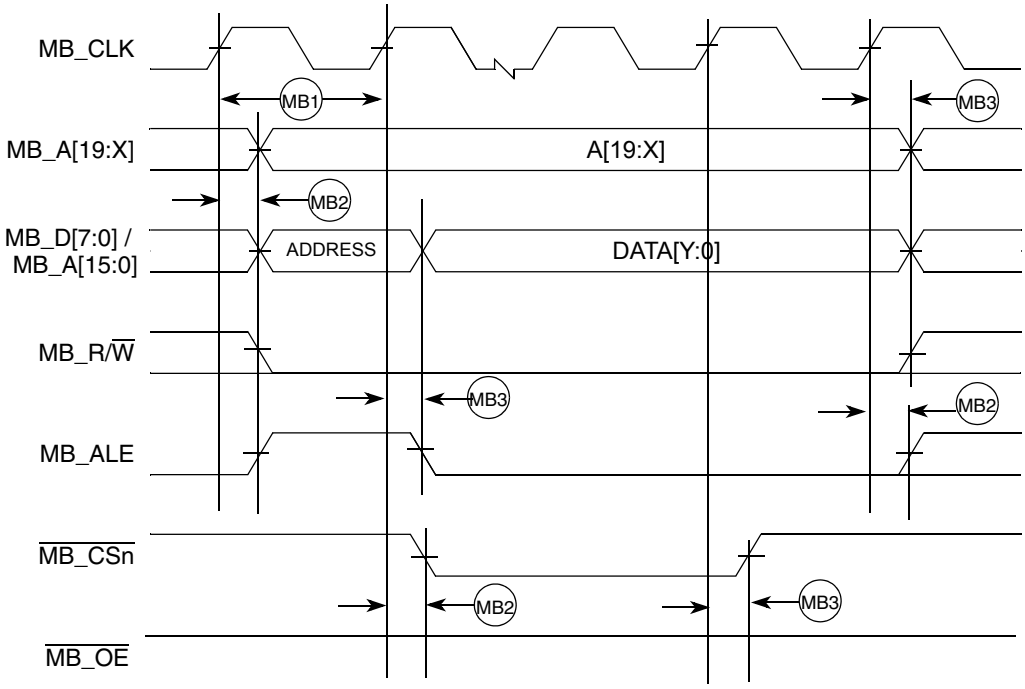


Figure 6. Mini-FlexBus Write Timing

2.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

- 25 pF / 25 Ω for low drive

Table 21. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

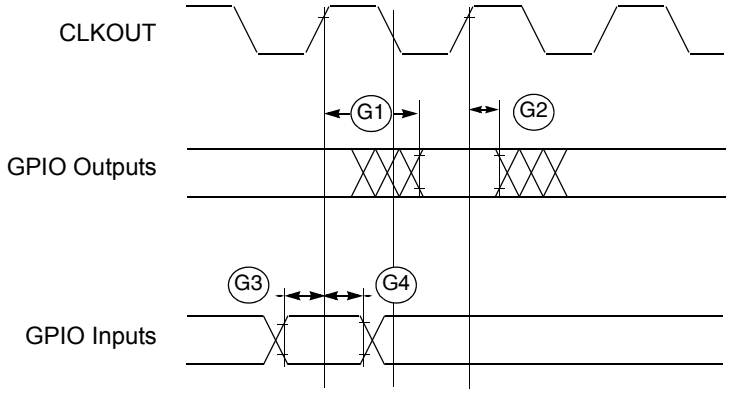


Figure 11. GPIO Timing

2.13 Reset Timing

Table 22. Reset and Configuration Override Timing

(V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

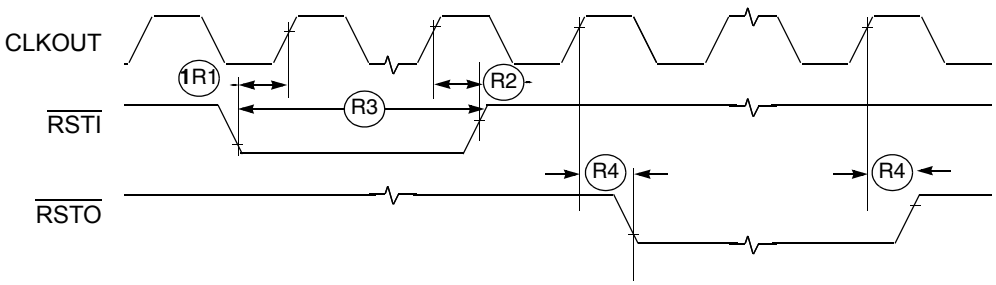


Figure 12. $\overline{RSTI}$ and Configuration Override Timing

2.14 I2C Input/Output Timing Specifications

Table 23 lists specifications for the I2C input timing parameters shown in Figure 13.

Table 23. I2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 24 lists specifications for the I2C output timing parameters shown in Figure 13.

Table 24. I2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

2 Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50 pF load.

Figure 13 shows timing for the values in Table 23 and Table 24.

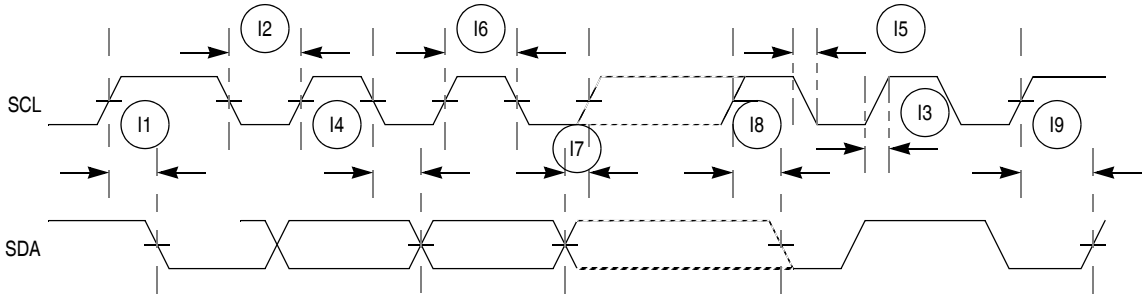


Figure 13. I2C Input/Output Timings

2.15 Analog-to-Digital Converter (ADC) Parameters

Table 25 lists specifications for the analog-to-digital converter.

Table 25. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SSA}	—	V_{SSA} + 50 mV	V
V_{REFH}	High reference voltage	V_{DDA} - 50 mV	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.1	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 14	—	pF
X_{IN}	Input impedance	—	See Figure 14	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV

Table 25. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

1 All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3 V, V_{REFH} = 3.3 V, and V_{REFL} = ground

2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

3 LSB = Least Significant Bit

4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

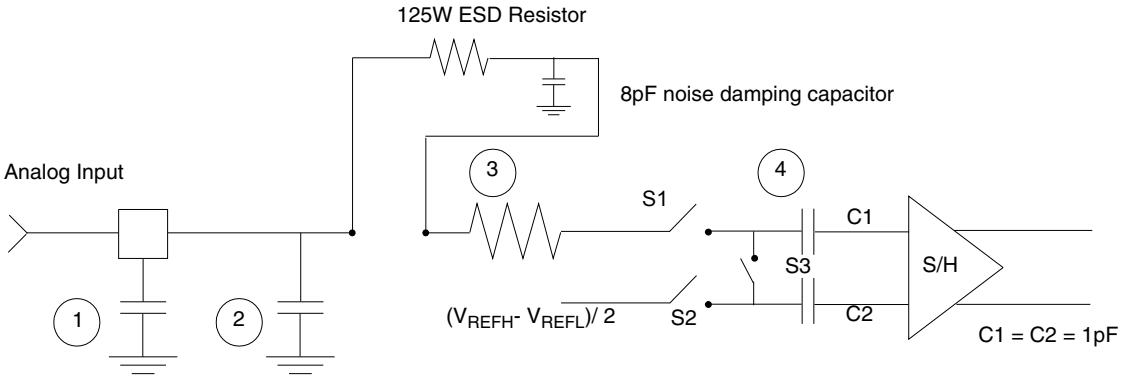
5 Includes power-up of ADC and V_{REF}

6 ADC clock cycles

7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.16 Equivalent Circuit for ADC Inputs

Figure 14 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed and S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8 pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04 pF
3. Equivalent resistance for the channel select mux; 100 Ω
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4 pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

Figure 14. Equivalent Circuit for A/D Loading

2.17 DMA Timers Timing Specifications

Table 26 lists timer module AC timings.

Table 26. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

1 All timing references to CLKOUT are given to its rising edge.

2.18 QSPI Electrical Specifications

Table 27 lists QSPI timings.

Table 27. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 27 correspond to Figure 15.

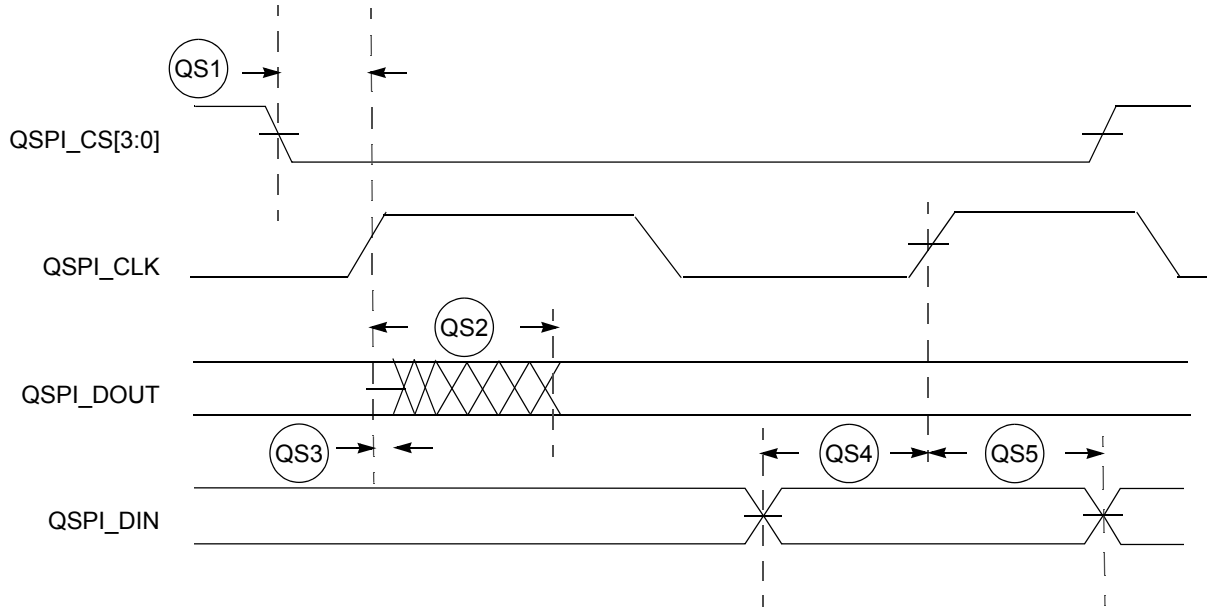


Figure 15. QSPI Timing

2.19 JTAG and Boundary Scan Timing

Figure 21 shows BDM serial port AC timing for the values in Table 29.

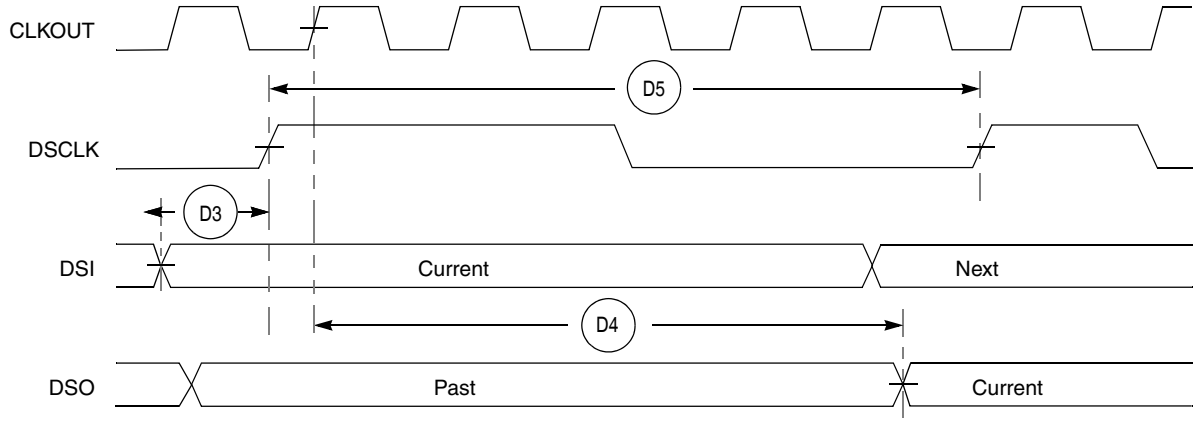


Figure 21. BDM Serial Port AC Timing

3 Package Information

The latest package outline drawings are available on the product summary pages on http://www.freescale.com/coldfire. Table 30 lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 30. Package Information

Device	Package Type	Case Outline Numbers
MCF52252	100 LQFP	98ASS23308W
MCF52254		
MCF52255		
MCF52256	144 LQFP or 144 MAPBGA	98ASS23177W 98ASH70694A
MCF52258		
MCF52259		