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Details

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Product Status	Obsolete
Core Processor	dsPIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	69
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33fj64gp708t-i-pt

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	Pin Type	Buffer Type	Description
AN0-AN31	I	Analog	Analog input channels.
AVDD	Р	Р	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	Ground reference for analog modules.
CLKI CLKO	I O	ST/CMOS —	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
COFS CSCK CSDI CSDO	I/O I/O I O	ST ST ST —	Data Converter Interface frame synchronization pin. Data Converter Interface serial clock input/output pin. Data Converter Interface serial data input pin. Data Converter Interface serial data output pin.
C1RX C1TX C2RX C2TX	 0 0	ST — ST —	ECAN1 bus receive pin. ECAN1 bus transmit pin. ECAN2 bus receive pin. ECAN2 bus transmit pin.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	Data I/O pin for programming/debugging communication channel 1. Clock input pin for programming/debugging communication channel 1. Data I/O pin for programming/debugging communication channel 2. Clock input pin for programming/debugging communication channel 2. Data I/O pin for programming/debugging communication channel 3. Clock input pin for programming/debugging communication channel 3.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INT0 INT1 INT2 INT3 INT4		ST ST ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2. External interrupt 3. External interrupt 4.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
OCFA OCFB OC1-OC8	 0	ST ST —	Compare Fault A input (for Compare Channels 1, 2, 3 and 4). Compare Fault B input (for Compare Channels 5, 6, 7 and 8). Compare outputs 1 through 8.
OSC1 OSC2	I I/O	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
RA0-RA7 RA9-RA10 RA12-RA15	I/O I/O I/O	ST ST ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC12-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE7	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8 RF12-RF13	I/O I/O	ST ST	PORTF is a bidirectional I/O port.
Legend: CMC	S = CMO	S compatible	e input or output; Analog = Analog input; P = Power

ST = Schmitt Trigger input with CMOS levels;

O = Output; I = Input

3.0 CPU

Note: This data sheet summarizes the features of the dsPIC33FJXXXGPX06/X08/X10 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2. "CPU"** (DS70204) in the *"dsPIC33F Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJXXXGPX06/X08/X10 CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for DSP. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

The dsPIC33FJXXXGPX06/X08/X10 devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The dsPIC33FJXXXGPX06/X08/X10 instruction set has two classes of instructions: MCU and DSP. These two instruction classes are seamlessly integrated into a single CPU. The instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the dsPIC33FJXXXGPX06/X08/X10 is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1. The programmer's model for the dsPIC33FJXXXGPX06/X08/X10 is shown in Figure 3-2.

3.1 Data Addressing Overview

The data space can be addressed as 32K words or 64 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear data space. Certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y data space boundary is device-specific.

Overhead-free circular buffers (Modulo Addressing mode) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. Furthermore, the X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space. The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

3.2 DSP Engine Overview

The DSP engine features a high-speed, 17-bit by 17-bit multiplier, a 40-bit ALU, two 40-bit saturating accumulators and a 40-bit bidirectional barrel shifter. The barrel shifter is capable of shifting a 40-bit value, up to 16 bits right or left, in a single cycle. The DSP instructions operate seamlessly with all other instructions and have been designed for optimal real-time performance. The MAC instruction and other associated instructions can concurrently fetch two data operands from memory while multiplying two W registers and accumulating and optionally saturating the result in the same cycle. This instruction functionality requires that the RAM memory data space be split for these instructions and linear for all others. Data space partitioning is achieved in a transparent and flexible manner through dedicating certain working registers to each address space.

3.3 Special MCU Features

The dsPIC33FJXXXGPX06/X08/X10 features a 17-bit by 17-bit, single-cycle multiplier that is shared by both the MCU ALU and DSP engine. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication not only allows you to perform mixed-sign multiplication, it also achieves accurate results for special operations, such as (-1.0) x (-1.0).

The dsPIC33FJXXXGPX06/X08/X10 supports 16/16 and 32/16 divide operations, both fractional and integer. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A 40-bit barrel shifter is used to perform up to a 16-bit, left or right shift in a single cycle. The barrel shifter can be used by both MCU and DSP instructions.

TABLE 4-15: ADC1 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300								ADC Data	Buffer 0								xxxx
AD1CON1	0320	ADON	_	ADSIDL	ADDMABM	_	AD12B	FOR	M<1:0>		SSRC<2:0>	>	_	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	,	VCFG<2:0	>	—	—	CSCNA	CHP	S<1:0>	BUFS	—		SMPI	<3:0>		BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—		S	AMC<4:0>						ADCS	6<7:0>				0000
AD1CHS123	0326	—	—	_	-	—	CH123N	VB<1:0>	CH123SB	—	-	_	—	—	CH123N	VA<1:0>	CH123SA	0000
AD1CHS0	0328	CH0NB	_	_		С	H0SB<4:0	>		CH0NA	_	_		(CH0SA<4:0)>		0000
AD1PCFGH ⁽¹⁾	032A	PCFG31	PCFG30	PCFG29	PCFG28	PCFG27	PCFG26	PCFG25	PCFG24	PCFG23	PCFG22	PCFG21	PCFG20	PCFG19	PCFG18	PCFG17	PCFG16	0000
AD1PCFGL	032C	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
AD1CSSH ⁽¹⁾	032E	CSS31	CSS30	CSS29	CSS28	CSS27	CSS26	CSS25	CSS24	CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16	0000
AD1CSSL	0330	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD1CON4	0332	_	_	_	_	_	_	_	_	_	_	_	_	_	I	DMABL<2:)>	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Not all ANx inputs are available on all devices. See the device pin diagrams for available ANx inputs.

TABLE 4-16: ADC2 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC2BUF0	0340								ADC Data	Buffer 0								xxxx
AD2CON1	0360	ADON	_	ADSIDL	ADDMABM	_	AD12B	FOR	M<1:0>		SSRC<2:0	>	_	SIMSAM	ASAM	SAMP	DONE	0000
AD2CON2	0362		VCFG<2:0	>	_	_	CSCNA	CHP	S<1:0>	BUFS	_		SMPI	<3:0>		BUFM	ALTS	0000
AD2CON3	0364	ADRC	_	_		S	AMC<4:0>						ADC	S<7:0>				0000
AD2CHS123	0366	_	_	_	_	_	CH123N	VB<1:0>	CH123SB	_	_	_	_	_	CH1231	NA<1:0>	CH123SA	0000
AD2CHS0	0368	CH0NB	_	_	_		CH0S	B<3:0>		CH0NA	_	_	_		CH05	SA<3:0>		0000
Reserved	036A	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
AD2PCFGL	036C	PCFG15	PCFG14	PCFG13	PCFG12	PCFG11	PCFG10	PCFG9	PCFG8	PCFG7	PCFG6	PCFG5	PCFG4	PCFG3	PCFG2	PCFG1	PCFG0	0000
Reserved	036E	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
AD2CSSL	0370	CSS15	CSS14	CSS13	CSS12	CSS11	CSS10	CSS9	CSS8	CSS7	CSS6	CSS5	CSS4	CSS3	CSS2	CSS1	CSS0	0000
AD2CON4	0372	_	_	_	_	_	_	_	_	_	_	_	_	_		DMABL<2	:0>	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: DCI REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
DCICON1	0280	DCIEN	—	DCISIDL	—	DLOOP	CSCKD	CSCKE	COFSD	UNFM	CSDOM	DJST	_	_	—	COFSM1	COFSM0	0000 0000 0000 0000
DCICON2	0282	_	_	_	_	BLEN1	BLEN0	_		COFS	G<3:0>				V	VS<3:0>		0000 0000 0000 0000
DCICON3	0284	—	—	_	—						BCG<11	1:0>						0000 0000 0000 0000
DCISTAT	0286	—	—	_	—	SLOT3	SLOT2	SLOT1	SLOT0	-	—	—		ROV	RFUL	TUNF	TMPTY	0000 0000 0000 0000
TSCON	0288	TSE15	TSE14	TSE13	TSE12	TSE11	TSE10	TSE9	TSE8	TSE7	TSE6	TSE5	TSE4	TSE3	TSE2	TSE1	TSE0	0000 0000 0000 0000
RSCON	028C	RSE15	RSE14	RSE13	RSE12	RSE11	RSE10	RSE9	RSE8	RSE7	RSE6	RSE5	RSE4	RSE3	RSE2	RSE1	RSE0	0000 0000 0000 0000
RXBUF0	0290							Receive B	Buffer #0 D	ata Regi	ster							0000 0000 0000 0000
RXBUF1	0292							Receive B	Buffer #1 D	ata Regi	ster							0000 0000 0000 0000
RXBUF2	0294							Receive B	Buffer #2 D	ata Regi	ster							0000 0000 0000 0000
RXBUF3	0296							Receive B	Buffer #3 D	ata Regi	ster							0000 0000 0000 0000
TXBUF0	0298							Transmit I	Buffer #0 D	ata Regi	ster							0000 0000 0000 0000
TXBUF1	029A							Transmit I	Buffer #1 D	ata Regi	ster							0000 0000 0000 0000
TXBUF2	029C							Transmit I	Buffer #2 D	ata Regi	ster							0000 0000 0000 0000
TXBUF3	029E							Transmit I	Buffer #3 D	ata Regi	ster							0000 0000 0000 0000

 Legend:
 — = unimplemented, read as '0'.

 Note
 1:
 Refer to the "dsPIC33F Family Reference Manual" for descriptions of register bit fields.

TABLE 4-25: PORTA REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	TRISA15	TRISA14	TRISA13	TRISA12	-	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	F6FF
PORTA	02C2	RA15	RA14	RA13	RA12	_	RA10	RA9	_	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	XXXX
LATA	02C4	LATA15	LATA14	LATA13	LATA12	_	LATA10	LATA9	_	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	XXXX
ODCA ⁽²⁾	06C0	ODCA15	ODCA14	_	_	_	_	_	_	_	_	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices. Legend:

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

TABLE 4-26: PORTB REGISTER MAP⁽¹⁾

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C6	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02C8	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CA	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

- bit 3 CNIF: Input Change Notification Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 2 Unimplemented: Read as '0'
- bit 1 MI2C1IF: I2C1 Master Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred
- bit 0 SI2C1IF: I2C1 Slave Events Interrupt Flag Status bit
 - 1 = Interrupt request has occurred
 - 0 = Interrupt request has not occurred

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1 (CONTINUED)

- bit 3 CNIE: Input Change Notification Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled
- bit 2 Unimplemented: Read as '0'
- bit 1 MI2C1IE: I2C1 Master Events Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled
- bit 0 SI2C1IE: I2C1 Slave Events Interrupt Enable bit
 - 1 = Interrupt request enabled
 - 0 = Interrupt request not enabled

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		T8IP<2:0>				MI2C2IP<2:0>	
bit 15							bit 8
	D 444	DAMO	DAMA			DAVA	DAM 0
U-0	R/W-1	R/W-0	R/W-0	0-0	R/W-1	R/W-0	R/W-0
— bit 7		312021F<2.02		_		1716~2.02	bit 0
							bit 0
Legend:							
R = Readable I	oit	W = Writable b	oit	U = Unimple	mented bit, rea	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	own
bit 15	Unimpleme	ented: Read as 'o)'				
bit 14-12	T8IP<2:0>:	Timer8 Interrupt	Priority bits				
	111 = Interr	rupt is priority 7 (h	highest priori	ity interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
L # 44		rupt source is disa	abled				
DIT 11	Unimpleme	ented: Read as 10					
DIT 10-8	MI2C2IP<2	:U>: 12C2 Master	Events Inter	rrupt Priority bit	S		
	•	upt is priority 7 (i	lighest phon	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is priority 1	ahlad				
hit 7		apt source is use	, ,				
bit 6-4	SI2C2IP<2.	ns: 12C2 Slave E	vents Interri	int Priority hits			
bit 0-4	111 = Interr	upt is priority 7 (h	nighest priori	ity interrupt)			
	•	aptie prierity : (i	g. eet p. ee				
	•						
	•	runt is priority 1					
	001 = Interior	upt is priority i upt source is disa	abled				
bit 3	Unimpleme	ented: Read as 'o)'				
bit 2-0	T7IP<2:0>:	Timer7 Interrupt	Priority bits				
	111 = Interr	rupt is priority 7 (h	nighest priori	ity interrupt)			
	•						
	•						
	001 = Interr	rupt is prioritv 1					
	000 = Interr	upt source is disa	abled				

8.0 DIRECT MEMORY ACCESS (DMA)

Note: This data sheet summarizes the features of the dsPIC33FJXXXGPX06/X08/X10 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 22. "Direct Memory Access (DMA)" (DS70182) in the "dsPIC33F Family Reference Manual", which is available the Microchip from web site (www.microchip.com).

Direct Memory Access (DMA) is a very efficient mechanism of copying data between peripheral SFRs (e.g., UART Receive register, Input Capture 1 buffer), and buffers or variables stored in RAM, with minimal CPU intervention. The DMA controller can automatically copy entire blocks of data without requiring the user software to read or write the peripheral Special Function Registers (SFRs) every time a peripheral interrupt occurs. The DMA controller uses a dedicated bus for data transfers and therefore, does not steal cycles from the code execution flow of the CPU. To exploit the DMA capability, the corresponding user buffers or variables must be located in DMA RAM.

The dsPIC33FJXXXGPX06/X08/X10 peripherals that can utilize DMA are listed in Table 8-1 along with their associated Interrupt Request (IRQ) numbers.

TABLE 8-1: PERIPHERALS WITH DMA SUPPORT

Peripheral	IRQ Number
INTO	0
Input Capture 1	1
Input Capture 2	5
Output Compare 1	2
Output Compare 2	6
Timer2	7
Timer3	8
SPI1	10
SPI2	33
UART1 Reception	11
UART1 Transmission	12
UART2 Reception	30
UART2 Transmission	31
ADC1	13
ADC2	21
DCI	60
ECAN1 Reception	34
ECAN1 Transmission	70
ECAN2 Reception	55
ECAN2 Transmission	71

The DMA controller features eight identical data transfer channels.

Each channel has its own set of control and status registers. Each DMA channel can be configured to copy data either from buffers stored in dual port DMA RAM to peripheral SFRs, or from peripheral SFRs to buffers in DMA RAM.

The DMA controller supports the following features:

- · Word or byte sized data transfers.
- Transfers from peripheral to DMA RAM or DMA RAM to peripheral.
- Indirect Addressing of DMA RAM locations with or without automatic post-increment.
- Peripheral Indirect Addressing In some peripherals, the DMA RAM read/write addresses may be partially derived from the peripheral.
- One-Shot Block Transfers Terminating DMA transfer after one block transfer.
- Continuous Block Transfers Reloading DMA RAM buffer start address after every block transfer is complete.
- Ping-Pong Mode Switching between two DMA RAM start addresses between successive block transfers, thereby filling two buffers alternately.
- Automatic or manual initiation of block transfers
- Each channel can select from 20 possible sources of data sources or destinations.

For each DMA channel, a DMA interrupt request is generated when a block transfer is complete. Alternatively, an interrupt can be generated when half of the block has been filled.

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REGISTER 8-	7: DMAC	S0: DMA CO	NTROLLER	STATUS RE	EGISTER 0		
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
PWCOL7	PWCOL6	PWCOL5	PWCOL4	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
XWCOL7	XWCOL6	XWCOL5	XWCOL4	XWCOL3	XWCOL2	XWCOL1	XWCOL0
bit 7							bit 0
Legend:		C = Clear onl	y bit				
R = Readable I	oit	W = Writable	bit		mented bit, read	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
hit 1E		annal 7 Darinh	aral Mrita Cal	liaion Flog hit			
DIL 15	1 = Write colli	sion detected		lision Flag bit			
	0 = No write com	collision detected	ed				
bit 14	PWCOL6: Ch	annel 6 Periph	eral Write Col	lision Flag bit			
	1 = Write colli	sion detected		-			
	0 = No write c	collision detected	ed				
bit 13	PWCOL5: Ch	annel 5 Periph	eral Write Col	lision Flag bit			
	1 = Write colli	sion detected	bd				
hit 12	PWCOL4: Ch	annel 4 Perinh	eral Write Col	lision Flag hit			
511 12	1 = Write colli	sion detected		lision r lag bit			
	0 = No write o	collision detected	ed				
bit 11	PWCOL3: Ch	annel 3 Periph	eral Write Col	lision Flag bit			
	1 = Write colli	sion detected					
	0 = No write c	collision detecte	ed				
bit 10	PWCOL2: Ch	annel 2 Periph	ieral Write Col	lision Flag bit			
	1 = VVrite colli0 = No write c	sion detected	ed				
bit 9	PWCOL1: Ch	annel 1 Periph	eral Write Col	lision Flag bit			
	1 = Write colli	sion detected					
	0 = No write o	collision detected	ed				
bit 8	PWCOL0: Ch	annel 0 Periph	eral Write Col	lision Flag bit			
	1 = Write colli	sion detected	od.				
hit 7		annel 7 DMA I	SAM Write Co	llision Flag hit			
	1 = Write colli	sion detected		ilision riag bit			
	0 = No write c	collision detected	ed				
bit 6	XWCOL6: Ch	annel 6 DMA I	RAM Write Co	llision Flag bit			
	1 = Write colli	sion detected					
	0 = No write c	collision detecte	ed				
bit 5	XWCOL5: Ch	annel 5 DMA I	RAM Write Co	llision Flag bit			
	\perp = vvrite colli 0 = No write c	sion detected	ed				
bit 4	XWCOI 4: Ch	annel 4 DMA I	 RAM Write Co	llision Flag bit			
	1 = Write colli	sion detected					
	0 = No write o	collision detected	ed				

REGISTER 9-	1: OSCC	ON: OSCILL	ATOR CON	TROL REGIS	STER ⁽¹⁾		
U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
		COSC<2:0>				NOSC<2:0> ⁽²⁾	
bit 15							bit 8
D/M/ O	11.0	P 0	11.0		11.0	D/M/ O	
	0-0		0-0		0-0		
bit 7	_	LUCK		UF		LFUSCEN	bit 0
Legend:		y = Value set	from Configur	ation bits on P	OR		
R = Readable b	pit	W = Writable	oit	U = Unimpler	mented bit, re	ad as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkno	own
bit 15	Unimplemen	ted: Read as ')'				
bit 14-12	COSC<2:0>:	Current Oscilla	tor Selection	bits (read-only)		
	001 = Fast R 010 = Primar 011 = Primar 100 = Second 101 = Low-Pc 110 = Fast R 111 = Fast R	C oscillator (FR y oscillator (XT, y oscillator (XT, dary oscillator (ower RC oscillator C oscillator (FR C oscillator (FR	C) with PLL HS, EC) HS, EC) with SOSC) tor (LPRC) C) with Divid	n PLL e-by-16 e-by-n			
bit 11	Unimplemen	ted: Read as 'd)'				
bit 10-8	NOSC<2:0>: 000 = Fast R 001 = Fast R 010 = Primar 011 = Primar 100 = Second 101 = Low-Pd 110 = Fast R 111 = Fast R	New Oscillator C oscillator (FR C oscillator (FR y oscillator (XT, y oscillator (XT, dary oscillator (ower RC oscillator C oscillator (FR C oscillator (FR	Selection bits C) with PLL HS, EC) HS, EC) with SOSC) tor (LPRC) C) with Divid C) with Divid	ı PLL e-by-16 e-by-n			
bit 7	CLKLOCK: C	Clock Lock Enal	ole bit				
	1 = If (FCKSI If (FCKSI 0 = Clock and	M0 = 1), then c M0 = 0), then c d PLL selection	lock and PLL lock and PLL is are not lock	configurations configurations (ed, configurati	are locked may be mod ions may be r	ified nodified	
bit 6	Unimplemen	ted: Read as 'o)'				
bit 5	LOCK: PLL L	ock Status bit (read-only)				
	1 = Indicates 0 = Indicates	that PLL is in I that PLL is out	ock, or PLL s of lock, start	tart-up timer is -up timer is in p	satisfied progress or P	LL is disabled	
bit 4	Unimplemen	ted: Read as 'o)'				
bit 3	CF: Clock Fai	il Detect bit (rea	ad/clear by ap	plication)			
	1 = FSCM has 0 = FSCM has 1 =	as detected cloo as not detected	ck failure clock failure				
bit 2	Unimplemen	ted: Read as 'o)'				
Note 1: Wri "ds	tes to this reg PIC33F Family	ister require ar / Reference Ma	n unlock sequ Inual" (availal	ience. Refer to ble from the Mi	o Section 7. crochip webs	" Oscillator" (DS7 ite) for details.	70186) in the

2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.

REGISTER	13-1: TxCO	N (T2CON, T4	ICON, T6C	ON OR T8CC	ON) CONTRO	L REGISTER				
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0			
TON	—	TSIDL		—	_	—	—			
bit 15					•		bit 8			
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0			
_	TGATE	TCKPS	6<1:0>	T32	—	TCS ⁽¹⁾	—			
bit 7							bit 0			
Legend:										
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'					ad as '0'					
-n = Value a	it POR	'1' = Bit is set		'0' = Bit is cl	eared	x = Bit is unkn	iown			
bit 15	TON: Timerx <u>When T32 =</u> 1 = Starts 32- 0 = Stops 32- <u>When T32 =</u> 1 = Starts 16- 0 = Stops 16-	On bit <u>1:</u> -bit Timerx/y -bit Timerx/y 0: -bit Timerx -bit Timerx								
bit 14	Unimplemen	ted: Read as '	0'							
bit 13	TSIDL: Stop	TSIDL: Stop in Idle Mode bit								
	1 = Discontin 0 = Continue	ue module ope module operat	ration when ion in Idle mo	device enters l ode	dle mode					
bit 12-7	Unimplemen	nted: Read as '	0'							
bit 6	TGATE: Time When TCS = This bit is ign When TCS = 1 = Gated tim 0 = Gated tim	erx Gated Time <u>1:</u> ored. <u>0:</u> ne accumulation ne accumulatior	Accumulation n enabled n disabled	on Enable bit						
bit 5-4	TCKPS<1:0> 11 = 1:256 10 = 1:64 01 = 1:8 00 = 1:1	•: Timerx Input	Clock Presca	ale Select bits						
bit 3	T32: 32-bit Ti 1 = Timerx ar 0 = Timerx ar	T32: 32-bit Timer Mode Select bit 1 = Timerx and Timery form a single 32-bit timer 0 = Timerx and Timery act as two 16-bit timers								
bit 2	Unimplemen	nted: Read as '	0'							
bit 1	TCS: Timerx	Clock Source S	Select bit ⁽¹⁾							
	1 = External o 0 = Internal c	clock from pin 1 lock (Fcy)	TxCK (on the	rising edge)						
bit 0	Unimplemen	nted: Read as '	0'							

Note 1: The TxCK pin is not available on all timers. Refer to the "Pin Diagrams" section for the available pins.

REGISTER 18-1: UXMODE: UARTX MODE REGISTER (CONTINUED)

bit 4	URXINV: Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	 BRGH: High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	<pre>PDSEL<1:0>: Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity</pre>
bit 0	STSEL: Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

- **Note 1:** Refer to **Section 17. "UART"** (DS70188) in the *"dsPIC33F Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.
 - 2: This feature is only available for the 16x BRG mode (BRGH = 0).

REGISTER 19-13: CiBUFPNT2: ECAN™ FILTER 4-7 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
F7BP<3:0>				F6BP<3:0>					
bit 15							bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F5BP<3:0>				F4BP<3:0>				
bit 7							bit 0	

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-12	F7BP<3:0>: RX Buffer Written when Filter 7 Hits bits
bit 11-8	F6BP<3:0>: RX Buffer Written when Filter 6 Hits bits
bit 7-4	F5BP<3:0>: RX Buffer Written when Filter 5 Hits bits
bit 3-0	F4BP<3:0>: RX Buffer Written when Filter 4 Hits bits

REGISTER 19-14: CiBUFPNT3: ECAN™ FILTER 8-11 BUFFER POINTER REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F11BP<3:0>				F10BP<3:0>				
bit 15						bit 8		

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F9BP<3:0>				F8BP<3:0>				
bit 7							bit 0	

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 11-8 F10BP<3:0>: RX Buffer Written when Filter 10 Hits bits

bit 7-4 **F9BP<3:0>:** RX Buffer Written when Filter 9 Hits bits

bit 3-0 F8BP<3:0>: RX Buffer Written when Filter 8 Hits bits

NOTES:

21.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note: This data sheet summarizes the features of the dsPIC33FJXXXGPX06/X08/X10 family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 16. "Analog-to-Digital Converter (ADC)" (DS70183) in the "dsPIC33F Family Reference Manual", which is available from the Microchip web site (www.microchip.com).

The dsPIC33FJXXXGPX06/X08/X10 devices have up to 32 ADC input channels. These devices also have up to 2 ADC modules (ADCx, where 'x' = 1 or 2), each with its own set of Special Function Registers.

The AD12B bit (ADxCON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

21.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- · Up to 32 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Four result alignment options (signed/unsigned, fractional/integer)
- · Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only 1 sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the ADC can have up to 32 analog input pins, designated AN0 through AN31. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other

analog input pins. The actual number of analog input pins and external voltage reference input configuration will depend on the specific device. Refer to the device data sheet for further details.

A block diagram of the ADC is shown in Figure 21-1.

21.2 ADC Initialization

The following configuration steps should be performed.

- 1. Configure the ADC module:
 - a) Select port pins as analog inputs (ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - b) Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>)
 - c) Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>)
 - d) Determine how many S/H channels will be used (ADxCON2<9:8> and ADxPCFGH<15:0> or ADxPCFGL<15:0>)
 - e) Select the appropriate sample/conversion sequence (ADxCON1<7:5> and ADxCON3<12:8>)
 - f) Select how conversion results are presented in the buffer (ADxCON1<9:8>)
 - g) Turn on ADC module (ADxCON1<15>)
 - Configure ADC interrupt (if required):
 - a) Clear the ADxIF bit
 - b) Select ADC interrupt priority

21.3 ADC and DMA

2.

If more than one conversion result needs to be buffered before triggering an interrupt, DMA data transfers can be used. Both ADC1 and ADC2 can trigger a DMA data transfer. If ADC1 or ADC2 is selected as the DMA IRQ source, a DMA transfer occurs when the AD1IF or AD2IF bit gets set as a result of an ADC1 or ADC2 sample conversion sequence.

The SMPI<3:0> bits (ADxCON2<5:2>) are used to select how often the DMA RAM buffer pointer is incremented.

The ADDMABM bit (ADxCON1<12>) determines how the conversion results are filled in the DMA RAM buffer area being used for ADC. If this bit is set, DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer. If the ADDMABM bit is cleared, then DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

Base Assembly # of # of Status Flags Instr Assembly Syntax Description Mnemonic Words Cycles Affected # 29 DIV Signed 16/16-bit Integer Divide N,Z,C,OV DIV.S 1 18 Wm,Wn N,Z,C,OV DIV.SD Wm,Wn Signed 32/16-bit Integer Divide 1 18 DIV.U Wm,Wn Unsigned 16/16-bit Integer Divide 1 18 N,Z,C,OV DIV.UD 1 18 N,Z,C,OV Wm,Wn Unsigned 32/16-bit Integer Divide 30 DIVF DIVF Wm,Wn Signed 16/16-bit Fractional Divide 1 18 N,Z,C,OV 2 31 Do code to PC + Expr, lit14 + 1 times 2 DO DO #lit14,Expr None DO Do code to PC + Expr, (Wn) + 1 times 2 2 None Wn,Expr 32 ED ED Wm*Wm, Acc, Wx, Wy, Wxd Euclidean Distance (no accumulate) 1 1 OA,OB,OAB, SA,SB,SAB 33 1 OA,OB,OAB, Euclidean Distance 1 EDAC EDAC Wm*Wm, Acc, Wx, Wy, Wxd SA,SB,SAB 34 EXCH EXCH Wns,Wnd Swap Wns with Wnd 1 1 None 35 FBCL FBCL Find Bit Change from Left (MSb) Side 1 1 С Ws,Wnd 36 FF1L FF1L Ws,Wnd Find First One from Left (MSb) Side 1 1 С 37 FF1R Find First One from Right (LSb) Side 1 С FF1R Ws,Wnd 1 38 2 GOTO GOTO Go to address 2 None Expr 1 2 GOTO Go to indirect None Wn 39 1 INC INC f f = f + 11 C,DC,N,OV,Z TNC f,WREG WREG = f + 11 1 C,DC,N,OV,Z INC Ws,Wd Wd = Ws + 11 1 C,DC,N,OV,Z 40 1 C,DC,N,OV,Z INC2 INC2 f = f + 2 1 f WREG = f + 21 C,DC,N,OV,Z INC2 1 f,WREG INC2 Ws,Wd Wd = Ws + 21 1 C,DC,N,OV,Z 41 TOR IOR f f = f .IOR. WREG 1 1 N.Z f,WREG WREG = f .IOR. WREG 1 1 N,Z IOR Wd = lit10 .IOR. Wd 1 1 N.Z #lit10,Wn TOR Wd = Wb .IOR. Ws 1 1 N,Z IOR Wb,Ws,Wd τor Wd = Wb .IOR. lit5 1 1 N.Z Wb, #lit5, Wd 42 LAC LAC Wso, #Slit4, Acc Load Accumulator 1 1 OA.OB.OAB. SA,SB,SAB 43 LNK LNK #lit14 Link Frame Pointer 1 1 None 44 LSR LSR f = Logical Right Shift f 1 1 C,N,OV,Z f LSR f,WREG WREG = Logical Right Shift f 1 1 C,N,OV,Z Wd = Logical Right Shift Ws 1 1 C,N,OV,Z LSR Ws,Wd Wnd = Logical Right Shift Wb by Wns 1 1 N,Z LSR Wb,Wns,Wnd Wnd = Logical Right Shift Wb by lit5 1 N.Z LSR Wb, #lit5, Wnd 1 45 OA,OB,OAB, MAC MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd Multiply and Accumulate 1 1 SA,SB,SAB AWB OA,OB,OAB, MAC 1 1 Wm*Wm,Acc,Wx,Wxd,Wy,Wyd Square and Accumulate SA,SB,SAB 46 MOV MOV Move f to Wn 1 1 None f,Wn MOV Move f to f 1 1 N,Z f Move f to WREG N,Z MOV f,WREG 1 1 MOV #lit16,Wn Move 16-bit literal to Wn 1 1 None Move 8-bit literal to Wn 1 1 MOV.b #lit8,Wn None Move Wn to f 1 MOV Wn,f 1 None Move Ws to Wd 1 MOV Wso,Wdo 1 None Move WREG to f N,Z MOV WREG, f 1 1 MOV.D Wns,Wd Move Double from W(ns):W(ns + 1) to Wd 1 2 None MOV.D Ws,Wnd Move Double from Ws to W(nd + 1):W(nd) 1 2 None 47 Prefetch and store accumulator 1 MOVSAC MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB 1 None

TABLE 23-2: INSTRUCTION SET OVERVIEW (CONTINUED)

24.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft[®] Windows[®] 32-bit operating system were chosen to best make these features available in a simple, unified application.

24.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

24.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming[™] (ICSP[™]) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

24.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

25.1 DC Characteristics

Characteristic	VDD Range	Temp Range	Max MIPS		
Characteristic	(in Volts)	(in °C)	dsPIC33FJXXXGPX06/X08/X10		
DC5	3.0-3.6V	-40°C to +85°C	40		

TABLE 25-1: OPERATING MIPS VS. VOLTAGE

TABLE 25-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Мах	Unit
dsPIC33FJXXXGPX06/X08/X10					
Operating Junction Temperature Range	TJ	-40	_	+125	°C
Operating Ambient Temperature Range	TA	-40	_	+85	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation: $I/O = \Sigma (\{VDD - VOH\} x IOH) + \Sigma (VOL x IOL)$	PD	PINT + PI/O		W	
Maximum Allowed Power Dissipation	PDMAX	(TJ - TA)/θJ	A	W

TABLE 25-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Мах	Unit	Notes
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θja	40	_	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θја	40	_	°C/W	1
Package Thermal Resistance, 80-pin TQFP (12x12x1 mm)	θја	40	-	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θja	40		°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimensio	n Limits	MIN NOM MAX			
Number of Leads	Ν	100			
Lead Pitch	е	0.50 BSC			
Overall Height	А	-	—	1.20	
Molded Package Thickness	A2	0.95	1.00	1.05	
Standoff	A1	0.05	-	0.15	
Foot Length	L	0.45	0.60	0.75	
Footprint	L1	1.00 REF			
Foot Angle	φ	0°	3.5°	7°	
Overall Width	Е	16.00 BSC			
Overall Length	D	16.00 BSC			
Molded Package Width	E1	14.00 BSC			
Molded Package Length	D1	14.00 BSC			
Lead Thickness	С	0.09	-	0.20	
Lead Width	b	0.17	0.22	0.27	
Mold Draft Angle Top	α	11°	12°	13°	
Mold Draft Angle Bottom	β	11°	12°	13°	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

- 4. Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110A