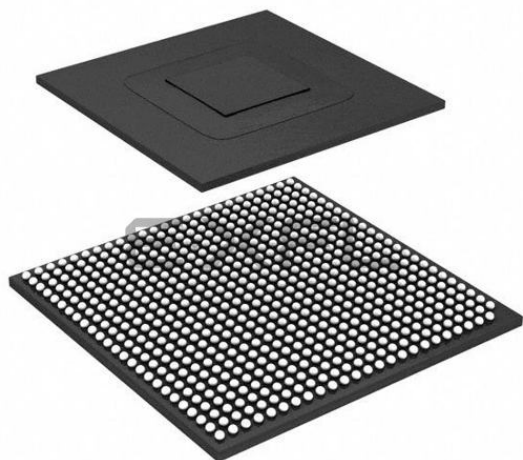




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

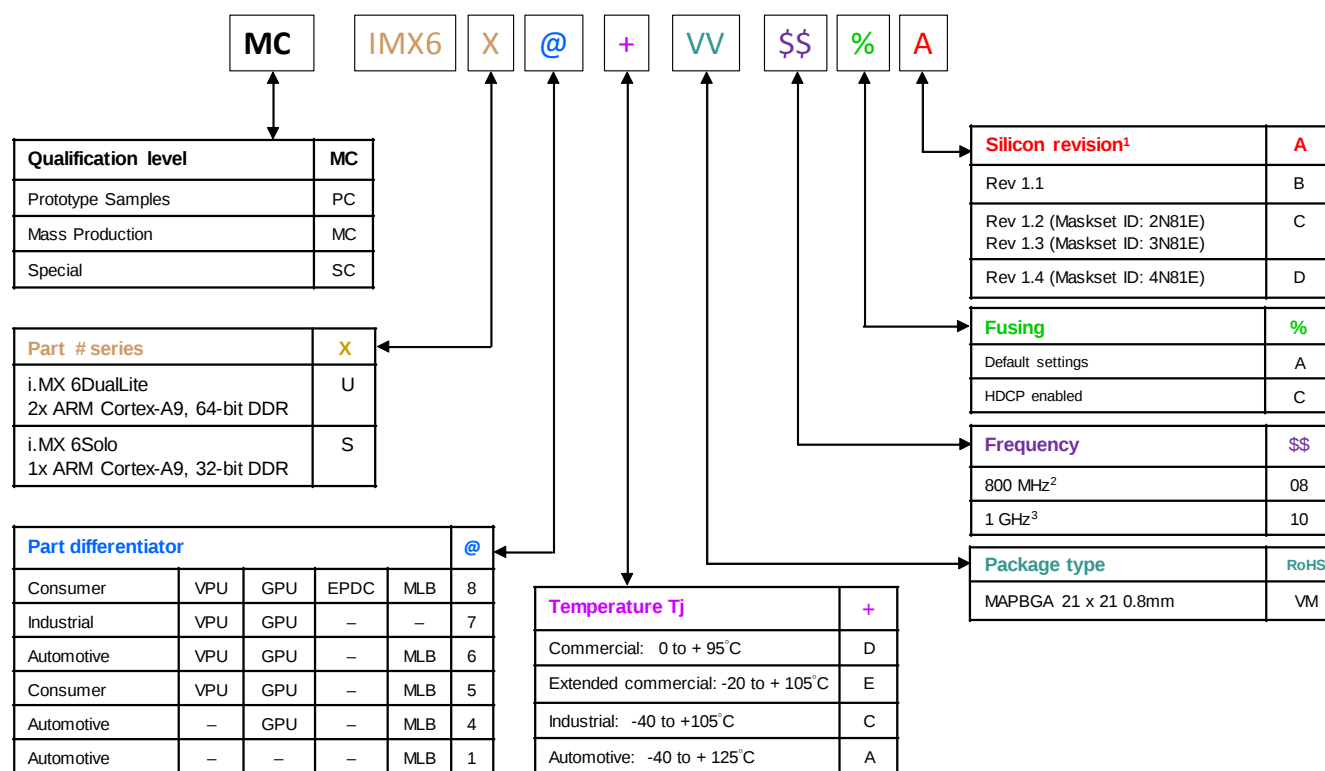
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM® Cortex® -A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6s4avm08ad

- The *i.MX 6Solo/6DualLite Applications Processors for Industrial Products* data sheet (IMX6SDLIEC) covers parts listed with “C (Industrial temp)”

For more information go to nxp.com/imx6series or contact a NXP representative for details.



- See the nxp.com/imx6series Web page for latest information on the available silicon revision.
- If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
- If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Solo and 6DualLite

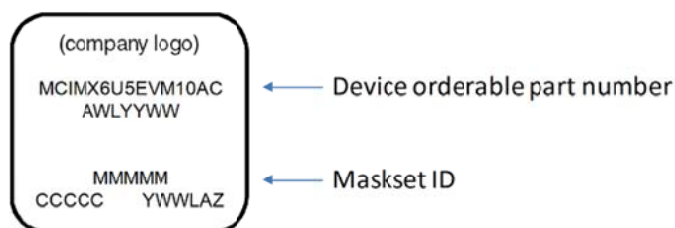


Figure 2. Example Part Marking

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:

Table 10. Maximum Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_LVDS2P5 ⁶	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handling the current required by NVCC_LVDS2P5.	—
MISC			
DDR_VREF	—	1	mA

¹ The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIP1, or HDMI and PCIe VPH supplies).

² Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown in Table 10. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

³ This is the maximum current per active USB physical interface.

⁴ The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

⁵ General equation for estimated, maximum power consumption of an IO power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.

⁶ NVCC_LVDS2P5 is supplied by VDD_HIGH_CAP (by external connection) so the maximum supply current is included in the current shown for VDD_HIGH_IN. The maximum supply current for NVCC_LVDS2P5 has not been characterized separately.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical ¹	Units
WAIT	- ARM, SoC, and PU LDOs are set to 1.225 - HIGH LDO set to 2.5 V - Clocks are gated. - DDR is in self refresh. - PLLs are active in bypass (24MHz) - Supply Voltages remain ON	VDD_ARM_IN (1.4V)	4.5	mA
		VDD_SOC_IN (1.4V)	23	
		VDD_HIGH_IN (3.0V)	13.5	
		Total	79	mW

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_VBUS valid detectors in typical condition. [Table 12](#) shows the USB interface current consumption in power down mode.

Table 12. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 μ A	1.7 μ A	<0.5 μ A

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

[Table 13](#) provides PCIe PHY currents under certain Tx operating modes.

Table 13. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	

4.2.1 Power-Up Sequence

The restrictions that follow must be observed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- The SRC_POR_B signal controls the processor POR and must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 6, “Package Information and Contact Assignments.”](#)

NOTE

When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies must be powered or grounded. The input and output supplies for the remaining ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo	—	1.6	—	kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in [Figure 5](#) and [Figure 6](#).

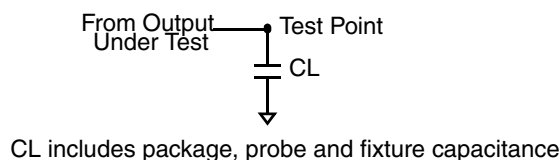


Figure 5. Load Circuit for Output

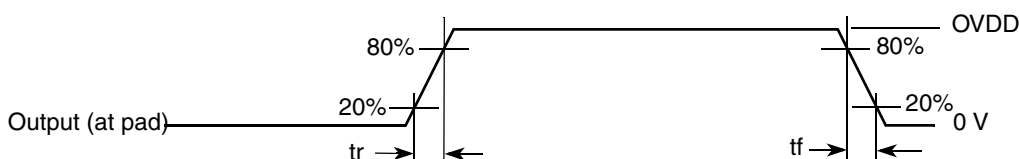


Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the [Table 29](#) and [Table 30](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in [Figure 7](#).

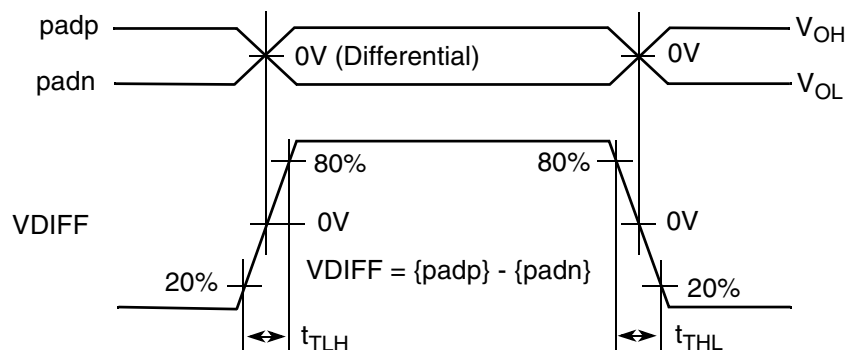


Figure 7. Differential LVDS Driver Transition Time Waveform

[Table 33](#) shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t_{SKD}	$R_{load} = 100\ \Omega$, $C_{load} = 2\ pF$	—	—	0.25	ns
Transition Low to High Time ²	t_{TLH}		—	—	0.5	
Transition High to Low Time ²	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in [Figure 8](#).

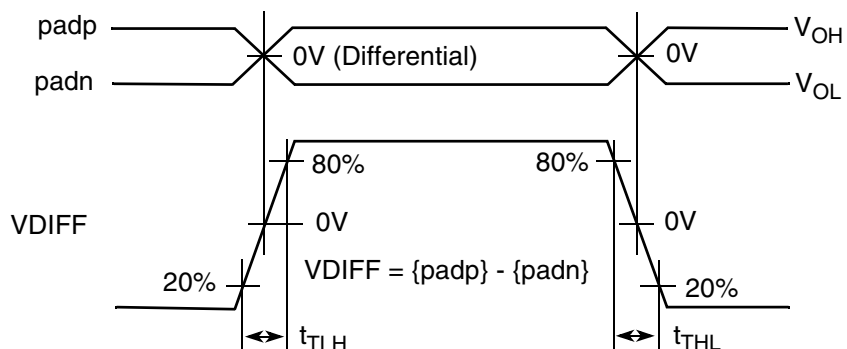


Figure 8. Differential MLB Driver Transition Time Waveform

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.8.4 MLB I/O Differential Output Impedance

Table 38 shows MLB I/O differential output impedance of the i.MX 6Solo/6DualLite processors.

Table 38. MLB I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Zo	—	1.6	—	—	kΩ

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 11 shows the reset timing and Table 39 lists the timing parameters.

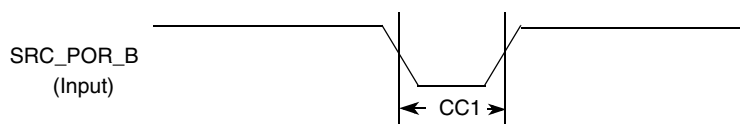


Figure 11. Reset Timing Diagram

Table 39. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 12 shows the WDOG reset timing and Table 40 lists the timing parameters.

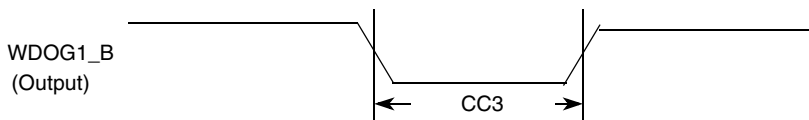


Figure 12. WDOG1_B Timing Diagram

Table 40. WDOG1_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	XTALOSC_RTC_XTALI cycle

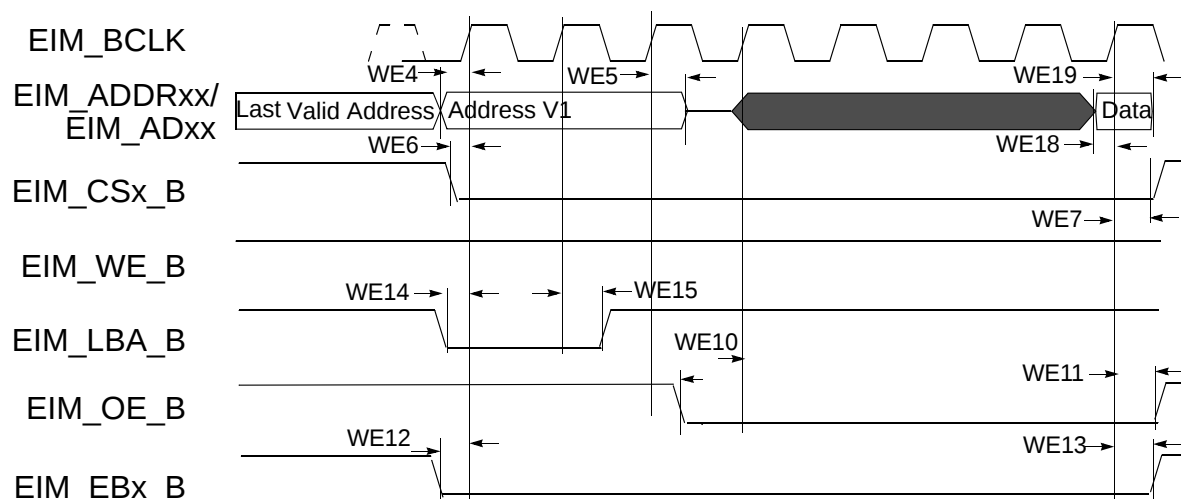


Figure 18. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 19 through Figure 23, and Table 43 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 19 through Figure 22 as RWSC, OEN and CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

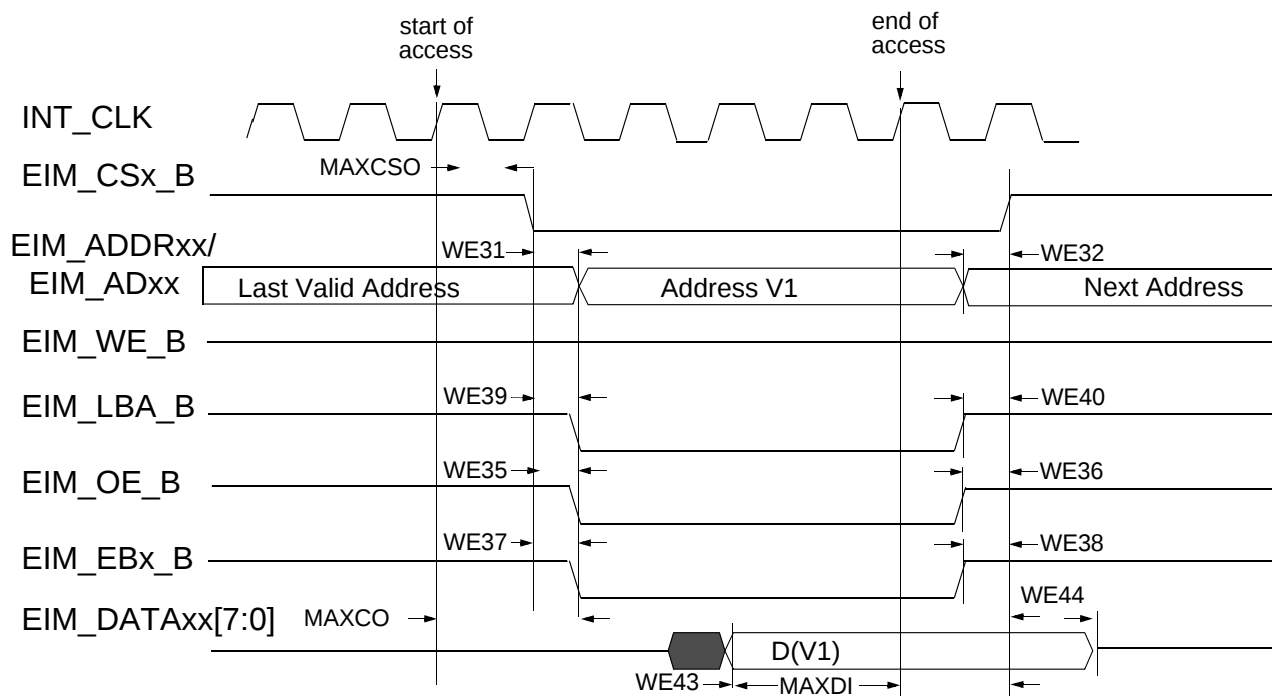


Figure 19. Asynchronous Memory Read Access (RWSC = 5)

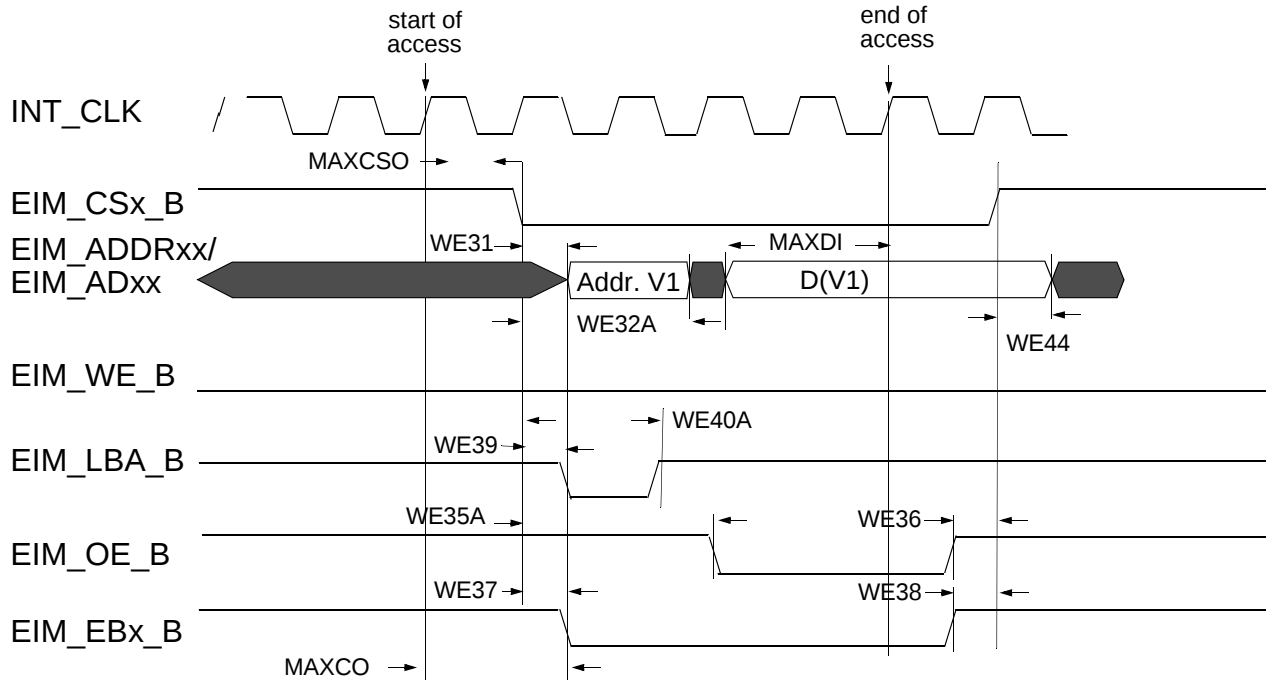


Figure 20. Asynchronous A/D Muxed Read Access (RWSC = 5)

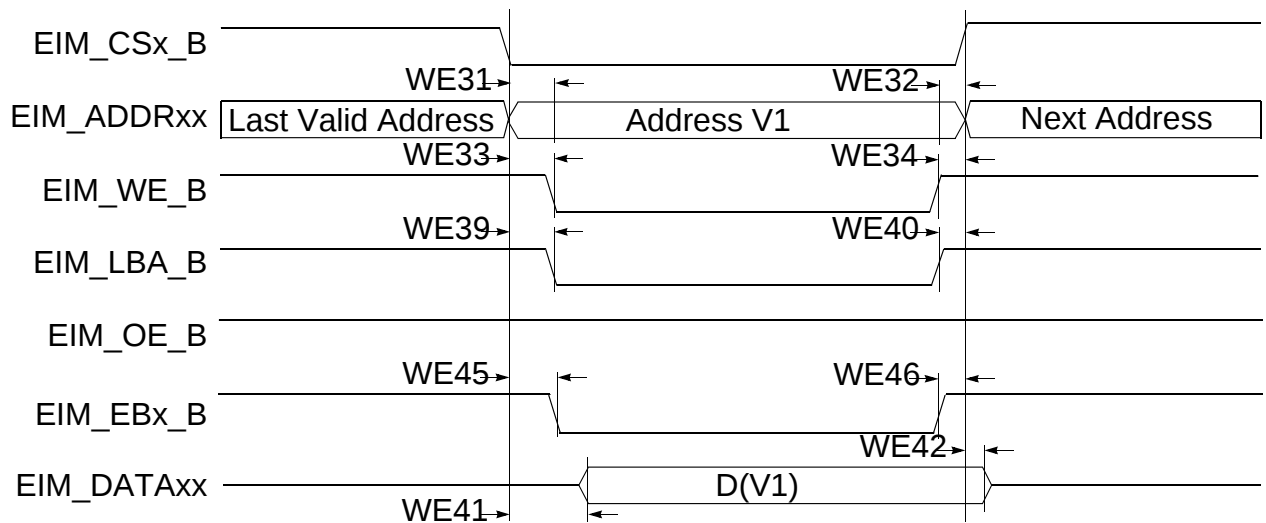


Figure 21. Asynchronous Memory Write Access

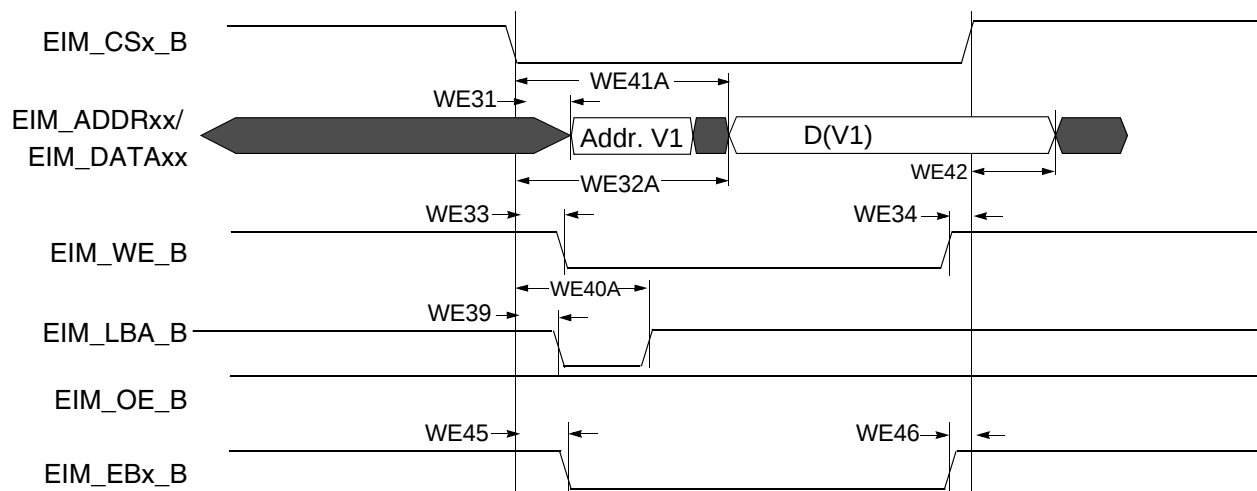


Figure 22. Asynchronous A/D Muxed Write Access

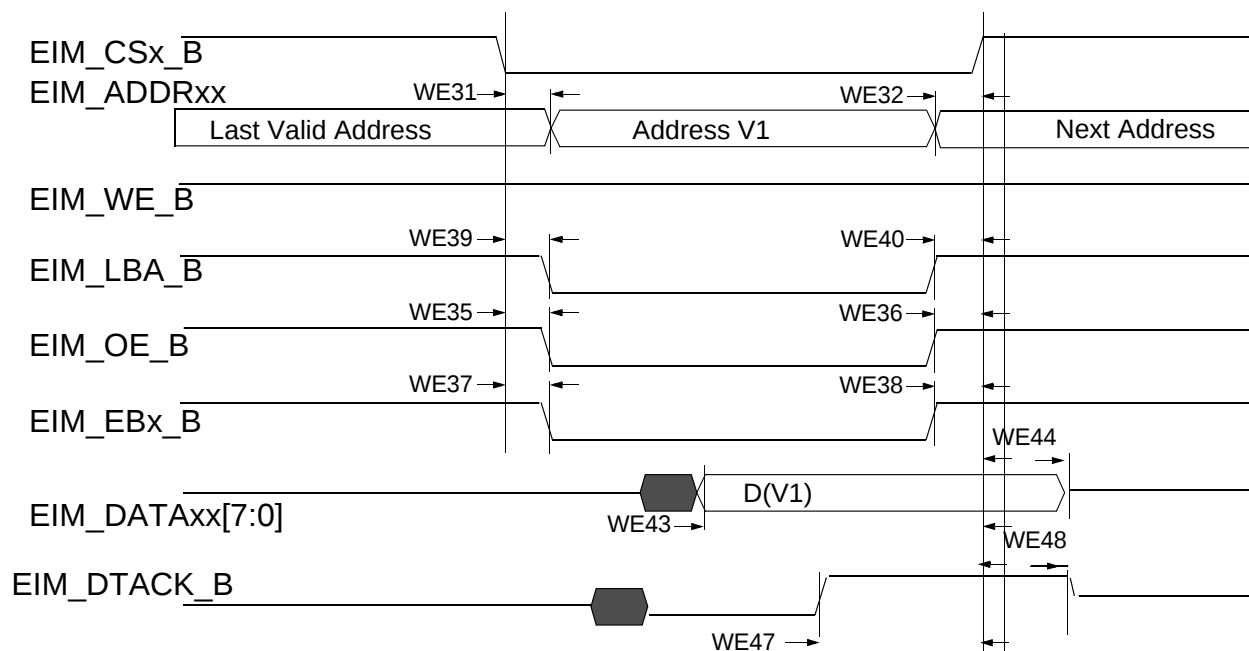


Figure 23. DTACK Mode Read Access (DAP=0)

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters ¹	Min	Max	Unit
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

² In this table, CSA means WCSA when write operation or RCSA when read operation.

³ In this table, CSN means WCSN when write operation or RCSN when read operation.

⁴ t is ACLK_EIM_SLOW_CLK_ROOT cycle time.

⁵ In this table, ADVN means WADV when write operation or RADVN when read operation.

⁶ In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.9.4.1 MMDC Compatibility with JEDEC-compliant SDRAMs

The i.MX 6Solo/6DualLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHGD)*.

4.9.4.2 MMDC Supported DDR3/DDR3L/LPDDR2 Configurations

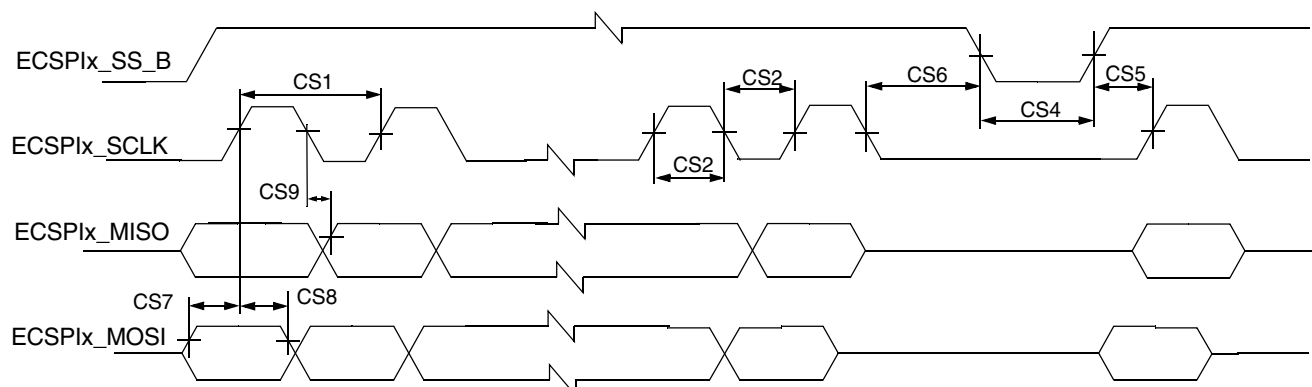
Table 44 and Table 45 show the supported DDR3/DDR3L/LPDDR2 configurations.

Table 44. i.MX 6Solo Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16/32-bit	16/32-bit	16/32-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.11.2.2 ECSPi Slave Mode Timing

Figure 37 depicts the timing of ECSPi in slave mode. Table 50 lists the ECSPi slave mode timing characteristics.



Note: ECSPi_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPi to be connected between a single master and a single slave.

Figure 37. ECSPi Slave Mode Timing Diagram

Table 50. ECSPi Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPi_SCLK Cycle Time—Read ECSPi_SCLK Cycle Time—Write	t_{clk}	43 15	—	ns
CS2	ECSPi_SCLK High or Low Time—Read ECSPi_SCLK High or Low Time—Write	t_{sw}	21.5 7	—	ns
CS4	ECSPi_SS_B pulse width	t_{CSLH}	Half ECSPi_SCLK period	—	ns
CS5	ECSPi_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPi_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPi_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPi_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPi_MISO Propagation Delay ($C_{LOAD} = 20 \text{ pF}$)	t_{PDmiso}	4	19	ns

Table 57. MII Asynchronous Inputs Signal Timing

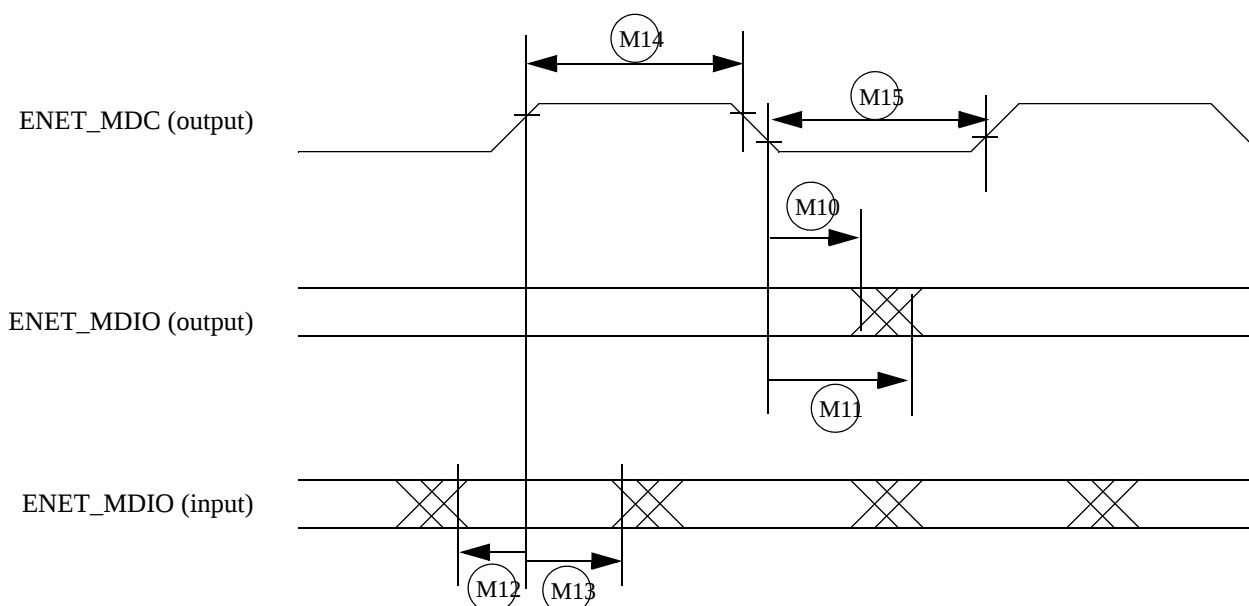
ID	Characteristic	Min	Max	Unit
M9 ¹	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 46 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

**Figure 46. MII Serial Management Channel Timing Diagram****Table 58. MII Serial Management Channel Timing**

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

Electrical Characteristics

Figure 66 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 68 lists the synchronous display interface timing characteristics.

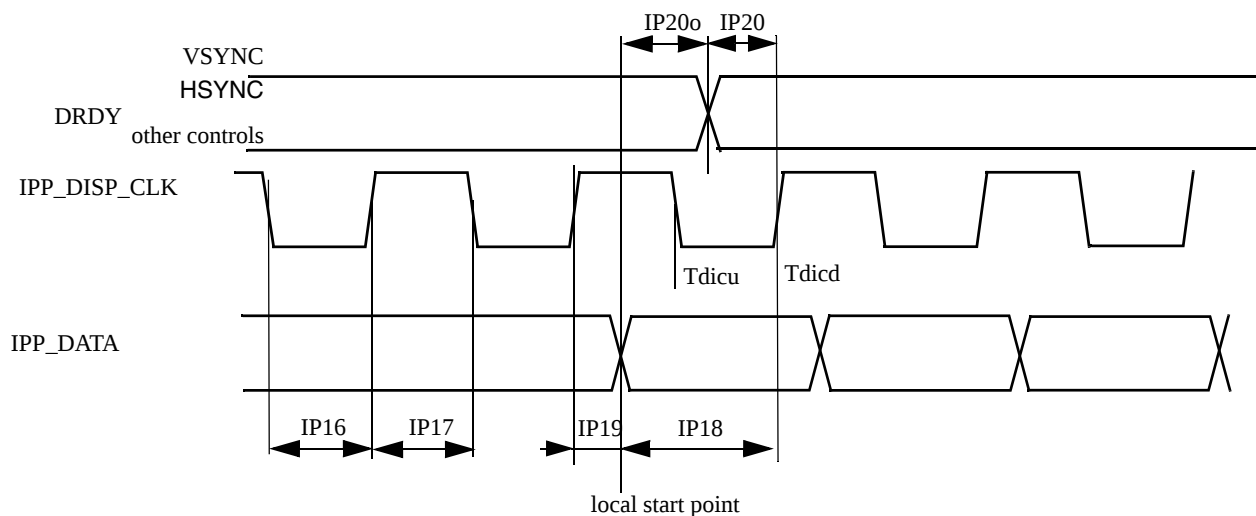


Figure 66. Synchronous Display Interface Timing Diagram—Access Level

Table 68. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ ¹	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	$Tdicd^2 - Tdicu^3$	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	$Tdicd-1.24-Tocsu\%Tdicp$	Tdicu	—	ns

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

² Display interface clock down time

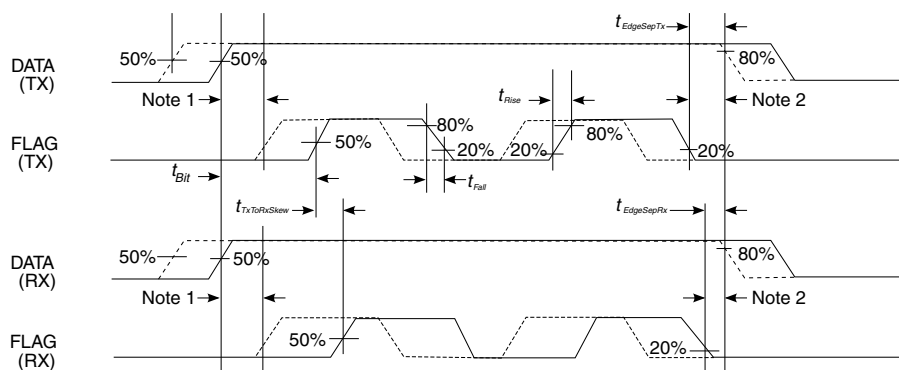
$$Tdicd = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_DOWN}}{\text{DI_CLK_PERIOD}} \right] \right)$$

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$Tdicu = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_UP}}{\text{DI_CLK_PERIOD}} \right] \right)$$

Table 72. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{\text{EdgeSepTx, min}}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{\text{EdgeSepRx, min}}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns



¹ This case shows that the DATA signal has slowed down more compared to the FLAG signal

² This case shows that the FLAG signal has slowed down more compared to the DATA signal.

Figure 81. DATA and FLAG Signal Timing

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 73 lists the MediaLB 3-pin interface electrical characteristics.

Table 73. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note ¹	1.8	—	V
Low level output threshold	V_{OL}	$I_{OL} = 6 \text{ mA}$	—	0.4	V
High level output threshold	V_{OH}	$I_{OH} = -6 \text{ mA}$	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < V_{DD}$	—	± 10	μA

¹ Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 75. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	10	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	10.75	ns	—

¹ The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

² MLB_CLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 76; unless otherwise noted.

Table 76. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK Operating Frequency ¹	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLB_CLK low time	t_{mckl}	6.1	—	ns	²
MLB_CLK high time	t_{mckh}	9.3	—	ns	—
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	³
Bus Hold from MLB_CLK low	t_{mdzh}	2	—	ns	—
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	7	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	6	ns	—

¹ The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

² MLB_CLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 77 lists the MediaLB 6-pin interface timing characteristics, and Figure 83 shows the MLB 6-pin delay, setup, and hold times.

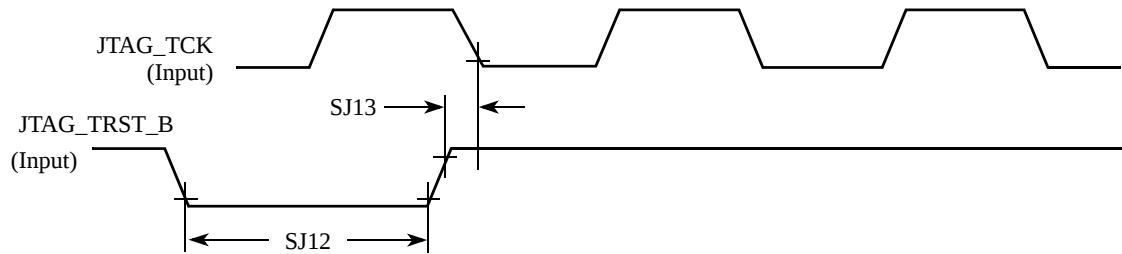


Figure 88. JTAG_TRST_B Timing Diagram

Table 79. JTAG Timing

ID	Parameter ^{1,2}	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \cdot T_{DC})^1$	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M^2	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

¹ T_{DC} = target frequency of SJC

² V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figure 89 and Figure 90 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value ²
LVDS1_TX2_N	AB1	NVCC_LVDS2P5	—	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS2P5	—	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5	—	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS2P5	—	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP	—	—	MLB_CLK_N	—	—
MLB_CP	B11	VDDHIGH_CAP	—	—	MLB_CLK_P	—	—
MLB_DN	B10	VDDHIGH_CAP	—	—	MLB_DATA_N	—	—
MLB_DP	A10	VDDHIGH_CAP	—	—	MLB_DATA_P	—	—
MLB_SN	A9	VDDHIGH_CAP	—	—	MLB_SIG_N	—	—
MLB_SP	B9	VDDHIGH_CAP	—	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	100 kΩ pull-up
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	SRC_ONOFF	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open drain with PU(100K) enable
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value ²
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	100 kΩ pull-down
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-up

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSIO_PIXCLK	CSIO_DAT4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSIO_DAT5	CSIO_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSIO_DATA_EN	CSIO_DAT7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSIO_MCLK	CSIO_DAT6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSIO_DAT9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSIO_DAT8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DIO_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DAT4	DIO_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DAT3	DIO_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DAT8	DISP0_DAT1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DAT6	DISP0_DAT2	EIM_DA14
GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	DISP0_DAT7	DISP0_DAT0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	DISP0_DAT5	DIO_PIN4	DIO_PIN2
Y	W	V	U	T	R	P	N