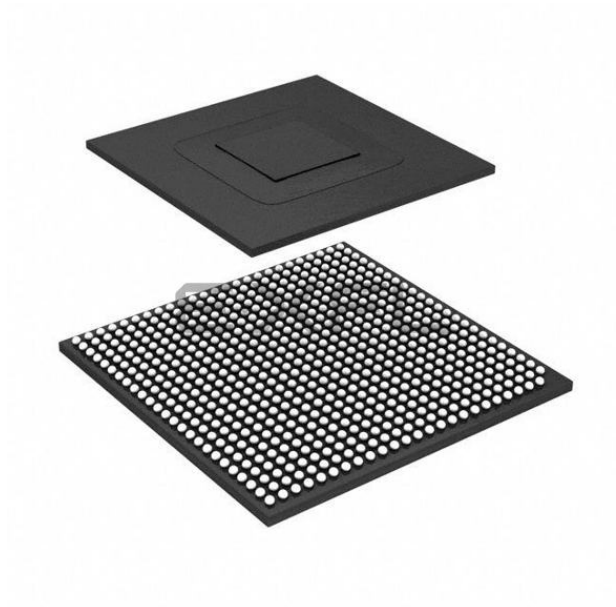

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u1avm08ad

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on the web page nxp.com/imx6series. If the desired part number is not listed in Table 1, go to nxp.com/imx6series or contact a NXP representative for details.

Table 1. Example Orderable Part Numbers

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade[1]	Temperature Grade	Package
MCIMX6U6AVM08AB	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U6AVM08AC	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U6AVM08AD	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM08AB	DualLite	With GPU, MLB, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM08AC	DualLite	With GPU, MLB, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM08AD	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM08AB	DualLite	With MLB, no GPU, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM08AC	DualLite	With MLB, no GPU, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM08AD	DualLite	With MLB, no GPU, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM08AB	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM08AC	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM08AD	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM08AB	Solo	With GPU, MLB, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM08AC	Solo	With GPU, MLB, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM08AD	Solo	With GPU, MLB, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S1AVM08AB	Solo	With MLB, no GPU, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S1AVM08AC	Solo	With MLB, no GPU, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

4.1.3 Operating Ranges

Table 8 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (*IMX6SDLRM*)*.

Table 8. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN	1.4[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.275 V minimum for operation up to 996MHz.
		1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.150 V minimum for operation up to 792MHz.
		1.25[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.125 V minimum for operation up to 396MHz.
	VDD_SOC_IN	1.275[3,4]	—	1.5	V	ARM ≤ 792 MHz, VPU ≤ 328 MHz: VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) = 1.225 V[5] maximum and 1.15 V minimum.
		1.275[3,]	—	1.5	V	ARM ≤ 996 MHz, VPU ≤ 328 MHz: VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) = 1.225 V[5] maximum and 1.175 V minimum.
Run mode: LDO bypassed[6]	VDD_ARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.125	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDD_SOC_IN	1.150[7]	—	1.21[5]	V	LDO bypassed for operation VPU ≤ 328 MHz
Standby/DSM mode	VDD_ARM_IN	0.9	—	1.3	V	Refer to Table 11, "Stop Mode Current and Power Consumption," on page 30.
	VDD_SOC_IN	0.9	—	1.225[5]	V	—
VDD_HIGH internal regulator	VDD_HIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[8]	2.9	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
Supply for RGMII I/O power group[9]	NVCC_RGMII	1.15	—	2.625	V	1.15 V–1.30 V in HSIC 1.2 V mode 1.43 V–1.58 V in RGMII 1.5 V mode 1.70 V–1.90 V in RGMII 1.8 V mode 2.25 V–2.625 V in RGMII 2.5 V mode

Table 13. PCIe PHY Current Drain (continued)

Mode	Test Conditions	Supply	Max Current	Unit
Power Down	—	PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.9 HDMI Power Consumption

Table 14 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 14. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down	—	HDMI_VPH	49	µA
		HDMI_VP	1100	µA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The restrictions that follow must be observed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- The SRC_POR_B signal controls the processor POR and must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of Section 6, “Package Information and Contact Assignments.”

NOTE

When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies must be powered or grounded. The input and output supplies for the remaining ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use

Table 45. i.MX 6DualLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2 (Dual channel)	LPDDR2 (Single channel)	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz	400 MHz
Bus width	32-bit per channel	16/32-bit	16/32/64-bit	16/32/64-bit
Channel	Dual	Single	Single	Single
Chip selects	2 per channel	2	2	2

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 25 through Figure 28 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 46 describes the timing parameters (NF1–NF17) that are shown in the figures.

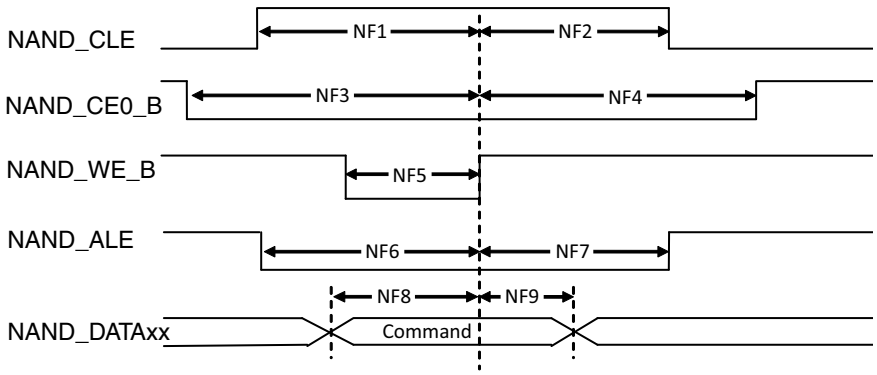

Figure 25. Command Latch Cycle Timing Diagram

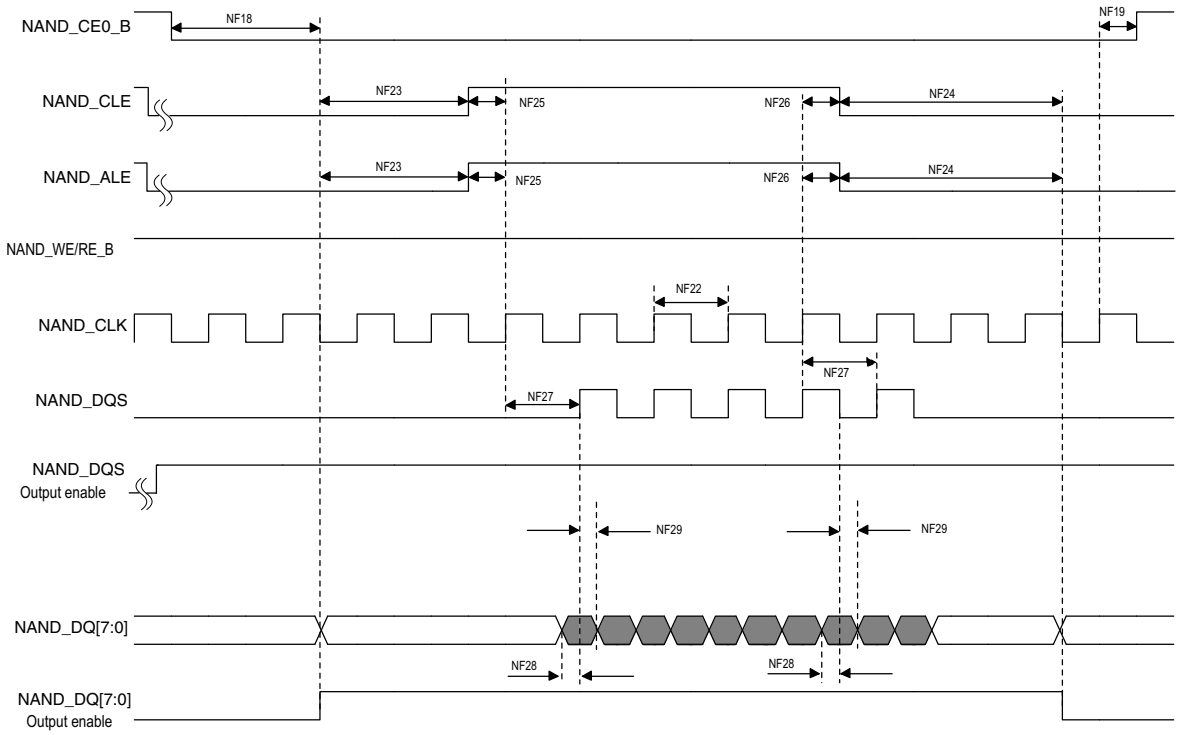

Figure 31. Source Synchronous Mode Data Write Timing Diagram

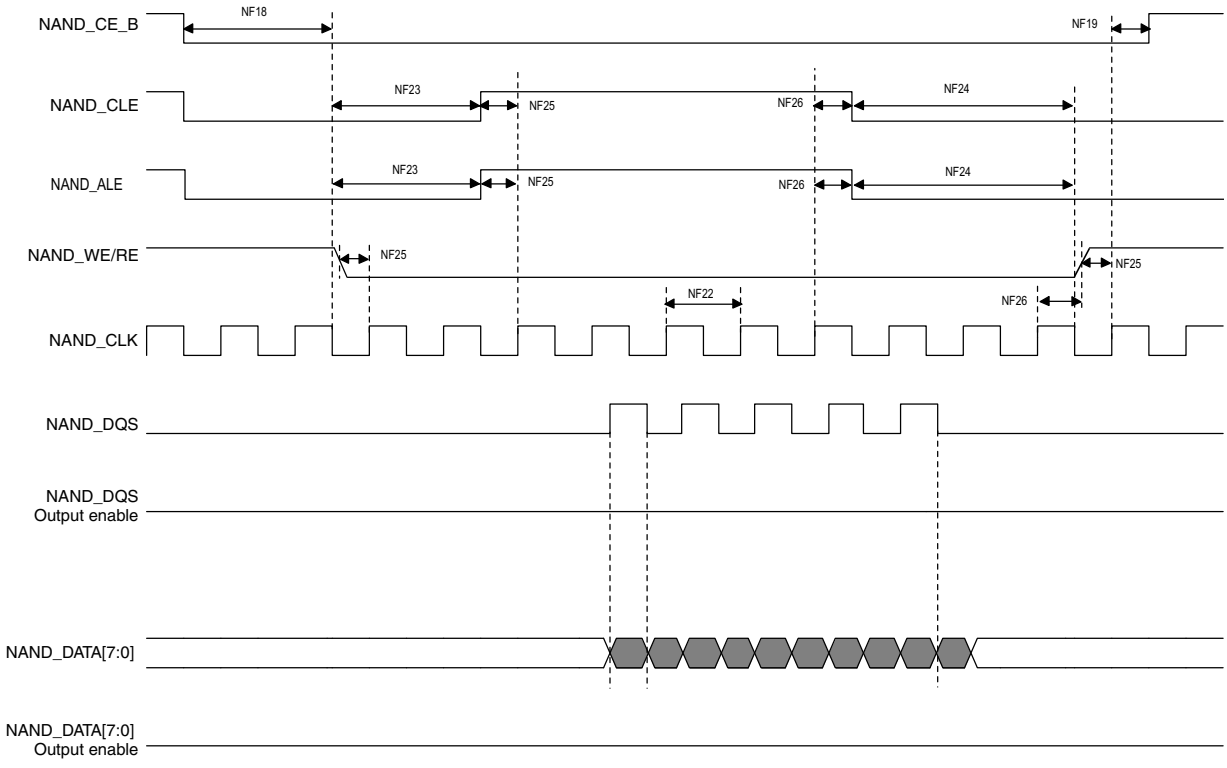

Figure 32. Source Synchronous Mode Data Read Timing Diagram

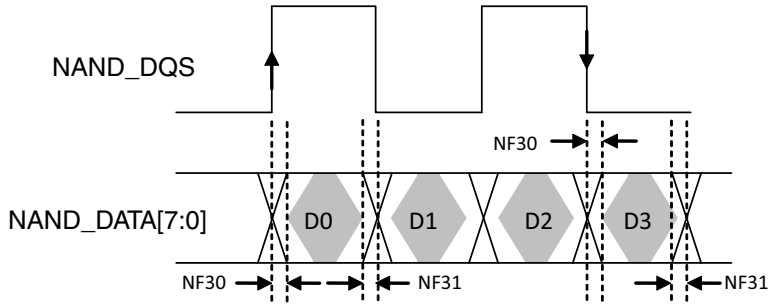

Figure 33. NAND_DQS/NAND_DQ Read Valid Window

Table 47. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		
NF29	Data write hold	—	0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	

1 GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 33 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET_TX_DATA[1:0], ENET_RX_DATA[1:0] and ENET_RX_ER.

Figure 47 shows RMII mode timings. Table 59 describes the timing parameters (M16–M21) shown in the figure.

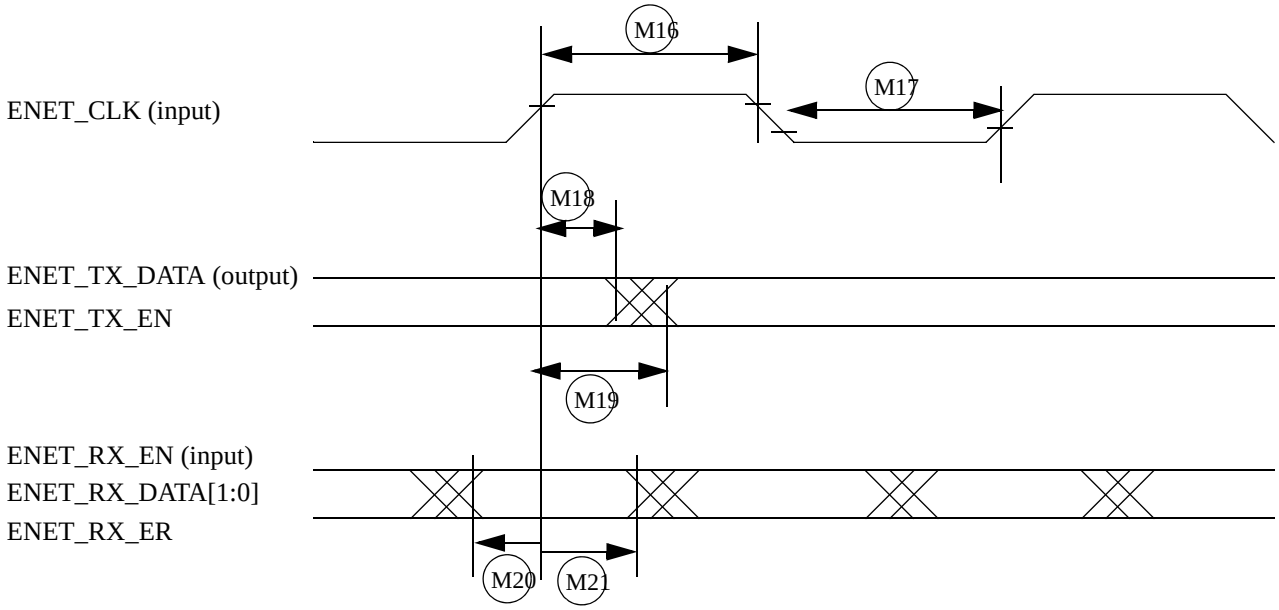

Figure 47. RMII Mode Signal Timing Diagram

Table 59. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.5.3 Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	—	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	—	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see Figure 53). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$^{VHPD}_{VL}$	Hot plug detect low range	—	0	—	0.8	V
$^{HPD}_{Z}$	Hot plug detect input impedance	—	10	—	—	kΩ
$^{HPD}_{t}$	Hot plug detect time delay	—	—	—	100	µs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 54 to Figure 58 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 59 depicts the timing of I²C module, and Table 63 lists the I²C module timing characteristics.

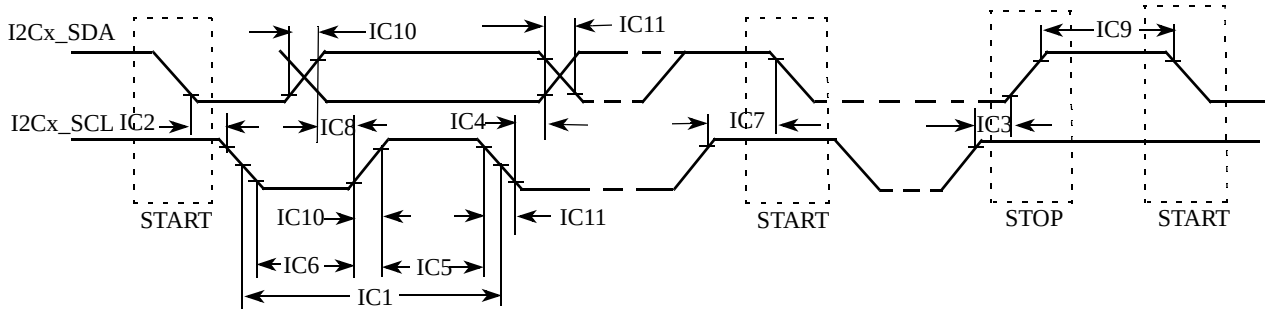

Figure 59. I²C Bus Timing

Table 63. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.11.12.8 Reverse High-Speed Data Transmission Timing

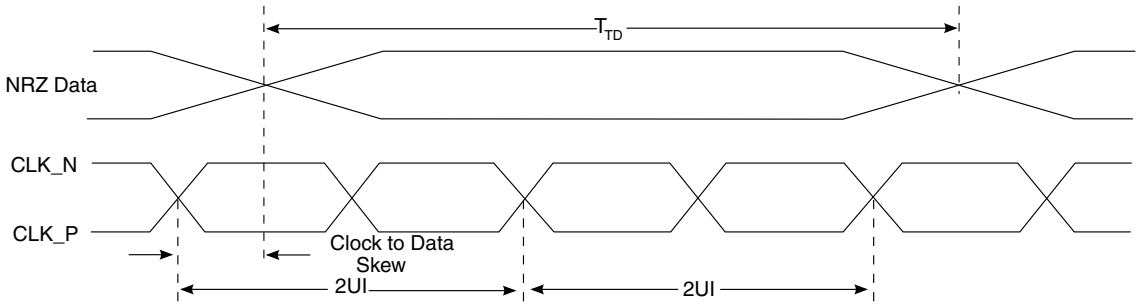

Figure 72. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.9 Low-Power Receiver Timing

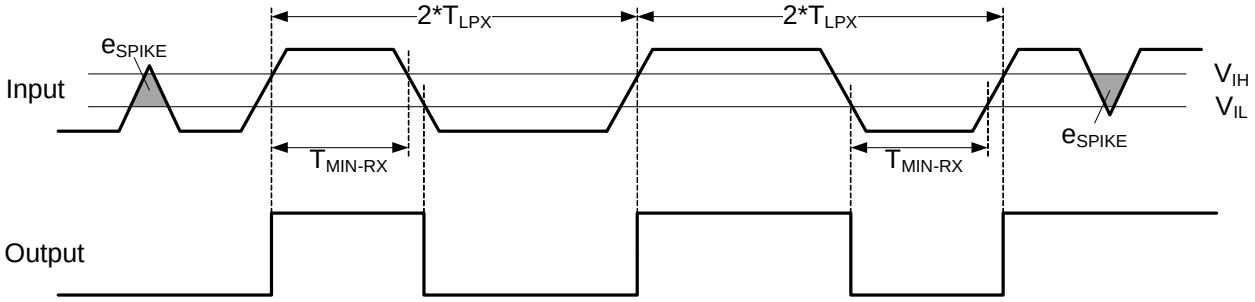

Figure 73. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

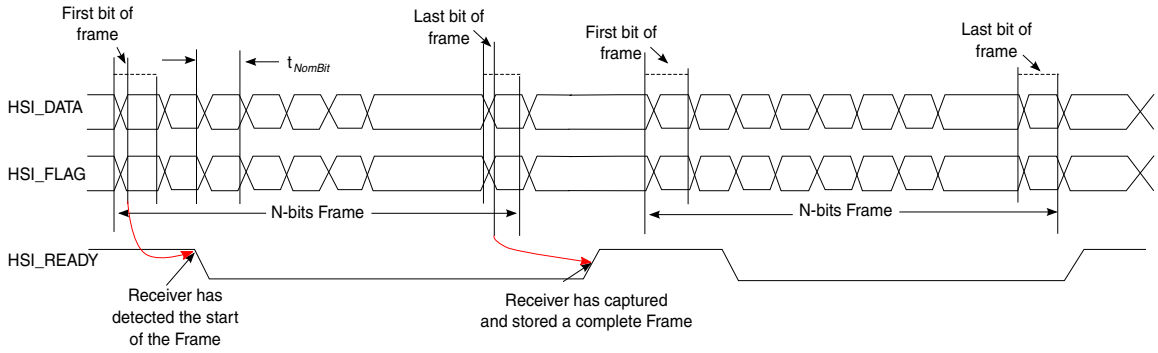

Figure 74. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 92 depicts the SSI receiver internal clock timing and Table 83 lists the timing parameters for the receiver timing with the internal clock.

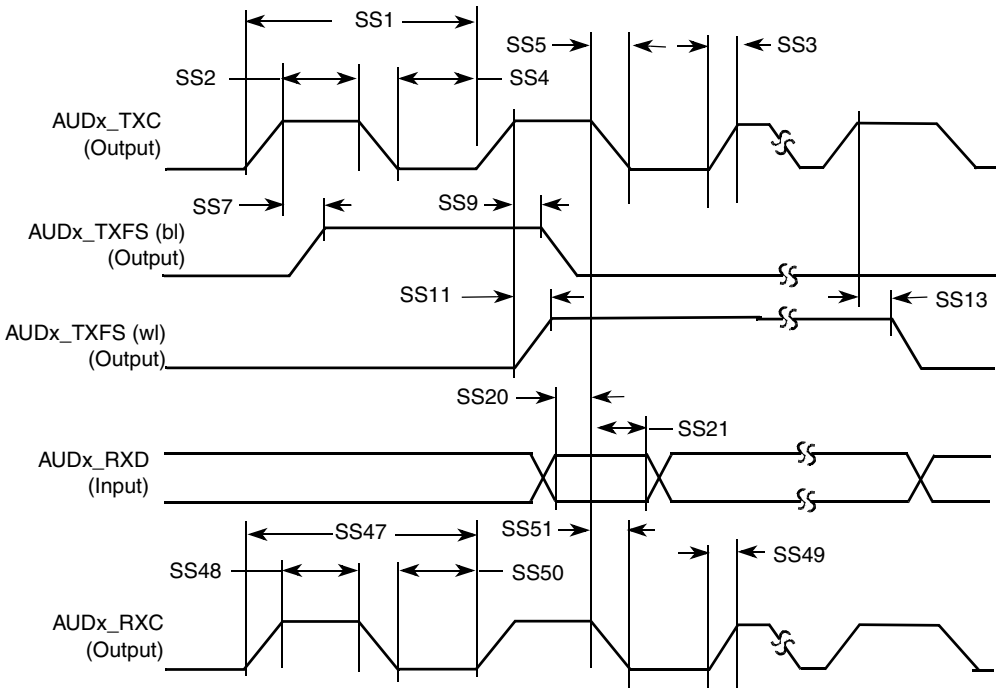

Figure 92. SSI Receiver Internal Clock Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.11.19.4 SSI Receiver Timing with External Clock

Figure 94 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

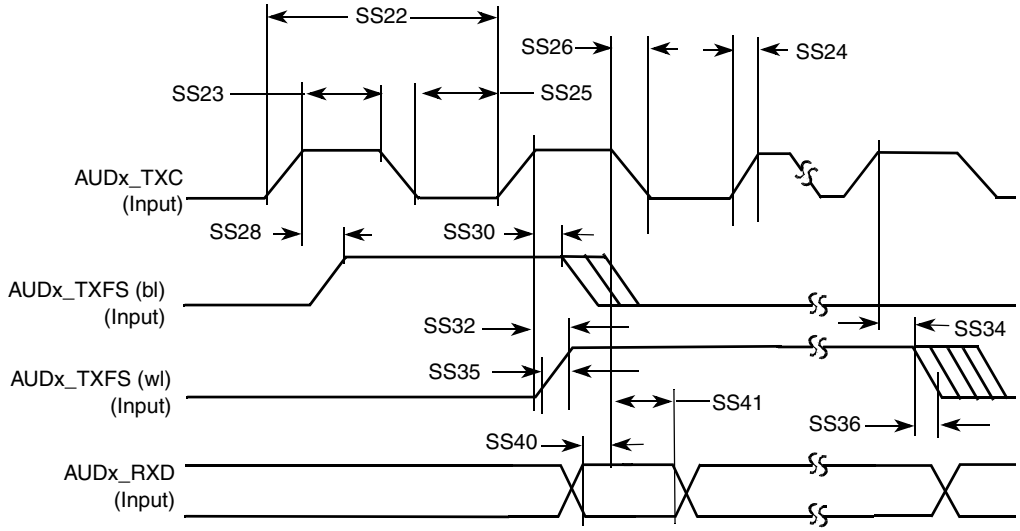

Figure 94. SSI Receiver External Clock Timing Diagram

4.11.21.2 Receive Timing

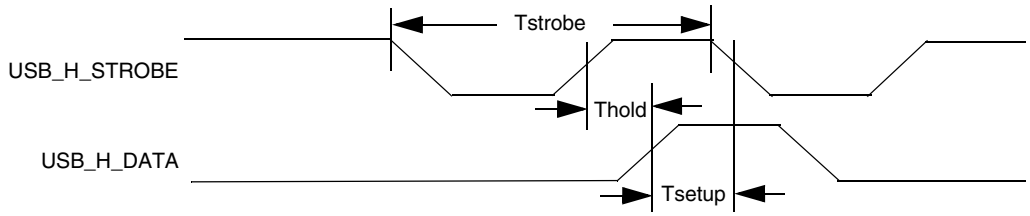

Figure 100. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification

— Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  — Revision 1.2, December 7, 2010
  — Portable device only

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 93 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 93. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	N/A
BOOT_MODE0	Input	N/A
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]

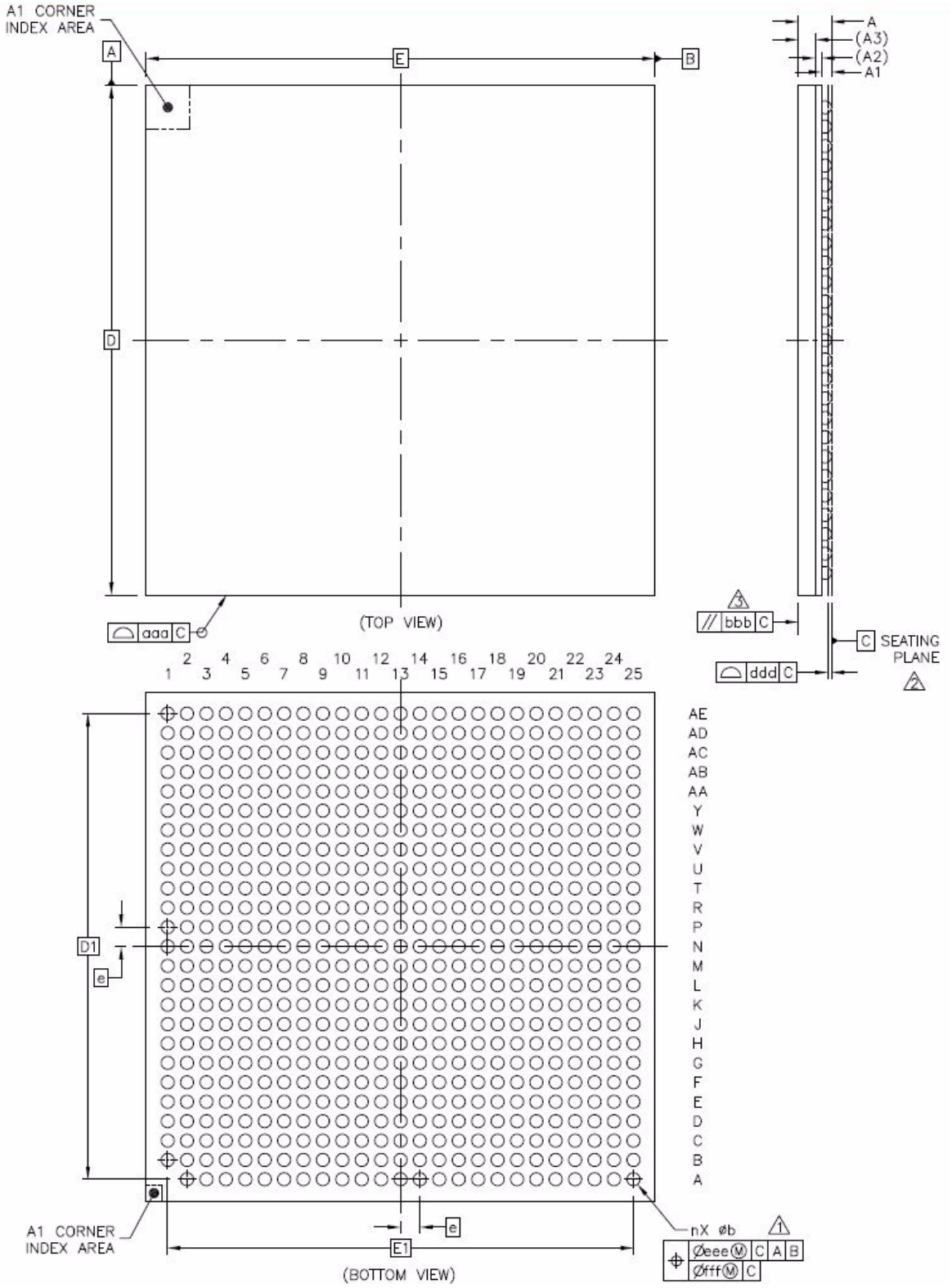

Figure 101. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

Table 96. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
ZQPAD	AE17	Connect ZQPAD to an external 240 Ω 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.
NC	**For i.MX 6DualLite:** A12, A14, B12, B14, C14, E1, E2, F1, F2, G12, G13, N12 **For i.MX 6Solo:** A12, A14, B12, B14, C14, E1, E2, F1, F2, G12, G13, N12, W25, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y25, AA17, AA18, AA20, AA21, AA23, AA24, AA25, AB18, AB19, AB20, AB21, AB22, AB23, AB25, AC18, AC19, AC20, AC21, AC22, AC23, AC24, AC25, AD18, AD20, AD21, AD23, AD24, AD25, AE18, AE19, AE20, AE21, AE22, AE23, AE24	—

Table 97 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 97. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE0	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	SRC_BOOT_MODE1	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP	—	—	CLK1_N	—	—
CLK1_P	D7	VDDHIGH_CAP	—	—	CLK1_P	—	—
CLK2_N	C5	VDDHIGH_CAP	—	—	CLK2_N	—	—
CLK2_P	D5	VDDHIGH_CAP	—	—	CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI	ANALOG	—	CSI_CLK_N	—	—
CSI_CLK0P	F3	NVCC_MIPI	ANALOG	—	CSI_CLK_P	—	—
CSI_D0M	E4	NVCC_MIPI	ANALOG	—	CSI_DATA0_N	—	—
CSI_D0P	E3	NVCC_MIPI	ANALOG	—	CSI_DATA0_P	—	—
CSI_D1M	D1	NVCC_MIPI	ANALOG	—	CSI_DATA1_N	—	—
CSI_D1P	D2	NVCC_MIPI	ANALOG	—	CSI_DATA1_P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	100 kΩ pull-up
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	—	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK1_P	Output	Low

6.2.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 99 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	NC	GND	NC	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND	**A**
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	NC	SD3_CMD	NC	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC	**B**
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N		RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	NC	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16	**C**
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23	**D**
E	NC	NC	CSI_D0P	CSI_D0M	GND	GND	GND	NVCC_PLL_OUT	USB_OTG_VBUS	USB_H1_DP	TAMPER	TEST_MODE	SD3_DAT6	SD3_DAT0	NANDF_WP_B	SD4_CLK	NANDF_D6	SD4_DAT4	SD1_DAT2	SD2_DAT1	RGMII_TD2	EIM_EB2	EIM_D22	EIM_D26	EIM_D27	**E**
F	NC	NC	CSI_CLK0P	CSI_CLK0M	GND	GND	GND	GND	VDDUSB_CAP	USB_H1_DN	PMIC_STBY_REQ	BOOT_MODE1	SD3_DAT7	SD3_DAT1	NANDF_CS0	NANDF_D2	SD4_DAT2	SD1_DAT3	SD2_CMD	RGMII_TD1	EIM_D17	EIM_D24	EIM_EB3	EIM_A22	EIM_A24	**F**
G	DSI_D0P	DSI_D0M	GND	DSI_REXT	JTAG_TDI	JTAG_TDO	PCIE_VPH	PCIE_VPTX	VDD_SNVS_CAP	GND	VDD_SNVS_IN	NC	NC	NVCC_SD3	NVCC_NANDF	NVCC_SD1	NVCC_SD2	NVCC_RGMII	GND	EIM_D20	EIM_D19	EIM_D25	EIM_D28	EIM_A17	EIM_A19	**G**