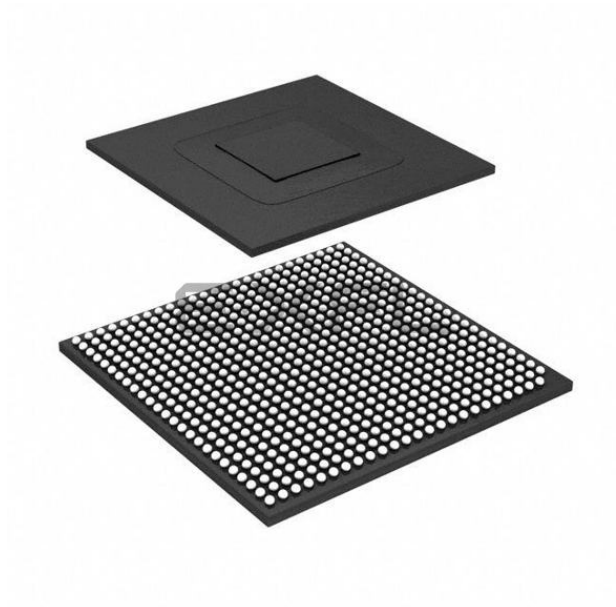

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u1avm10ad

Table 1. Example Orderable Part Numbers (continued)

Part Number	i.MX6 CPU Solo/ DualLite	Options	Speed Grade[1]	Temperature Grade	Package
MCIMX6S1AVM08AD	Solo	With MLB, no GPU, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U6AVM10AC	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U6AVM10AD	DualLite	With VPU, GPU, MLB, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM10AC	DualLite	With GPU, MLB, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM10AD	DualLite	With GPU, MLB, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM10AC	DualLite	With MLB, no GPU, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM10AD	DualLite	With MLB, no GPU, no VPU, no EPDC 2x ARM Cortex-A9 64-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM10AC	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM10AD	Solo	With VPU, GPU, MLB, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM10AC	Solo	With GPU, MLB, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM10AD	Solo	With GPU, MLB, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S1AVM10AC	Solo	With MLB, no GPU, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S1AVM10AD	Solo	With MLB, no GPU, no VPU, no EPDC 1x ARM Cortex-A9 32-bit DDR	1 GHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

[1] For 800 MHz speed grade: If a 24 MHz clock is used (required for USB), then the maximum SoC speed is limited to 792 MHz. For 1 GHz speed grade: If a 24 MHz clock is used (required for USB), then the maximum SoC speed is limited to 996 MHz.

Figure 1 describes the part number nomenclature to identify the characteristics of a specific part number (for example, cores, frequency, temperature grade, fuse options, and silicon revision).

The primary characteristic that differentiates which data sheet applies to a specific part is the temperature grade (junction) field. The following list describes the correct data sheet to use for a specific part:

- The *i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors* data sheet (IMX6SDLAEC) covers parts listed with an “A (Automotive temp)”
- The *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* data sheet (IMX6SDLCEC) covers parts listed with a “D (Commercial temp)” or “E (Extended Commercial temp)”

Table 11. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Units
STOP_ON	• ARM LDO set to 0.9V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh.	VDD_ARM_IN (1.4V)	4	mA
		VDD_SOC_IN (1.4V)	22	
		VDD_HIGH_IN (3.0V)	8.5	
		Total	61.9	mW
STOP_OFF	• ARM LDO set to 0.9V • SoC LDO set to: 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4V)	4	mA
		VDD_SOC_IN (1.4V)	13.5	
		VDD_HIGH_IN (3.0V)	7.5	
		Total	47	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9V)	0.1	mA
		VDD_SOC_IN (0.9V)	5	
		VDD_HIGH_IN (3.0V)	5	
		Total	19.6	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5V • PLLs are disabled • Low Voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9V)	0.1	mA
		VDD_SOC_IN (0.9V)	2	
		VDD_HIGH_IN (3.0V)	0.5	
		Total	3.4	mW
SNVS only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical wafer at 25°C.

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 19. MLB PLL's Electrical Parameters

Parameter	Value
Lock time	<1 ms

4.4.6 ARM PLL

Table 20. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

Table 23. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Ioh= -0.1mA (DSE=001,010) Ioh= -1mA (DSE=011,100,101,110,111)	OVDD - 0.15	—	V
Low-level output voltage[1]	VOL	Iol= 0.1mA (DSE=001,010) Iol= 1mA (DSE=011,100,101,110,111)	—	0.15	V
High-Level input voltage[1,2]	VIH	—	0.7 × OVDD	OVDD	V
Low-Level input voltage[1,2]	VIL	—	0	0.3 × OVDD	V
Input Hysteresis (OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250	—	mV
Input Hysteresis (OVDD=3.3V	VHYS_HighVDD	OVDD=3.3V	250	—	mV
Schmitt trigger VT+[2,3]	VTH+	—	0.5 × OVDD	—	mV
Schmitt trigger VT-[2,3]	VTH-	—	—	0.5 × OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V	—	212	uA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD	—	1	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V	—	100	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD	—	1	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V	—	48	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD	—	1	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD	—	48	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V	—	1	uA
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD	-1	1	uA
Keeper Circuit Resistance	R_Keeper	VI = 0.3 × OVDD, VI = 0.7 × OVDD	105	175	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 24. LPDDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	Ioh= -0.1mA	0.9 × OVDD	—	V
Low-level output voltage	VOL	Iol= 0.1mA	—	0.1 × OVDD	V

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 DDR I/O Output Buffer Impedance

For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000 001 010 011 100 101 110 111	Hi-Z 240 120 80 60 48 40 34	Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

4.8.4 MLB I/O Differential Output Impedance

Table 38 shows MLB I/O differential output impedance of the i.MX 6Solo/6DualLite processors.

Table 38. MLB I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Zo	—	1.6	—	—	kΩ

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 11 shows the reset timing and Table 39 lists the timing parameters.

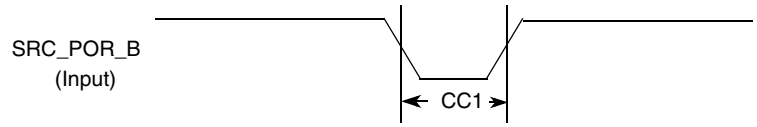

Figure 11. Reset Timing Diagram

Table 39. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 12 shows the WDOG reset timing and Table 40 lists the timing parameters.

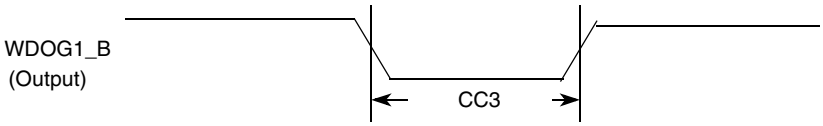

Figure 12. WDOG1_B Timing Diagram

Table 40. WDOG1_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	XTALOSC_RTC_XTALI cycle

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal FF	5	—	—	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal FF + 2 cycles for synchronization	10	—	—	—

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min	Max	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 46 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

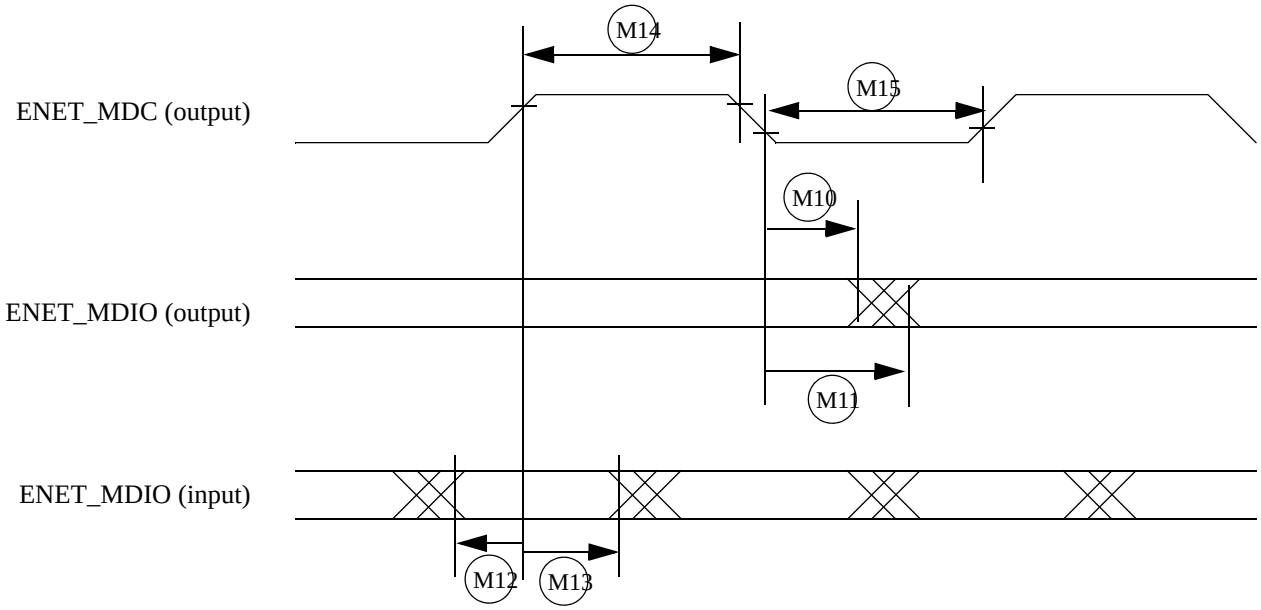

Figure 46. MII Serial Management Channel Timing Diagram

Table 58. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

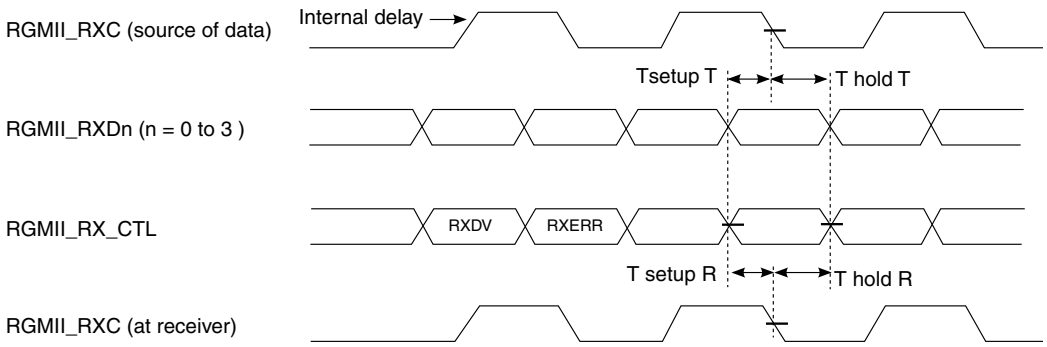

Figure 50. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	—	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	—	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see Figure 53). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$^{VHPD}_{VL}$	Hot plug detect low range	—	0	—	0.8	V
$^{HPD}_{Z}$	Hot plug detect input impedance	—	10	—	—	kΩ
$^{HPD}_{t}$	Hot plug detect time delay	—	—	—	100	µs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 54 to Figure 58 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 63 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPUx_DIx_PIN02 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPUx_DIx_PIN03 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

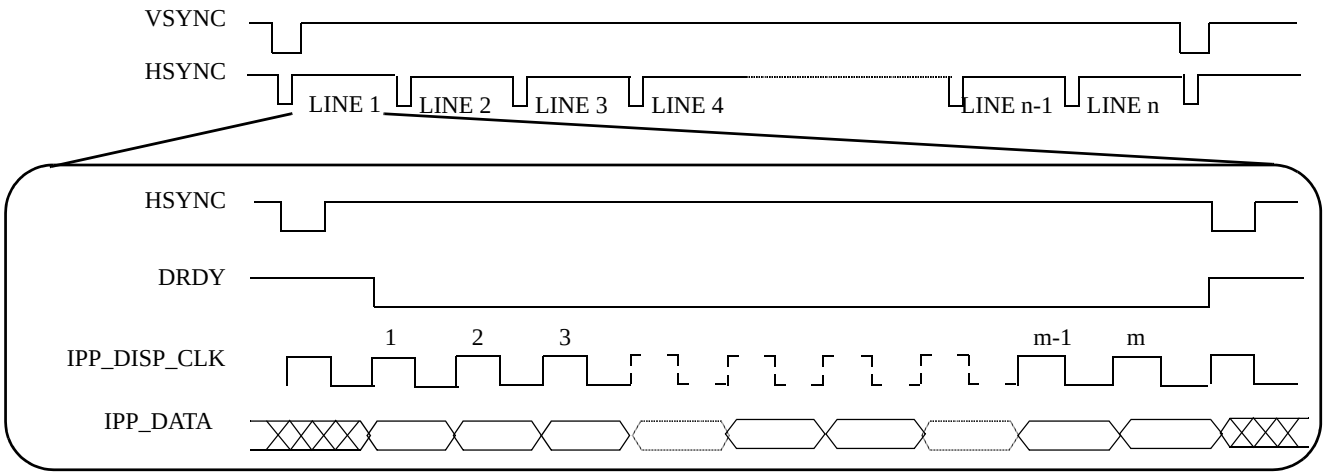

Figure 63. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 64 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by

Table 71. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF
L_S	Equivalent wire bond series inductance	—	—	—	1.5	nH
R_S	Equivalent wire bond series resistance	—	—	—	0.15	Ω
R_L	Load resistance	—	80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

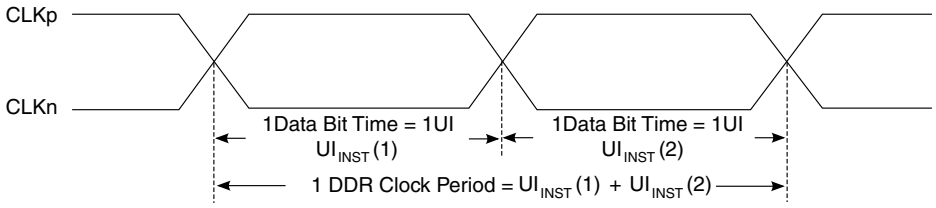

Figure 70. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 71:

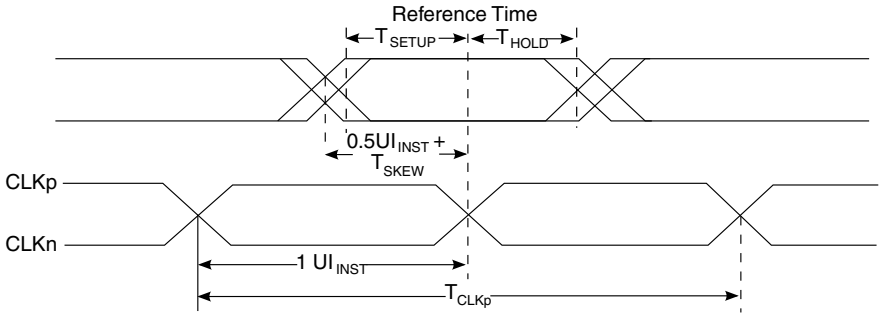

Figure 71. Data to Clock Timing Definitions

Table 74 lists the MediaLB 6-pin interface electrical characteristics.

Table 74. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $\lvert V_{O+} - V_{O-} \rvert$	V_{OD}	See Note[1]	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $\lvert V_{OD, high} - V_{OD, low} \rvert$	ΔV_{OD}	—	-50	50	mV
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\lvert V_{OCM, high} - V_{OCM, low} \rvert$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\lvert I_{OS} \rvert$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					
Differential clock input: • logic low steady-state • logic high steady-state • hysteresis	 V_{ILC} V_{IHC} V_{HSC}	See Note[4]	 — 50 -25	 -50 — 25	 mV mV mV
Differential signal/data input: • logic low steady-state • logic high steady-state	 V_{ILS} V_{IHS}	—	 — 50	 -50 —	 mV mV
Signal-ended input voltage (steady-state): • MLB_SIG_P, MLB_DATA_P • MLB_SIG_N, MLB_DATA_N	 V_{IN+} V_{IN-}	—	 0.5 0.5	 2.0 2.0	 V V

1 The signal-ended output voltage of a driver is defined as V_{O+} on MLB_CLK_P, MLB_SIG_P, and MLB_DATA_P. The signal-ended output voltage of a driver is defined as V_{O-} on MLB_CLK_N, MLB_SIG_N, and MLB_DATA_N.

2 Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-}.

3 Short circuit current is applicable when V_{O+} and V_{O-} are shorted together and/or shorted to ground.

4 The logic state of the receiver is undefined when -50 mV < V_{ID} < 50 mV.

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 92 depicts the SSI receiver internal clock timing and Table 83 lists the timing parameters for the receiver timing with the internal clock.

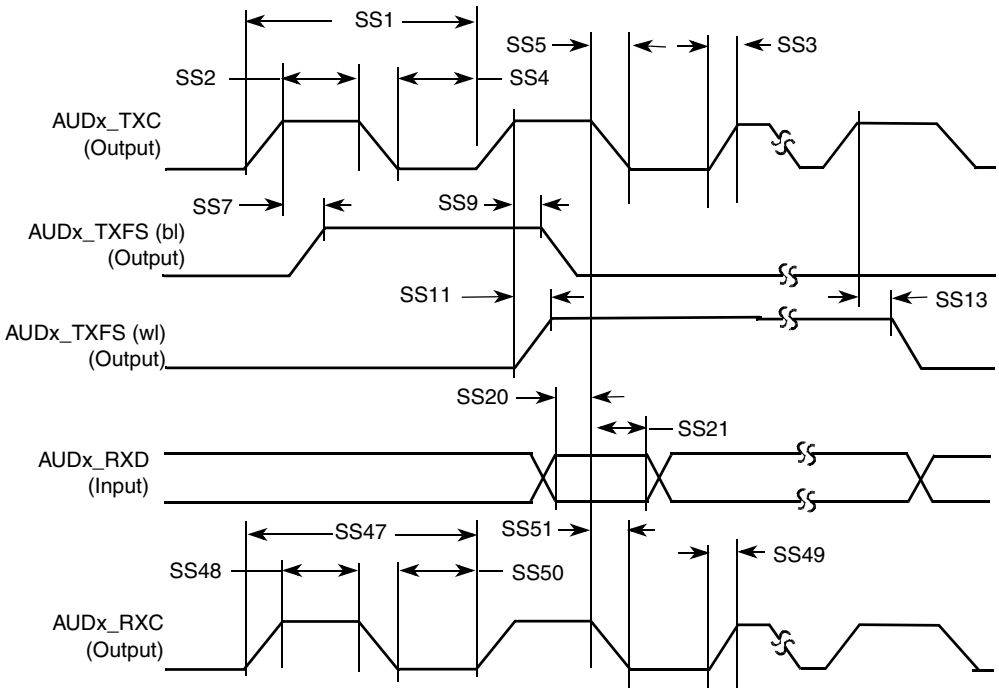

Figure 92. SSI Receiver Internal Clock Timing Diagram

Table 83. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

4.11.21.2 Receive Timing

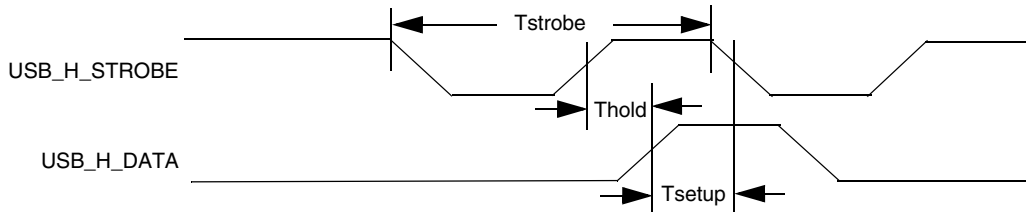

Figure 100. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	DRAM_DATA52	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	DRAM_DATA53	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	DRAM_DATA54	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	DRAM_DATA55	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	DRAM_DATA56	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	DRAM_DATA57	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	DRAM_DATA58	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	DRAM_DATA59	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	DRAM_DATA60	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	DRAM_DATA61	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	DRAM_DATA62	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	DRAM_DATA63	Input	100 kΩ pull-up
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	100 kΩ pull-up
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	DRAM_DQM4	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	DRAM_DQM5	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	DRAM_DQM6	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	DRAM_DQM7	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	—	—	DRAM_SDCLK0_N	—	—
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK1_P	Output	Low

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
LVDS1_TX2_N	AB1	NVCC_LVDS2P5	—	—	LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS2P5	—	ALT0	LVDS1_TX2_P	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5	—	—	LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS2P5	—	ALT0	LVDS1_TX3_P	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP	—	—	MLB_CLK_N	—	—
MLB_CP	B11	VDDHIGH_CAP	—	—	MLB_CLK_P	—	—
MLB_DN	B10	VDDHIGH_CAP	—	—	MLB_DATA_N	—	—
MLB_DP	A10	VDDHIGH_CAP	—	—	MLB_DATA_P	—	—
MLB_SN	A9	VDDHIGH_CAP	—	—	MLB_SIG_N	—	—
MLB_SP	B9	VDDHIGH_CAP	—	—	MLB_SIG_P	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO08	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO07	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO11	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO14	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	GPIO6_IO15	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO16	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO00	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO01	Input	100 kΩ pull-up
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	GPIO2_IO02	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO03	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO04	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO05	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO06	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO07	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	GPIO6_IO10	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	GPIO6_IO09	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	SRC_ONOFF	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH	—	—	PCIE_RX_N	—	—
PCIE_RXP	B2	PCIE_VPH	—	—	PCIE_RX_P	—	—
PCIE_TXM	A3	PCIE_VPH	—	—	PCIE_TX_N	—	—
PCIE_TXP	B3	PCIE_VPH	—	—	PCIE_TX_P	—	—
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open drain with PU(100K) enable
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	GPIO6_IO25	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	GPIO6_IO27	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	GPIO6_IO28	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	GPIO6_IO29	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	GPIO6_IO24	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	GPIO6_IO30	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	GPIO6_IO20	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	100 kΩ pull-down
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-up

Table 98. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.2.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 99 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 99. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	NC	GND	NC	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND	**A**
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	NC	SD3_CMD	NC	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC	**B**
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N		RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	NC	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16	**C**
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23	**D**
E	NC	NC	CSI_D0P	CSI_D0M	GND	GND	GND	NVCC_PLL_OUT	USB_OTG_VBUS	USB_H1_DP	TAMPER	TEST_MODE	SD3_DAT6	SD3_DAT0	NANDF_WP_B	SD4_CLK	NANDF_D6	SD4_DAT4	SD1_DAT2	SD2_DAT1	RGMII_TD2	EIM_EB2	EIM_D22	EIM_D26	EIM_D27	**E**
F	NC	NC	CSI_CLK0P	CSI_CLK0M	GND	GND	GND	GND	VDDUSB_CAP	USB_H1_DN	PMIC_STBY_REQ	BOOT_MODE1	SD3_DAT7	SD3_DAT1	NANDF_CS0	NANDF_D2	SD4_DAT2	SD1_DAT3	SD2_CMD	RGMII_TD1	EIM_D17	EIM_D24	EIM_EB3	EIM_A22	EIM_A24	**F**
G	DSI_D0P	DSI_D0M	GND	DSI_REXT	JTAG_TDI	JTAG_TDO	PCIE_VPH	PCIE_VPTX	VDD_SNVS_CAP	GND	VDD_SNVS_IN	NC	NC	NVCC_SD3	NVCC_NANDF	NVCC_SD1	NVCC_SD2	NVCC_RGMII	GND	EIM_D20	EIM_D19	EIM_D25	EIM_D28	EIM_A17	EIM_A19	**G**