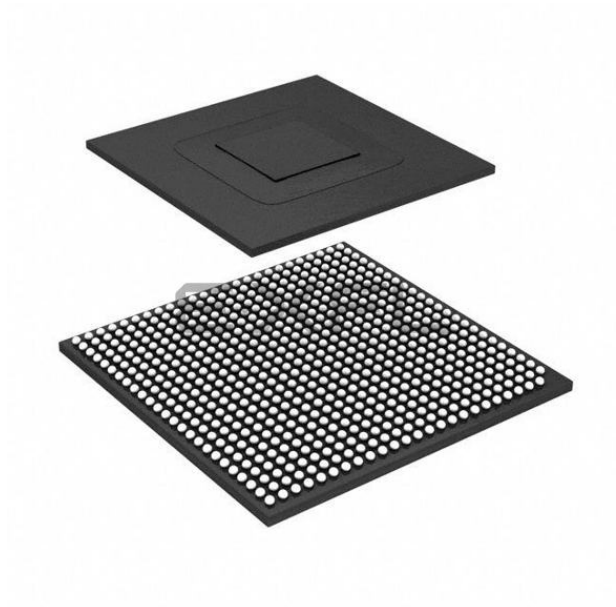

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u4avm08adr

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 3. Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

1.3 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, etc.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse fox accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPUv3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from VDD_HIGH_IN/VDD_SNVS_IN.

Table 21. OSC32K Main Characteristics

Characteristic	Min	Typ	Max	Comments
Fosc	—	32.768 KHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K will work as well.
Current consumption	—	4 μA	—	The 4 μA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μA when ring oscillator is inactive, 20 μA when the ring oscillator is running. Another 1.5 μA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μA on vdd_rtc when the ring oscillator is not running.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

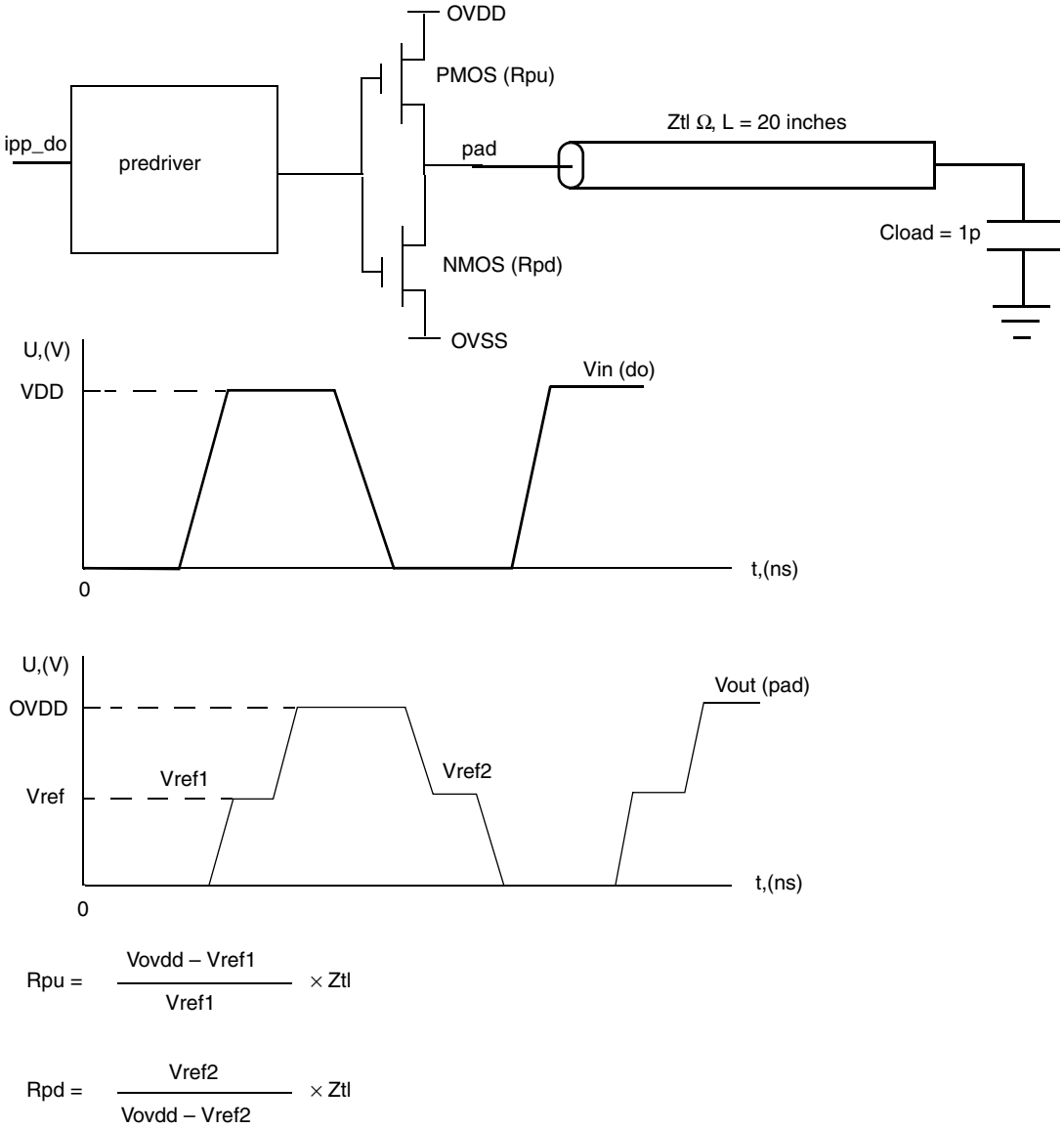
- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 10).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 10. Impedance Matching Load for Measurement

[1] For more information on configuration ports mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 13, Figure 14, and Table 42 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

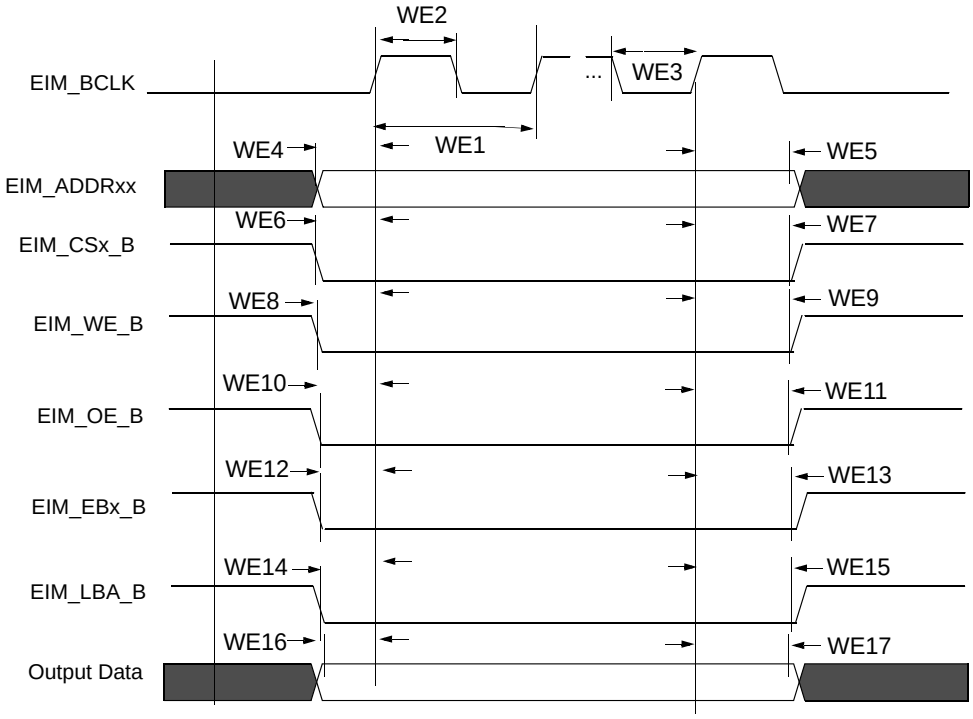


Figure 13. EIM Outputs Timing Diagram

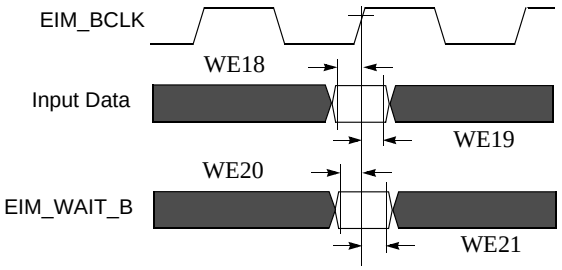


Figure 14. EIM Inputs Timing Diagram

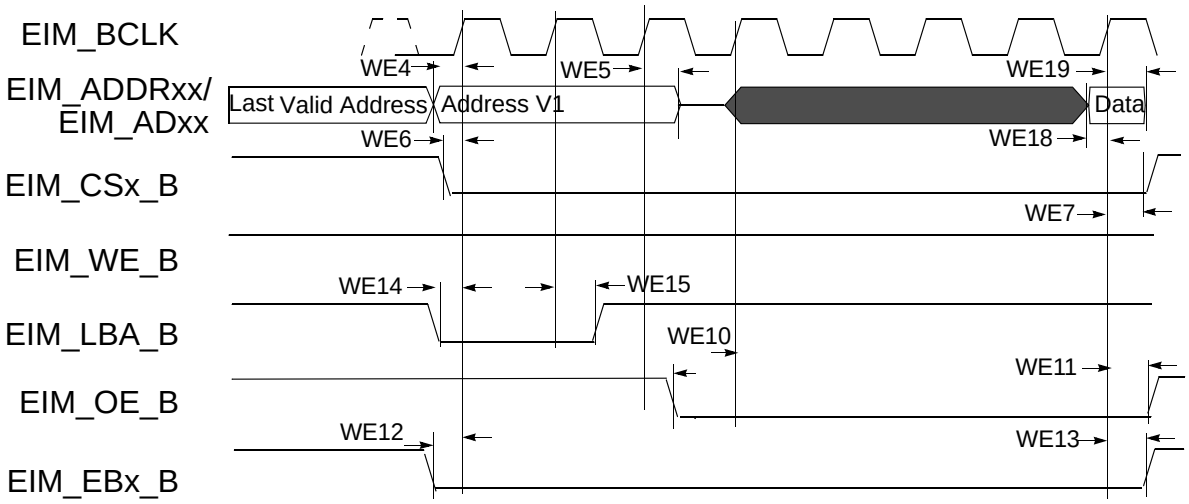


Figure 18. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.4 General EIM Timing-Asynchronous Mode

Figure 19 through Figure 23, and Table 43 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 19 through Figure 22 as RWSC, OEN and CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

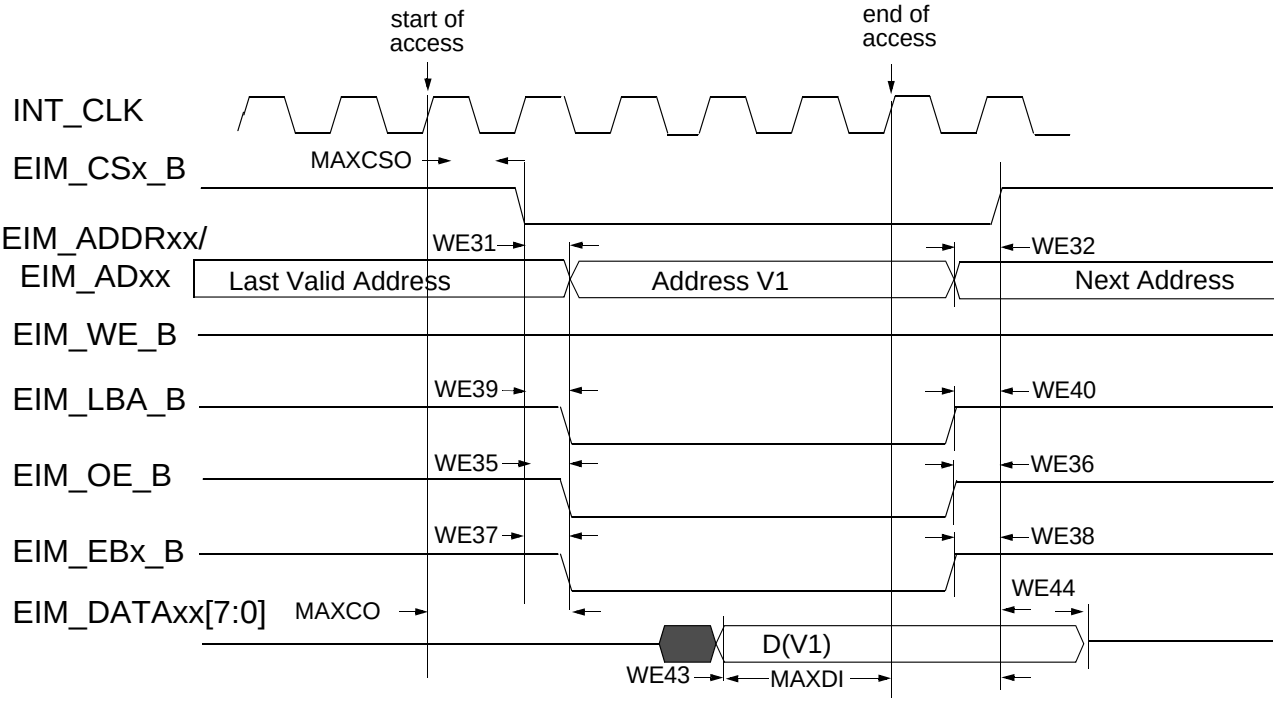


Figure 19. Asynchronous Memory Read Access (RWSC = 5)

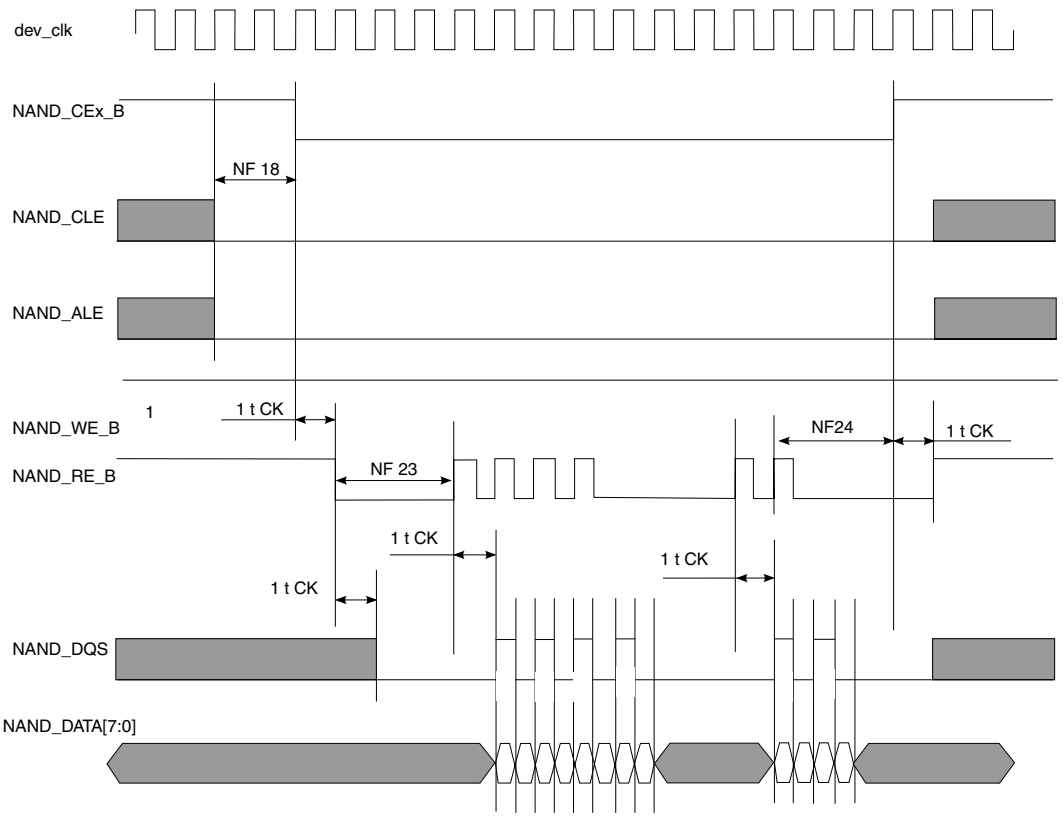


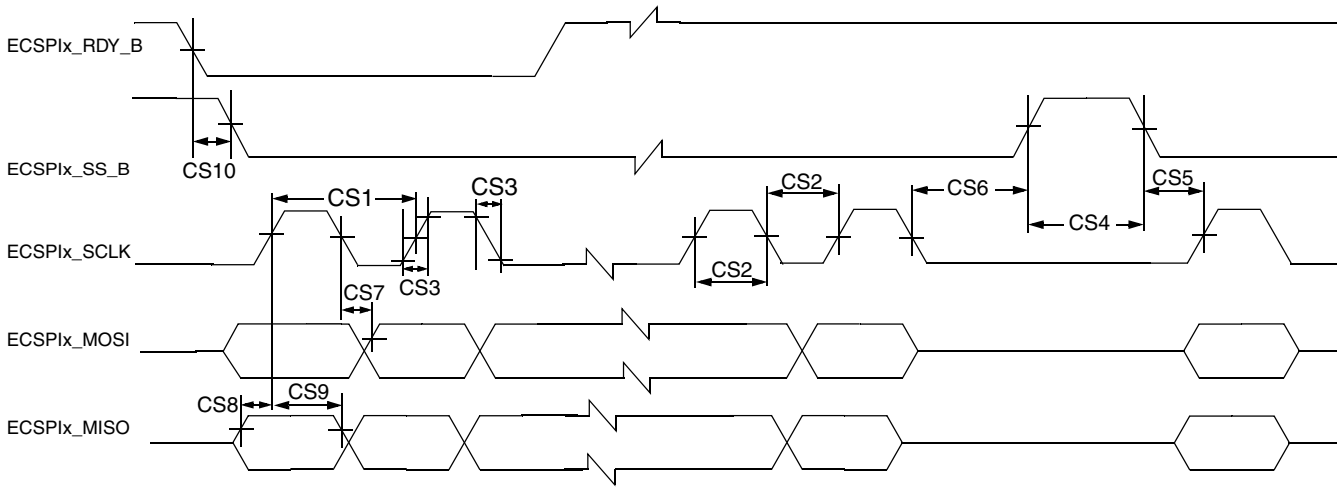
Figure 35. Samsung Toggle Mode Data Read Timing

Table 48. Samsung Toggle Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see 3,2]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see 2]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see 2]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see 2]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see 2]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see 4,2]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see 5,2]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see 2]	—	ns

4.11.2.1 ECSPI Master Mode Timing

Figure 36 depicts the timing of ECSPI in master mode. Table 49 lists the ECSPI master mode timing characteristics.



Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 36. ECSPI Master Mode Timing Diagram

Table 49. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time •	t_{Smiso}	18	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

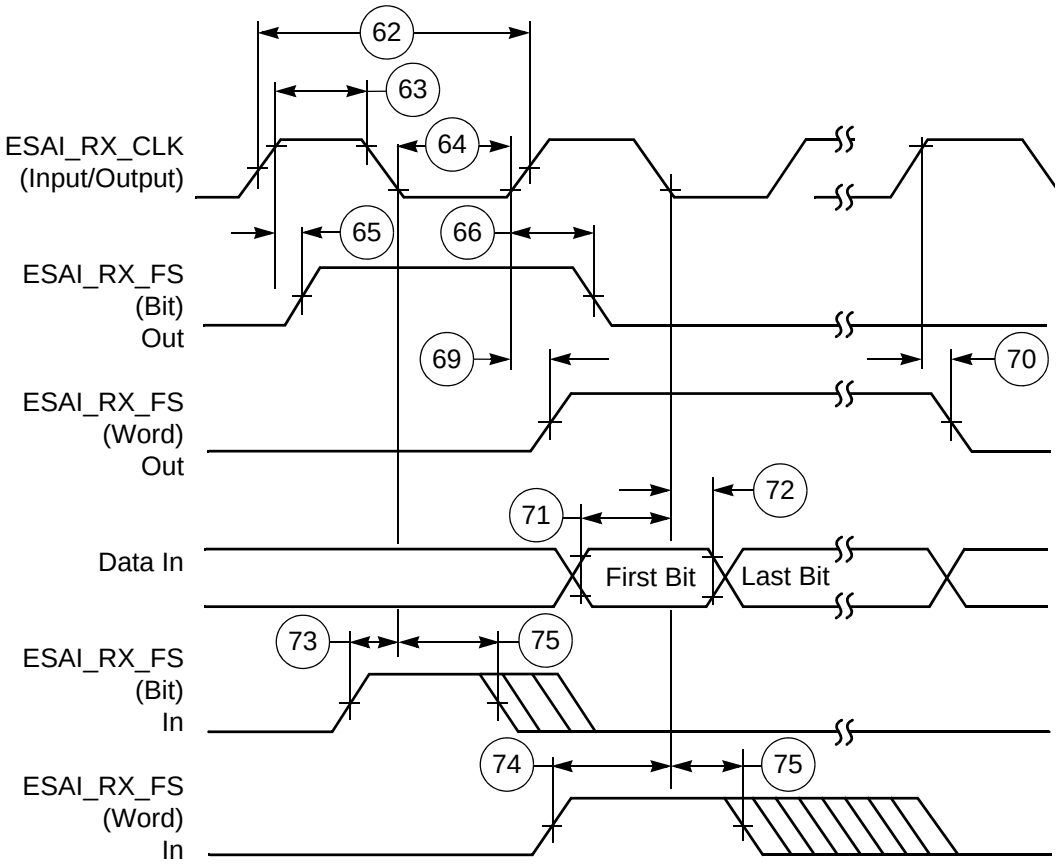


Figure 39. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41 (Dual Date Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 40 depicts the timing of SD/eMMC4.3, and Table 52 lists the SD/eMMC4.3 timing characteristics.

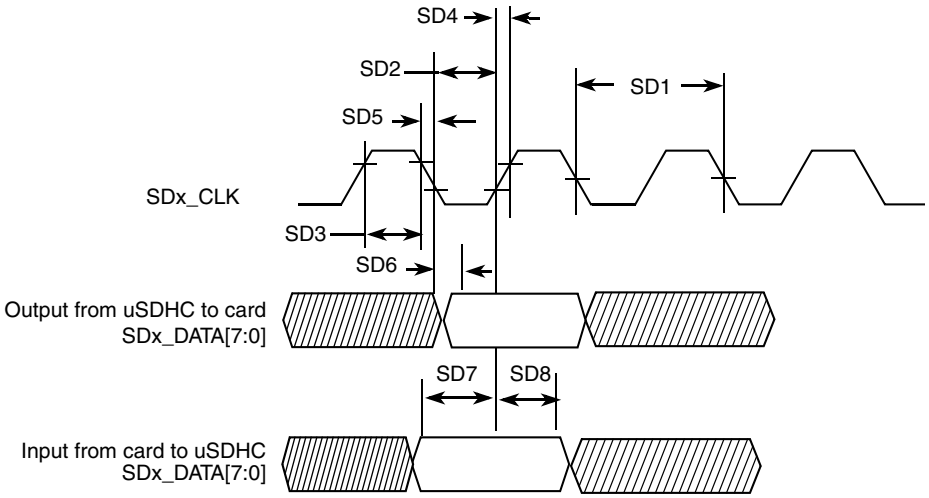


Figure 40. SD/eMMC4.3 Timing

Table 52. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 52. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

Figure 41 depicts the timing of eMMC4.4/4.41. Table 53 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

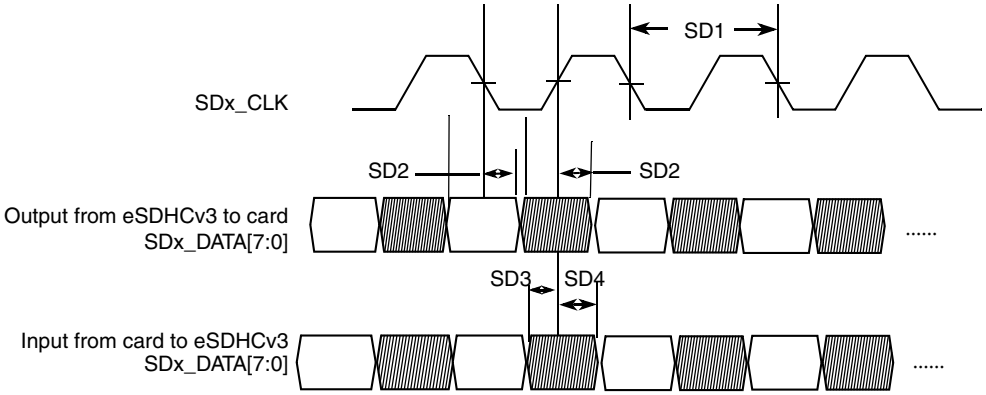


Figure 41. eMMC4.4/4.41 Timing

Table 53. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

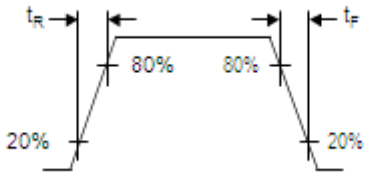


Figure 58. TMDS Output Signals Rise and Fall Time Definition

Table 62. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 54.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 54.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 54.	4	5	6	UI[1]
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 54.	4	5	6	UI[1]
—	TMDSCLK jitter[2]	RL = 50 Ω	—	—	0.25	UI[1]
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 56.	—	—	0.15	UI[1]
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 57.	—	—	1	UI[1]
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 58.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 58.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%

1 UI means TMDS clock unit.

2 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

Table 71. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}		30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—		—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—		ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz

4.11.21.2 Receive Timing

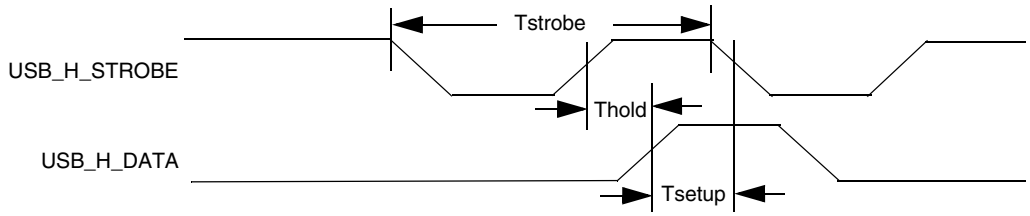


Figure 100. USB HSIC Receive Waveform

Table 92. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point
Tsetup	data setup time	365	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification

— Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  — Revision 1.2, December 7, 2010
  — Portable device only

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 93 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 93. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	N/A
BOOT_MODE0	Input	N/A
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	EIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	EIM_CS0	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	EIM_CS1	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	GPIO3_IO16	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	GPIO3_IO17	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	GPIO3_IO18	Input	100 kΩ pull-up
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	GPIO3_IO19	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	GPIO3_IO20	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	GPIO3_IO21	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	GPIO3_IO22	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	GPIO3_IO23	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	GPIO3_IO24	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	GPIO3_IO25	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	GPIO3_IO26	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	GPIO3_IO27	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	GPIO3_IO28	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	GPIO3_IO29	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	GPIO3_IO30	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	GPIO3_IO31	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	EIM_AD00	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	EIM_AD01	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	EIM_AD10	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	EIM_AD11	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	EIM_AD12	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	EIM_AD13	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	EIM_AD14	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	EIM_AD15	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	EIM_AD02	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	EIM_AD03	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	EIM_AD04	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	EIM_AD05	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	EIM_AD06	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	EIM_AD07	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	EIM_AD08	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	EIM_AD09	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	EIM_EB0	Output	High

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_EB1	K23	NVCC_EIM	GPIO	ALT0	EIM_EB1	Output	High
EIM_EB2	E22	NVCC_EIM	GPIO	ALT5	GPIO2_IO30	Input	100 kΩ pull-up
EIM_EB3	F23	NVCC_EIM	GPIO	ALT5	GPIO2_IO31	Input	100 kΩ pull-up
EIM_LBA	K22	NVCC_EIM	GPIO	ALT0	EIM_LBA	Output	High
EIM_OE	J24	NVCC_EIM	GPIO	ALT0	EIM_OE	Output	High
EIM_RW	K20	NVCC_EIM	GPIO	ALT0	EIM_RW	Output	High
EIM_WAIT	M25	NVCC_EIM	GPIO	ALT0	EIM_WAIT	Input	100 kΩ pull-up
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	100 kΩ pull-up
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	100 kΩ pull-up
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	100 kΩ pull-up
ENET_REF_CLK[3]	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	100 kΩ pull-up
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	100 kΩ pull-up
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	100 kΩ pull-up
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	100 kΩ pull-up
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	100 kΩ pull-up
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	100 kΩ pull-up
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	100 kΩ pull-up
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	100 kΩ pull-down
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	100 kΩ pull-up
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	100 kΩ pull-up
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	100 kΩ pull-up
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	100 kΩ pull-up
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	100 kΩ pull-up
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	100 kΩ pull-up
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	100 kΩ pull-up
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	100 kΩ pull-up
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	100 kΩ pull-up
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	100 kΩ pull-up
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	100 kΩ pull-up
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	100 kΩ pull-up
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	J6	HDMI	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	K5	HDMI	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	K6	HDMI	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	J3	HDMI	—	—	HDMI_TX_DATA1_N	—	—

7 Revision History

Table 101 provides the current revision history for this data sheet. Table 102 provides a revision history for previous revisions.

Table 101. i.MX 6Solo/6DualLite Data Sheet Document Rev. 8 History

Rev. Number	Date	Substantive Changes
8	09/2017	• Replaced ipp_dse with DSE throughout. • Section 1, “Introduction: Replaced text “low voltage DDR3” with “DDR3L” in the features list of i.MX 6Solo/6DualLite applications processors. • Table 1, "Example Orderable Part Numbers," on page 3: Added orderable part numbers. • Figure 1: Updated to include Rev 1.4 in Silicon Revision section. • Section 2.1, “Block Diagram: Updated WEIM with EIM in the block diagram. • Table 2, "i.MX 6Solo/6DualLite Modules List," on page 11: Rearranged alphabetically. • Table 6, "Absolute Maximum Ratings," on page 24: – Removed VDD_HIGH_IN supply voltage (LDO bypass) parameter. – Max. value of VDD_HIGH_CAP supply output voltage corrected to 2.85V. • Table 22: Updated test condition of “XTALI input leakage current at startup” parameter; replaced 32KHz RTC with 24MHz. • Added Section 4.6.4, “RGMII I/O 2.5V I/O DC Electrical Parameters. • Section 4.8.2, “DDR I/O Output Buffer Impedance: Modified introductory text. • Corrected Figure 22, "Asynchronous A/D Muxed Write Access," on page 60. • Table 53, "eMMC4.4/4.41 Interface Timing Specification," on page 80: – Added the following footnote to Card Input Clock section: 1 Clock duty cycle will be in the range of 47% to 53%. – Min. value of uSDHC Input Setup Time reduced to 1.7ns.

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
6	8/2016	• Changed throughout: - LVDDR3 to DDR3L - Changed terminology from “floating” to “not connected”. • Table 1, "Example Orderable Part Numbers," on page 3”: Added (6) part numbers MCIMX6_10AC. • Table 2, "i.MX 6Solo/6DualLite Modules List," on page 11: - uSDHC1–4, SD/MMC and SDXC Enhanced Multi-Media Card/Secure Digital Host Controller row: Added new bullet at top: “Conforms to the SD Host Controller…”. - eCSPI1-4 row: removed from the Brief Description column, “with data rate up to 52Mbit/s.” - BCH row, removed from Brief Description column, “encryption/decryption”. • Table 3, "Special Signal Considerations," on page 21: - GPANAIO row, modified remarks to be NXP use only. - SRC_POR_B row: removed reference to internal POR which is not supported on device. - TEST_MODE row: modified remarks to be NXP use only and added tie to Vss or remain unconnected. • Table 6, "Absolute Maximum Ratings," on page 24” throughout table: clarified parameter descriptions including adding LDO state. Clarified symbol names. - Added row, RGMII I/O supply voltage. - MLB I/O supply voltage combined with LVDS I/O supply voltage - Added VDD_HIGH_CAP supply voltage row for LDO output. - Added to USB supply voltage row: USB_OTG_CHD_B. - All maximum voltages increased (improved). • Section 4.1.2, “Thermal Resistance: added NOTE. • Table 8, "Operating Ranges," on page 26: Added Run mode: LDO enable option for 996 MHz. • Table 8, "Operating Ranges," on page 26: Changed minimum parameter of Run mode: LDO enabled from 1.175 to 1.25 V. • Section 4.2.1, “Power-Up Sequence”: Removed references to the internal POR function. Internal POR is not supported. Removed fourth and fifth bullets. • Section 4.2.3, “Power Supplies Usage”: Added NOTE, “When the PCIE interface is not used…”. • Section 4.5.2, “OSC32K”: Removed battery resistor (coin cell) calculation. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters”: - Added 3 rows: Input capacitance; Startup current; and DC input current. - Added footnote to RTC_XTALI high-level DC input voltage at the Max parameter. - Added NOTE following table: “The Vil and Vih only apply when external clock source is used…”. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”: this new section added, replacing the original section 4.9.4 “DDR SRAM Specific Parameters (DDR3/DDR3L and LPDDR2)”. • Figure 36, "ECSPI Master Mode Timing Diagram," on page 73: Added note, “ECSPI_MOSI always…”. • Figure 37, "ECSPI Slave Mode Timing Diagram," on page 74: Added note, “ECSPI_MOSI always driven…”. • Figure 42, "SDR50/SDR104 Timing," on page 81: Aligned SD4 and SD5. • Table 54, "SDR50/SDR104 Interface Timing Specification," on page 81: - Corrected Clock High Time ID to SD3. - Changed SD2 and SD3 Min and max values to 0.46 and 0.54. - Changed SD5 Max to 0.74. • Table 64, "Camera Input Signal Cross Reference, Format, and Bits Per Cycle," on page 93: Changed RGB565 column heading from 2 to 1 cycle. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: - Table row: DRAM_SDCLK0 and DRAM_SDCLK1 changed Out of Reset Condition from Low to 0. - Added to ZQPAD row: requirement to add resistor to GND.
5	6/2015	• Table 8, “Operating Ranges,” Run mode: LDO enabled row; Changed comments for VDD_ARM_IN, from “1.05V minimum for operation up to 396MHz” to “1.125V minimum for operation up to 396MHz”. • Table 3, “Special Signal Considerations,” XTALI/XTALO row: Changed from “The crystal must be rated...”, to “See Hardware Development Guide”.