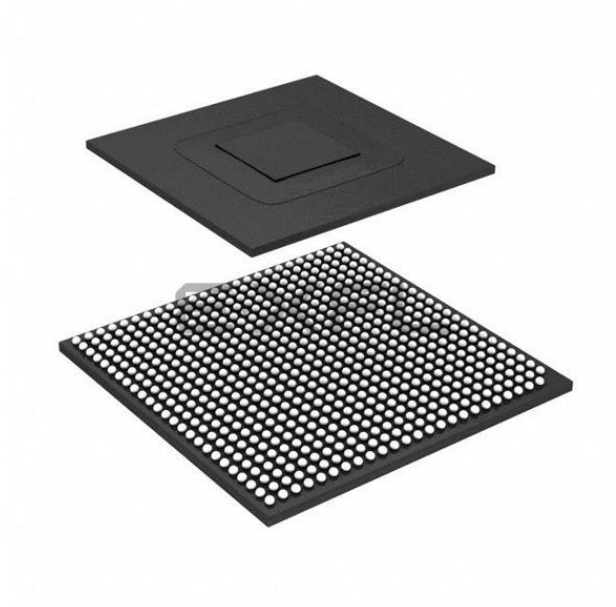

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

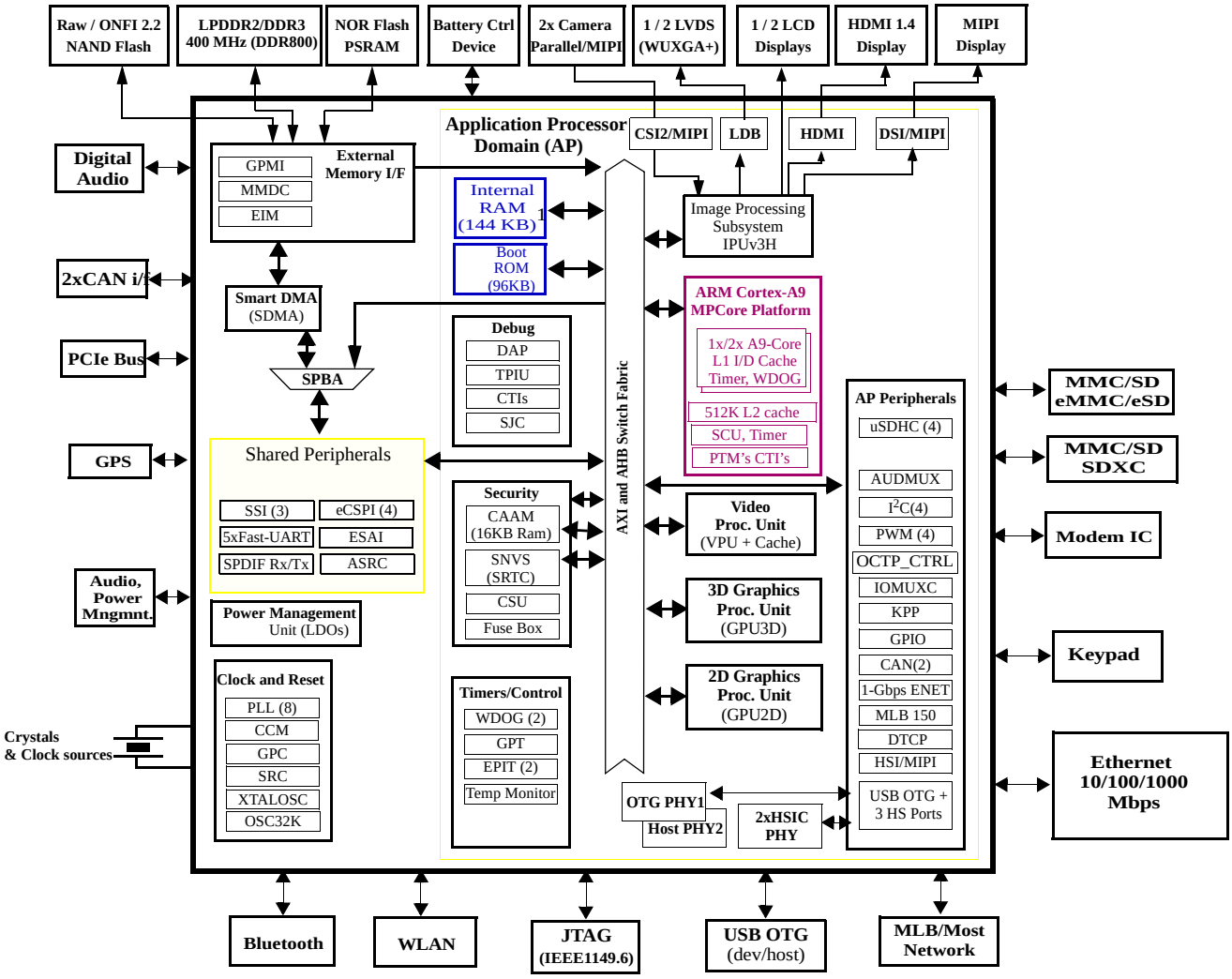
Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u6avm08adr

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 3 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



1 144 KB RAM including 16 KB RAM inside the CAAM.

2 For i.MX 6Solo, there is only one A9-core platform in the chip; for i.MX 6DualLite, there are two A9-core platforms.

Figure 3. i.MX 6Solo/6DualLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

4.1.5 Maximum Supply Currents

The Power Virus numbers shown in Table 10 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 10, however a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 10. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	i.MX 6DualLite: 996 MHz ARM clock based on Power Virus operation	2200	mA
	i.MX 6Solo: 996 MHz ARM clock based on Power Virus operation	1320	mA
VDD_SOC_IN	996 MHz ARM clock	1260	mA
VDD_HIGH_IN	—	125[1]	mA
VDD_SNVS_IN	—	275[2]	µA
USB_OTG_VBUS/ USB_H1_VBUS (LDO 3P0)	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	—
NVCC_ENET	N=10	Use maximum IO equation[5]	—
NVCC_LCD	N=29	Use maximum IO equation[5]	—
NVCC_GPIO	N=24	Use maximum IO equation[5]	—
NVCC_CSI	N=20	Use maximum IO equation[5]	—
NVCC_EIM	N=53	Use maximum IO equation[5]	—
NVCC_JTAG	N=6	Use maximum IO equation[5]	—
NVCC_RGMII	N=6	Use maximum IO equation[5]	—
NVCC_SD1	N=6	Use maximum IO equation[5]	—
NVCC_SD2	N=6	Use maximum IO equation[5]	—
NVCC_SD3	N=11	Use maximum IO equation[5]	—
NVCC_NANDF	N=26	Use maximum IO equation[5]	—

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 19. MLB PLL's Electrical Parameters

Parameter	Value
Lock time	<1 ms

4.4.6 ARM PLL

Table 20. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM. Maximum operating frequency for EIM data transfer is 104 MHz. Two system clocks are used with the EIM:

- ACLK_EIM_SLOW_CLK_ROOT is used to clock the EIM module.
  The maximum frequency for CLK_EIM_SLOW_CLK_ROOT is 132 MHz.
- ACLK_EXSC is also used when the EIM is in synchronous mode.
  The maximum frequency for ACLK_EXSC is 104 MHz.

Timing parameters in this section that are given as a function of register settings.

4.9.3.1 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 41 provides EIM interface pads allocation in different modes.

Table 41. EIM Internal Module Multiplexing[1]

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
EIM_ADDR [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]	EIM_AD [15:00]
EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_ADDR [25:16]	EIM_DATA [09:00]
EIM_DATA [07:00], EIM_EB0_B	EIM_DATA [07:00]	—	—	—	EIM_DATA [07:00]	—	EIM_DATA [07:00]	EIM_AD [07:00]	EIM_AD [07:00]
EIM_DATA [15:08], EIM_EB1_B	—	EIM_DATA [15:08]	—	—	EIM_DATA [15:08]	—	EIM_DATA [15:08]	EIM_AD [15:08]	EIM_AD [15:08]
EIM_DATA [23:16], EIM_EB2_B	—	—	EIM_DATA [23:16]	—	—	EIM_DATA [23:16]	EIM_DATA [23:16]	—	EIM_DATA [07:00]
EIM_DATA [31:24], EIM_EB3_B	—	—	—	EIM_DATA [31:24]	—	EIM_DATA [31:24]	EIM_DATA [31:24]	—	EIM_DATA [15:08]

[1] For more information on configuration ports mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 13, Figure 14, and Table 42 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

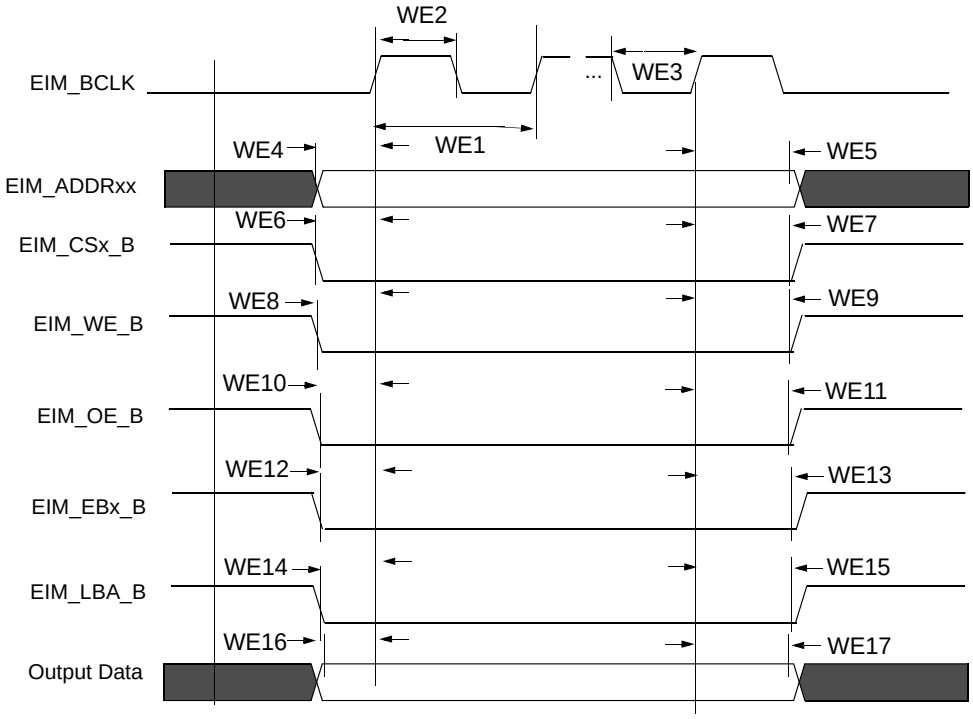


Figure 13. EIM Outputs Timing Diagram

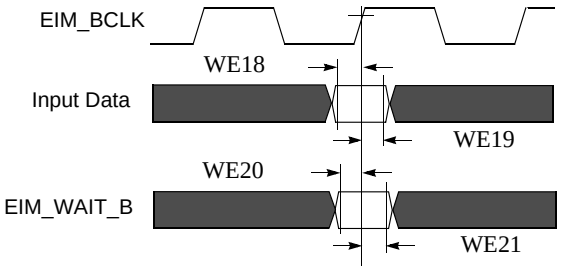


Figure 14. EIM Inputs Timing Diagram

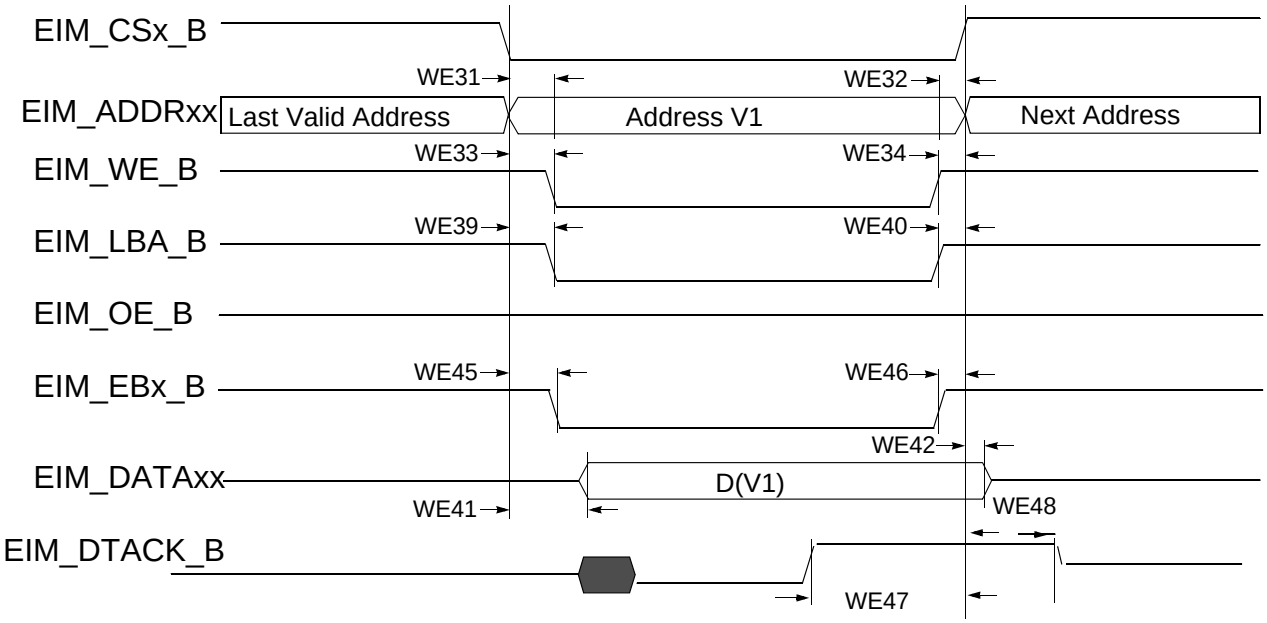


Figure 24. DTACK Mode Write Access (DAP=0)

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4 - WE6 - CSA[2]	—	3 - CSA	ns
WE32	Address Invalid to EIM_CSx_B invalid	WE7 - WE5 - CSN[3]	—	3 - CSN	ns
WE32A (muxed A/D	EIM_CSx_B valid to Address Invalid	t[4] + WE4 - WE7 + (ADVN[5] + ADVA[6] + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN_WCSN)	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-RCSA)	3 + (OEA + RADVN+RADVA+ADH +1-RCSA)	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns

Table 43. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN- RCSN)	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal FF	5	—	—	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	MAXIMUM delay from EIM_DTACK_B to its internal FF + 2 cycles for synchronization	10	—	—	—

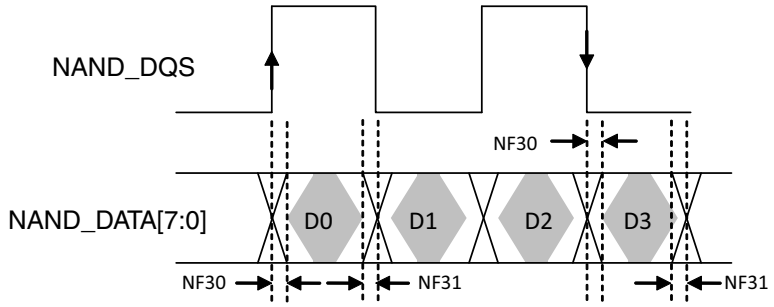


Figure 33. NAND_DQS/NAND_DQ Read Valid Window

Table 47. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		
NF29	Data write hold	—	0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	

1 GPMI's source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) -0.075ns (half of maximum p-p jitter).

For DDR Source sync mode, Figure 33 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

Table 48. Samsung Toggle Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS).

6 Shown in Figure 34, Samsung Toggle Mode Data Write Timing diagram.

7 Shown in Figure 33, NAND_DQS/NAND_DQ Read Valid Window.

For DDR Toggle mode, Figure 33 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

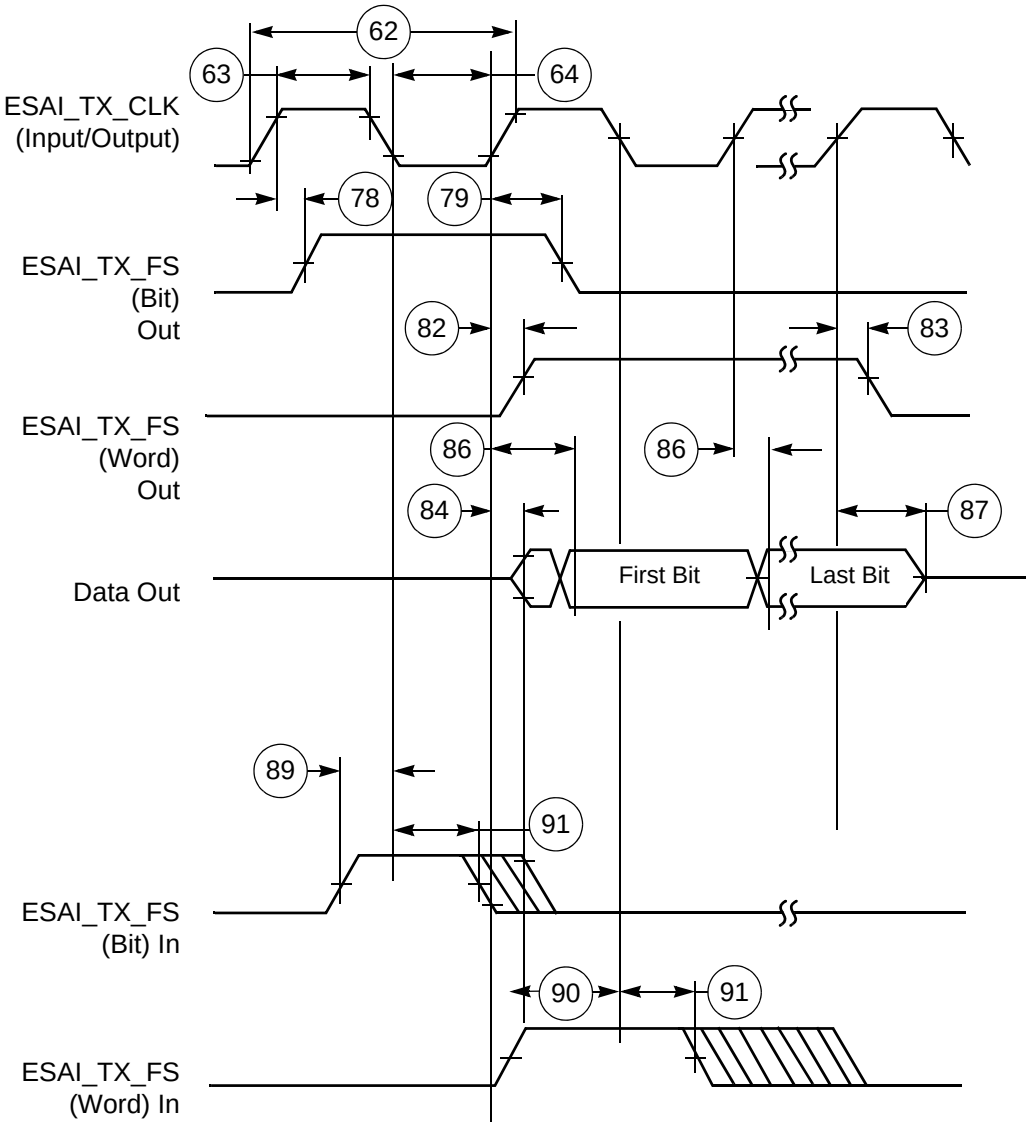


Figure 38. ESAI Transmitter Timing

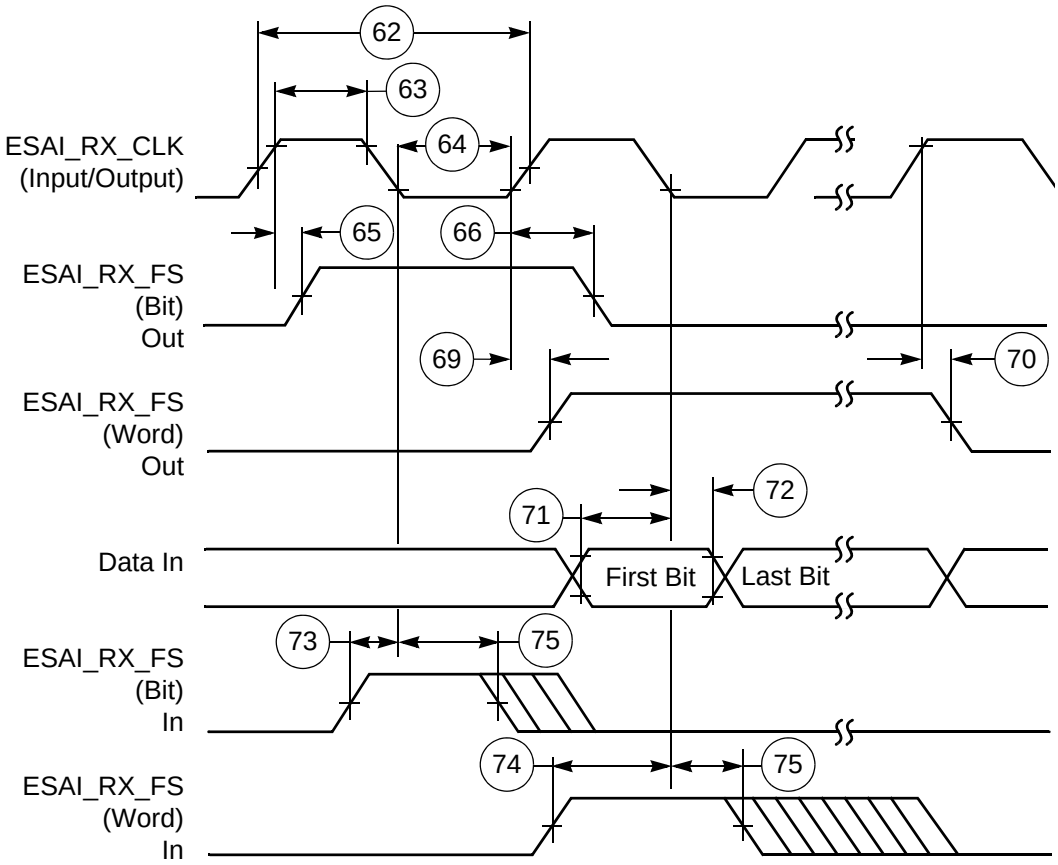


Figure 39. ESAI Receiver Timing

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	RT = 50 Ω For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	avddtmds ± 10 mV			mV
V_{SWING}	Single-ended output swing voltage		400	—	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds ± 10 mV			mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 200 mV	—	avddtmds + 10 mV	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCLK < or = 165 MHz	avddtmds - 600 mV	—	avddtmds - 400mV	mV
		If attached sink supports TMDSCLK > 165 MHz	avddtmds - 700 mV	—	avddtmds - 400 mV	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see Figure 53). **Note:** R_{TERM} can also be configured to be open and not present on TMDS channels.	—	50	—	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	—	2.0	—	5.3	V
$^{VHPD}_{VL}$	Hot plug detect low range	—	0	—	0.8	V
$^{HPD}_{Z}$	Hot plug detect input impedance	—	10	—	—	kΩ
$^{HPD}_{t}$	Hot plug detect time delay	—	—	—	100	µs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 54 to Figure 58 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

4.11.10.3 Electrical Characteristics

Figure 62 depicts the sensor interface timing. IPUx_CSIx_PIX_CLK signal described here is not generated by the IPU. Table 65 lists the sensor interface timing characteristics.

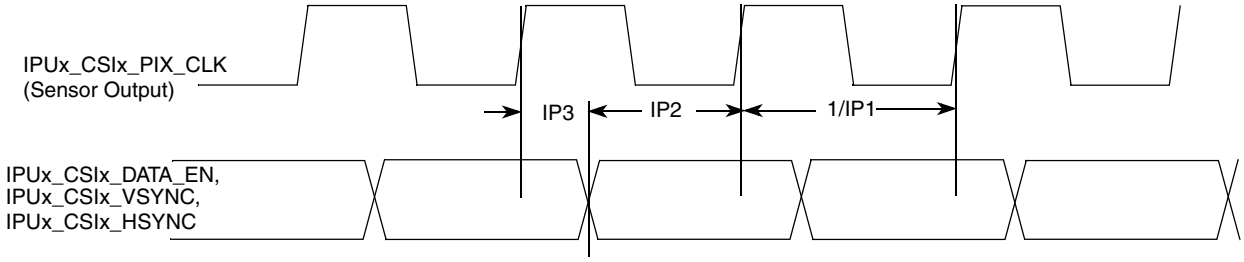


Figure 62. Sensor Interface Timing Diagram

Table 65. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 66 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 66. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment[1,2]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DISPx_DAT00	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	—
IPUx_DISPx_DAT01	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	—
IPUx_DISPx_DAT02	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	—
IPUx_DISPx_DAT03	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	—
IPUx_DISPx_DAT04	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	—
IPUx_DISPx_DAT05	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	—
IPUx_DISPx_DAT06	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	—

Table 71. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
F_{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P_{DDRCLK}	DDR CLK period	80 Ω<= RL< = 125 Ω	2	—	25	ns
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk–pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}		30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—		—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—		ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz

Table 82. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDxRXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDxRXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDxRXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDxRXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDxRXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = ‘0’. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Device Interface Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interface Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	100 kΩ pull-up
Note: DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.							
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	DRAM_DATA32	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	DRAM_DATA33	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	DRAM_DATA34	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	DRAM_DATA35	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	DRAM_DATA36	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	DRAM_DATA37	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	DRAM_DATA38	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	DRAM_DATA39	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	DRAM_DATA40	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	DRAM_DATA41	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	DRAM_DATA42	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	DRAM_DATA43	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	DRAM_DATA44	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	DRAM_DATA45	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	DRAM_DATA46	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	DRAM_DATA47	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	DRAM_DATA48	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	DRAM_DATA49	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	DRAM_DATA50	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	DRAM_DATA51	Input	100 kΩ pull-up

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	EIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	EIM_CS0	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	EIM_CS1	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	GPIO3_IO16	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	GPIO3_IO17	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	GPIO3_IO18	Input	100 kΩ pull-up
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	GPIO3_IO19	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	GPIO3_IO20	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	GPIO3_IO21	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	GPIO3_IO22	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	GPIO3_IO23	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	GPIO3_IO24	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	GPIO3_IO25	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	GPIO3_IO26	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	GPIO3_IO27	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	GPIO3_IO28	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	GPIO3_IO29	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	GPIO3_IO30	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	GPIO3_IO31	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	EIM_AD00	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	EIM_AD01	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	EIM_AD10	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	EIM_AD11	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	EIM_AD12	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	EIM_AD13	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	EIM_AD14	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	EIM_AD15	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	EIM_AD02	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	EIM_AD03	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	EIM_AD04	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	EIM_AD05	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	EIM_AD06	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	EIM_AD07	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	EIM_AD08	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	EIM_AD09	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	EIM_EB0	Output	High

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
6	8/2016	• Changed throughout: - LVDDR3 to DDR3L - Changed terminology from “floating” to “not connected”. • Table 1, "Example Orderable Part Numbers," on page 3”: Added (6) part numbers MCIMX6_10AC. • Table 2, "i.MX 6Solo/6DualLite Modules List," on page 11: - uSDHC1–4, SD/MMC and SDXC Enhanced Multi-Media Card/Secure Digital Host Controller row: Added new bullet at top: “Conforms to the SD Host Controller…”. - eCSPI1-4 row: removed from the Brief Description column, “with data rate up to 52Mbit/s.” - BCH row, removed from Brief Description column, “encryption/decryption”. • Table 3, "Special Signal Considerations," on page 21: - GPANAIO row, modified remarks to be NXP use only. - SRC_POR_B row: removed reference to internal POR which is not supported on device. - TEST_MODE row: modified remarks to be NXP use only and added tie to Vss or remain unconnected. • Table 6, "Absolute Maximum Ratings," on page 24” throughout table: clarified parameter descriptions including adding LDO state. Clarified symbol names. - Added row, RGMII I/O supply voltage. - MLB I/O supply voltage combined with LVDS I/O supply voltage - Added VDD_HIGH_CAP supply voltage row for LDO output. - Added to USB supply voltage row: USB_OTG_CHD_B. - All maximum voltages increased (improved). • Section 4.1.2, “Thermal Resistance: added NOTE. • Table 8, "Operating Ranges," on page 26: Added Run mode: LDO enable option for 996 MHz. • Table 8, "Operating Ranges," on page 26: Changed minimum parameter of Run mode: LDO enabled from 1.175 to 1.25 V. • Section 4.2.1, “Power-Up Sequence”: Removed references to the internal POR function. Internal POR is not supported. Removed fourth and fifth bullets. • Section 4.2.3, “Power Supplies Usage”: Added NOTE, “When the PCIE interface is not used…”. • Section 4.5.2, “OSC32K”: Removed battery resistor (coin cell) calculation. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters”: - Added 3 rows: Input capacitance; Startup current; and DC input current. - Added footnote to RTC_XTALI high-level DC input voltage at the Max parameter. - Added NOTE following table: “The Vil and Vih only apply when external clock source is used…”. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”: this new section added, replacing the original section 4.9.4 “DDR SRAM Specific Parameters (DDR3/DDR3L and LPDDR2)”. • Figure 36, "ECSPI Master Mode Timing Diagram," on page 73: Added note, “ECSPI_MOSI always…”. • Figure 37, "ECSPI Slave Mode Timing Diagram," on page 74: Added note, “ECSPI_MOSI always driven…”. • Figure 42, "SDR50/SDR104 Timing," on page 81: Aligned SD4 and SD5. • Table 54, "SDR50/SDR104 Interface Timing Specification," on page 81: - Corrected Clock High Time ID to SD3. - Changed SD2 and SD3 Min and max values to 0.46 and 0.54. - Changed SD5 Max to 0.74. • Table 64, "Camera Input Signal Cross Reference, Format, and Bits Per Cycle," on page 93: Changed RGB565 column heading from 2 to 1 cycle. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: - Table row: DRAM_SDCLK0 and DRAM_SDCLK1 changed Out of Reset Condition from Low to 0. - Added to ZQPAD row: requirement to add resistor to GND.
5	6/2015	• Table 8, “Operating Ranges,” Run mode: LDO enabled row; Changed comments for VDD_ARM_IN, from “1.05V minimum for operation up to 396MHz” to “1.125V minimum for operation up to 396MHz”. • Table 3, “Special Signal Considerations,” XTALI/XTALO row: Changed from “The crystal must be rated...”, to “See Hardware Development Guide”.