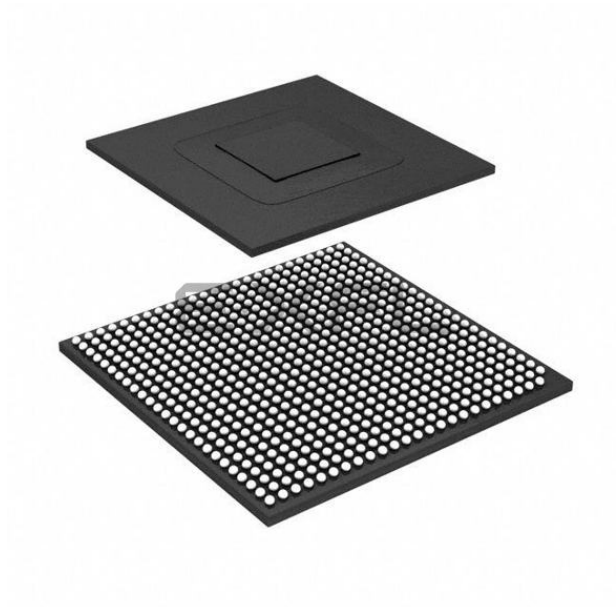

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u6avm10ac

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Solo/6DualLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Solo/6DualLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 8. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supply voltages[9]	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	—
	NVCC_LVDS_2P5[10] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.21	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.21	V	—
Junction temperature	T_J	-40	—	125	°C	See *i.MX 6Solo/6DualLite Product Lifetime Usage Estimates Application Note*, AN4725, for information on product lifetime for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 VDD_ARM_IN and VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

4 In LDO enabled mode, the internal LDO output set points must be configured such that the:

- VDD_ARM LDO output set point does not exceed the VDD_SOC LDO output set point by more than 100 mV.
- VDD_SOC LDO output set point is equal to the VDD_PU LDO output set point.

The VDD_ARM LDO output set point can be lower than the VDD_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

5 When VDD_SOC_IN does not supply PCIE_VP and PCIE_VPTX, or when the PCIe PHY is not used, then this maximum can be 1.3 V.

6 Run mode: LDO Bypassed is not supported for the 1 GHz option.

7 In LDO bypassed mode, the external power supply must ensure that VDD_ARM_IN does not exceed VDD_SOC_IN by more than 100 mV. The VDD_ARM_IN supply voltage can be lower than the VDD_SOC_IN supply voltage. The minimum voltages shown in this table must be maintained.

8 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

9 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a pull-up or pull-down resistor applied to limit any non-connected gate current.

10 This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used.

4.1.4 External Clock Sources

Each i.MX 6Solo/6DualLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

Table 10. Maximum Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_LVDS2P5[6]	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.	—
MISC			
DDR_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown in Table 10. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

6 NVCC_LVDS2P5 is supplied by VDD_HIGH_CAP (by external connection) so the maximum supply current is included in the current shown for VDD_HIGH_IN. The maximum supply current for NVCC_LVDS2P5 has not been characterized separately.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 • HIGH LDO set to 2.5 V • Clocks are gated. • DDR is in self refresh. • PLLs are active in bypass (24MHz) • Supply Voltages remain ON	VDD_ARM_IN (1.4V)	4.5	mA
		VDD_SOC_IN (1.4V)	23	
		VDD_HIGH_IN (3.0V)	13.5	
		Total	79	mW

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, DSE=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, DSE=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, DSE=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. DSE=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC).

Table 31. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V

[1] t is the maximum EIM logic (ACLK_EXSC) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed EIM_BCLK frequency is:

—Fixed latency for both read and write is 104 MHz.

—Variable latency for read only is 104 MHz.

—Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz.Write BCD = 1 and 104 MHz ACLK_EXSC, will result in a EIM_BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

[2] EIM_BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

[3] For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 15 to Figure 18 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

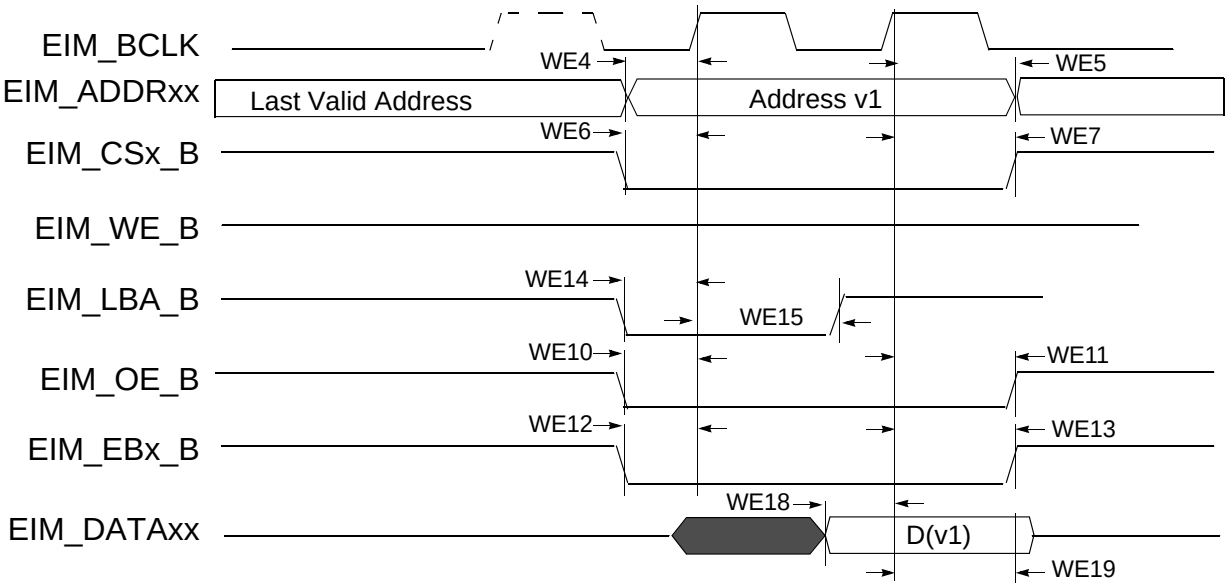

Figure 15. Synchronous Memory Read Access, WSC=1

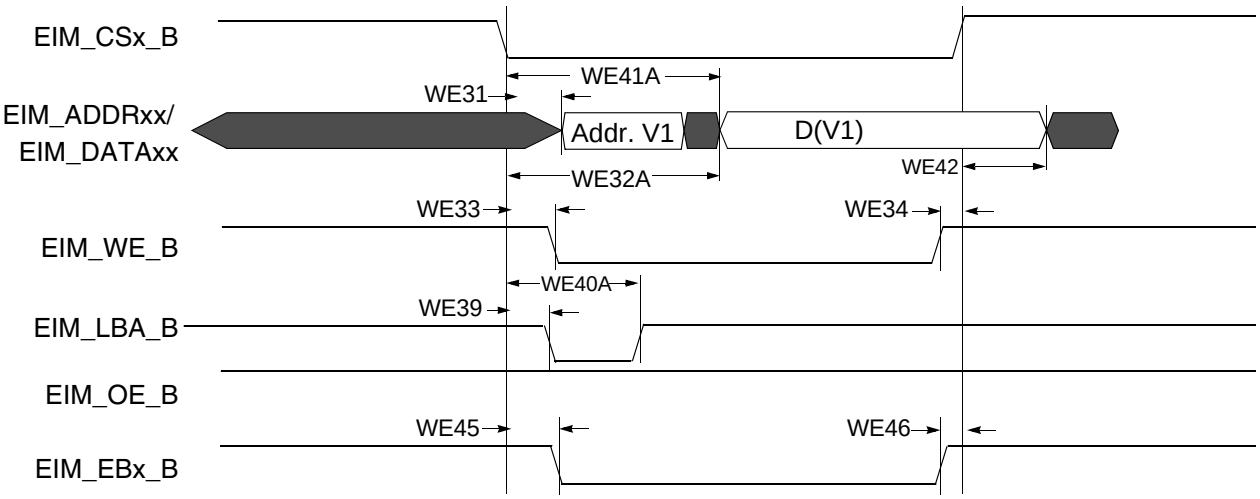

Figure 22. Asynchronous A/D Muxed Write Access

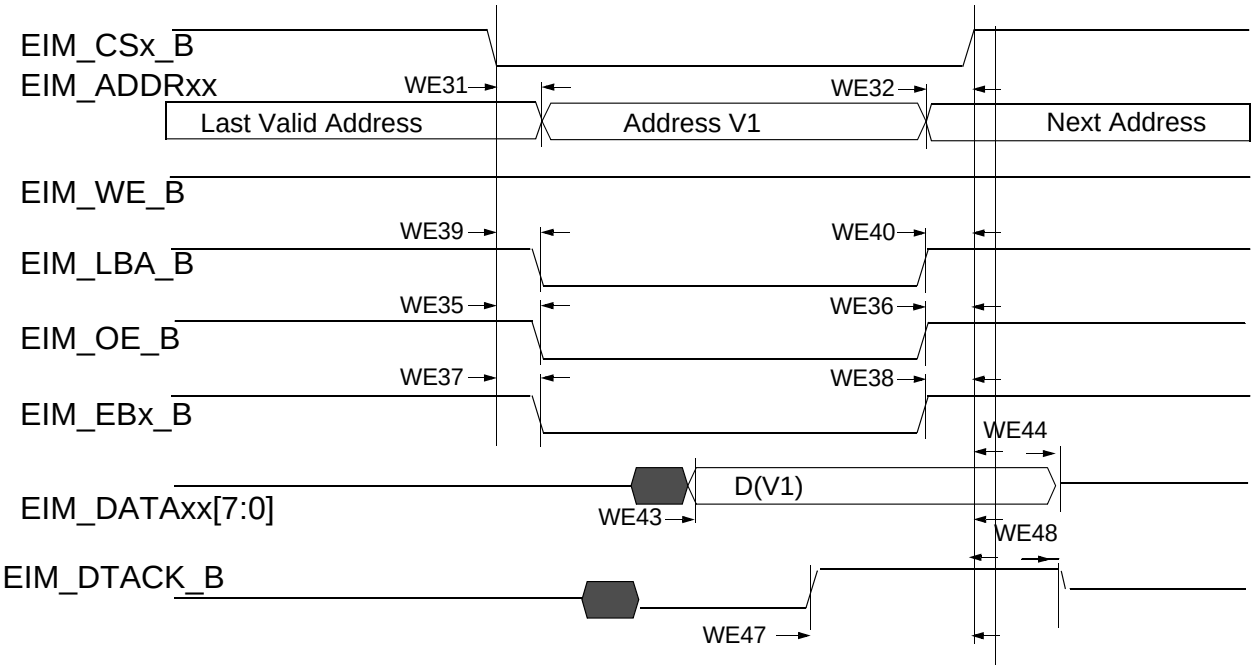

Figure 23. DTACK Mode Read Access (DAP=0)

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min	Max	Unit
M9[1]	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

[1] ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 46 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

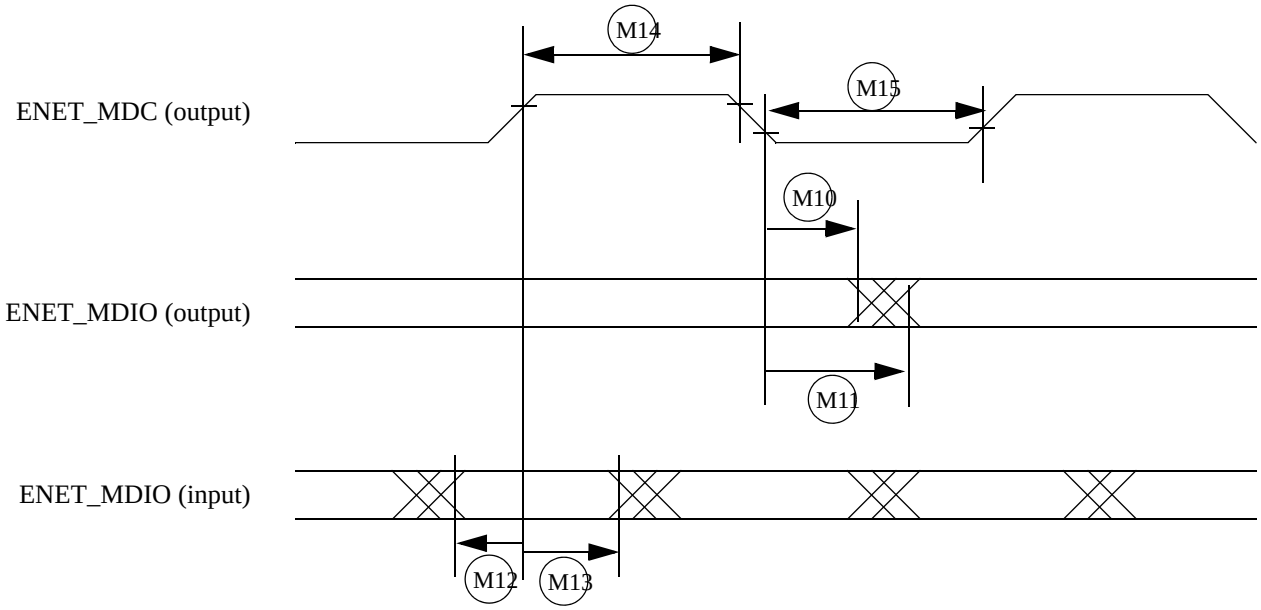

Figure 46. MII Serial Management Channel Timing Diagram

Table 58. MII Serial Management Channel Timing

ID	Characteristic	Min	Max	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

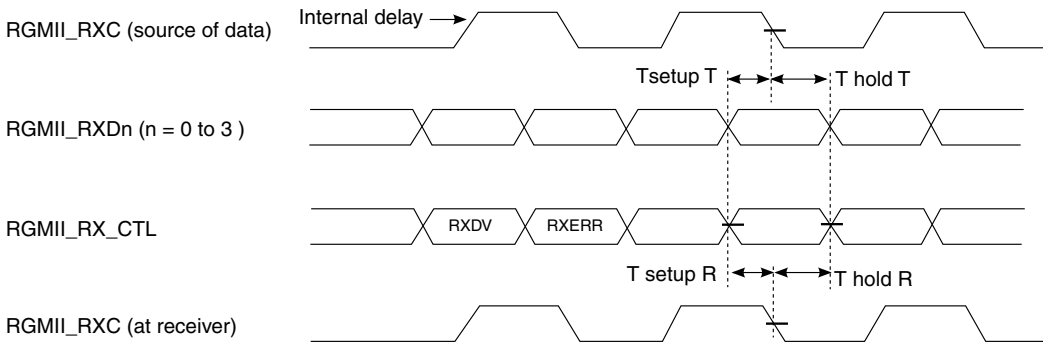

Figure 50. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

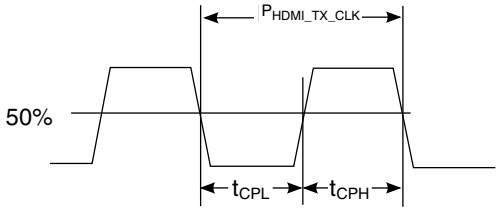

Figure 54. TMDS Clock Signal Definitions

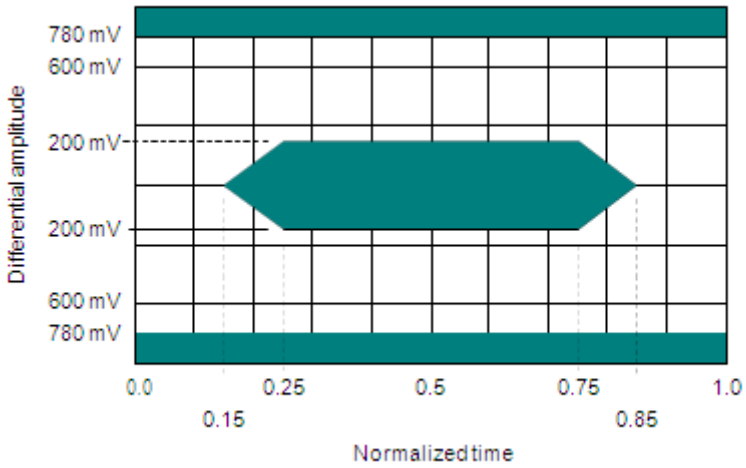

Figure 55. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

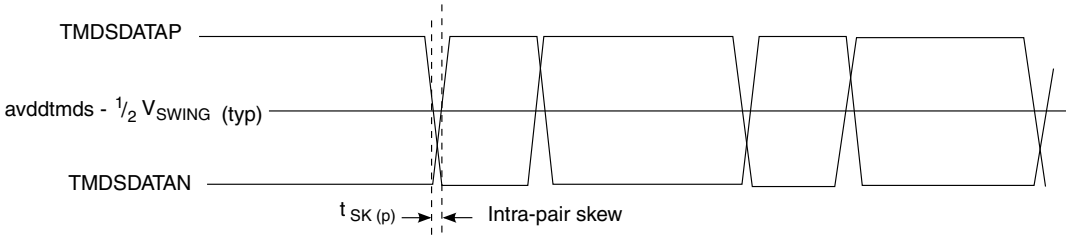

Figure 56. Intra-Pair Skew Definition

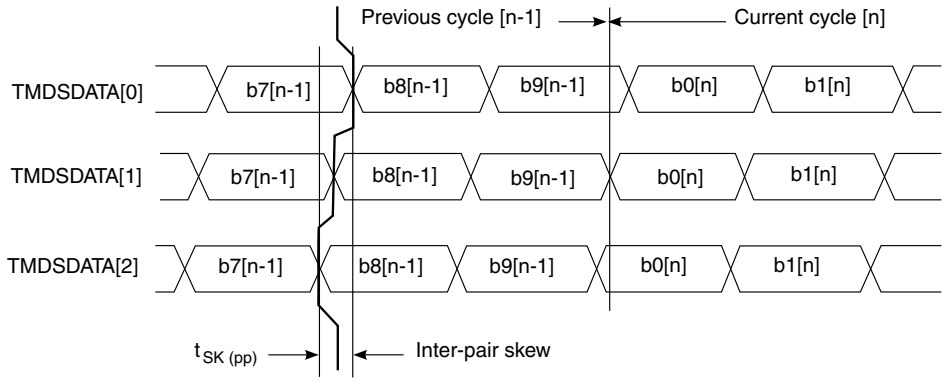

Figure 57. Inter-Pair Skew Definition

4.11.10.2.2 Gated Clock Mode

The IPUx_CSIx_VSYNC, IPUx_CSIx_HSYNC, and IPUx_CSIx_PIX_CLK signals are used in this mode. See Figure 60.

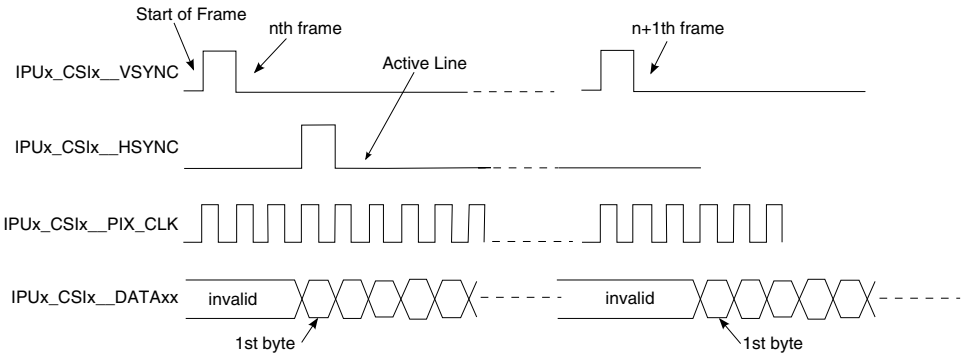

Figure 60. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPUx_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPUx_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPUx_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPUx_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the IPUx_CSIx_HSYNC timing repeats. For the next frame, the IPUx_CSIx_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the IPUx_CSIx_HSYNC signal, which is not used (see Figure 61). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The IPUx_CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

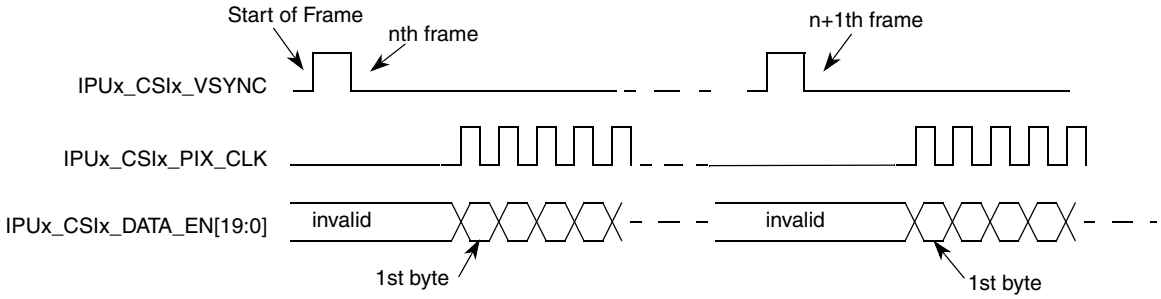

Figure 61. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 61 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered IPUx_CSIx_VSYNC; active-high/low IPUx_CSIx_HSYNC; and rising/falling-edge triggered IPUx_CSIx_PIX_CLK.

corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

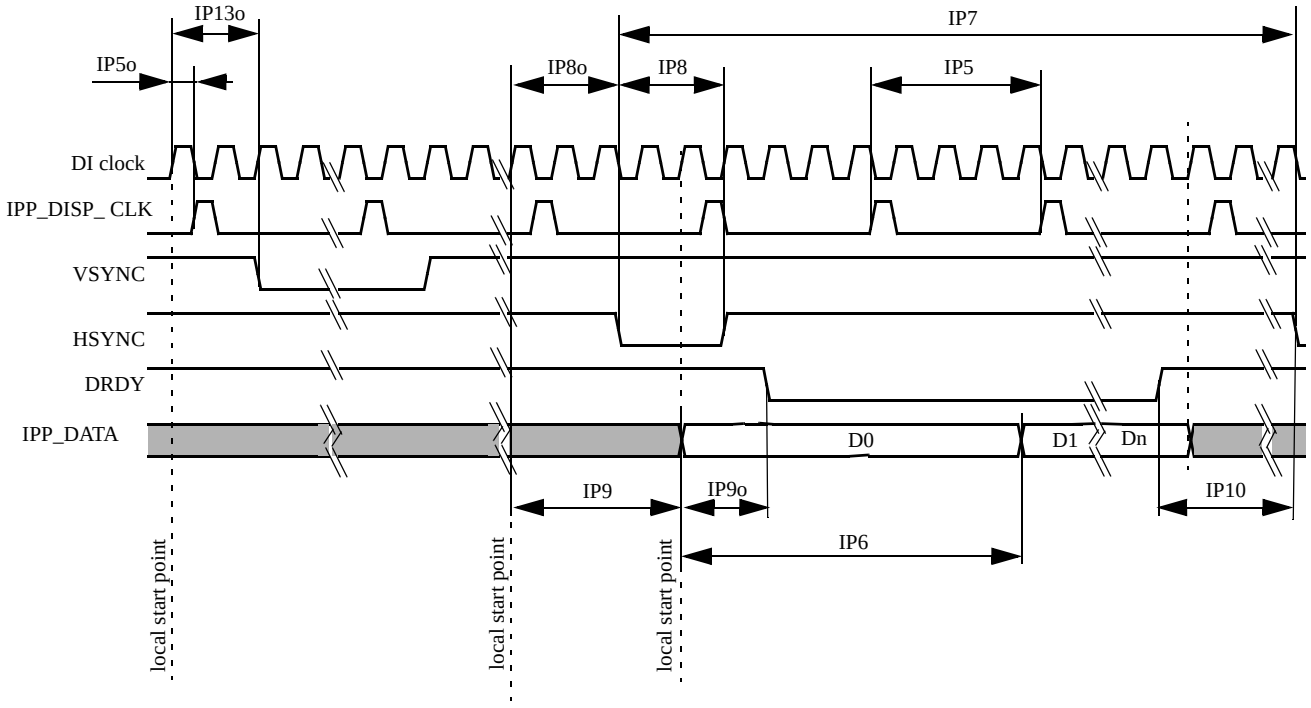

Figure 64. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 65 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

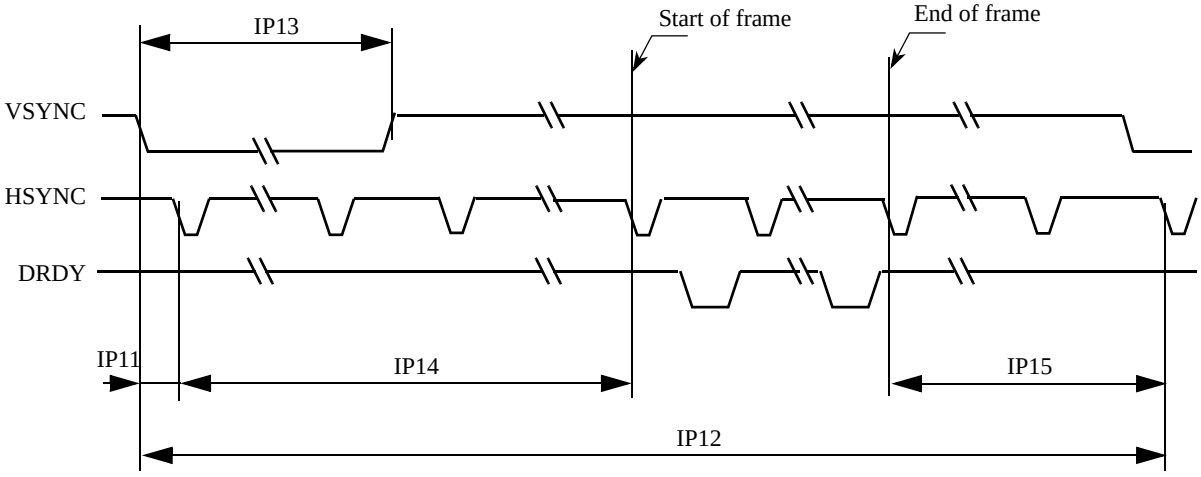

Figure 65. TFT Panels Timing Diagram—Vertical Sync Pulse

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*".

Table 69. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
Input DC Specifications - Apply to DSI_CLK_P/DSI_CLK_N and DSI_DATA_P/DSI_DATA_N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV
V_{LEAK}	Input leakage current	VGNDSH(min) = VI = VGNDSH(max) + VOH(absmax) Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift	—	-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level	—	—	—	1.45	V

4.11.12.8 Reverse High-Speed Data Transmission Timing

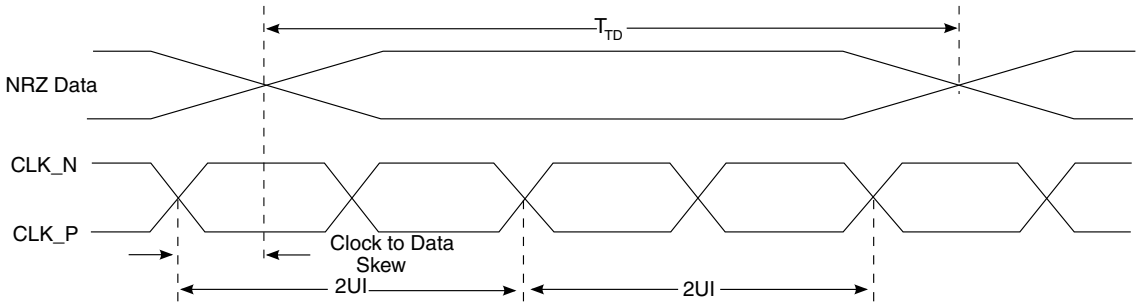

Figure 72. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.9 Low-Power Receiver Timing

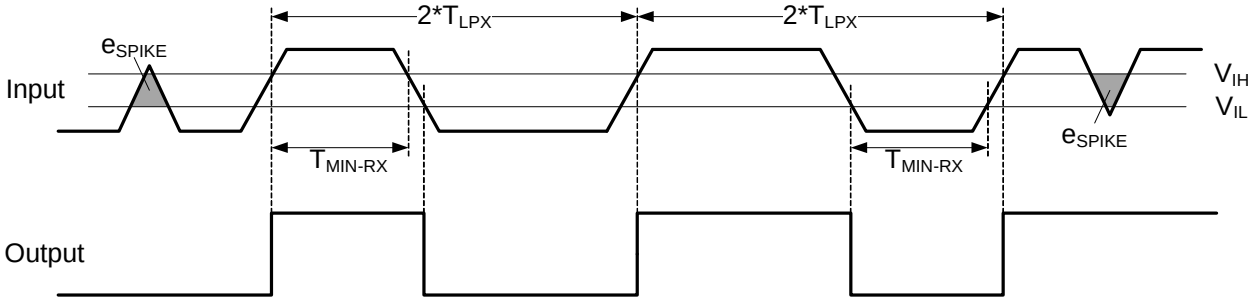

Figure 73. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version1.01.

4.11.13.1 Synchronous Data Flow

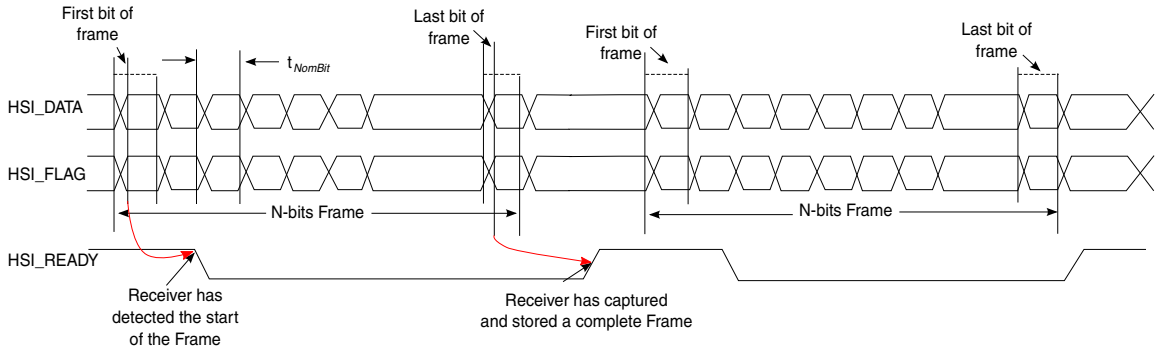

Figure 74. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.5 Stream Transmission Mode Frame Transfer

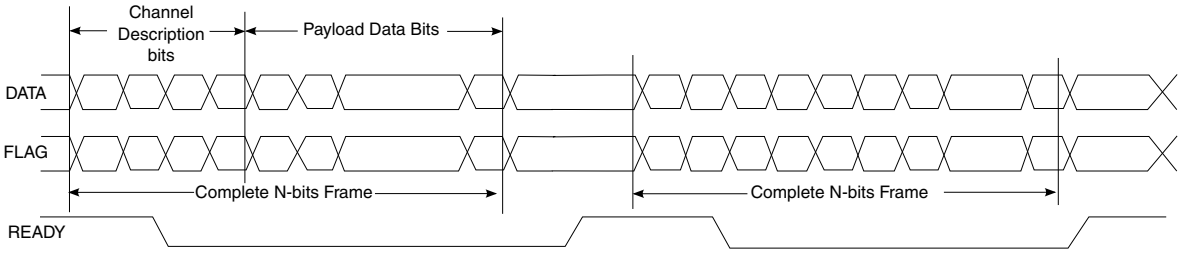

Figure 78. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

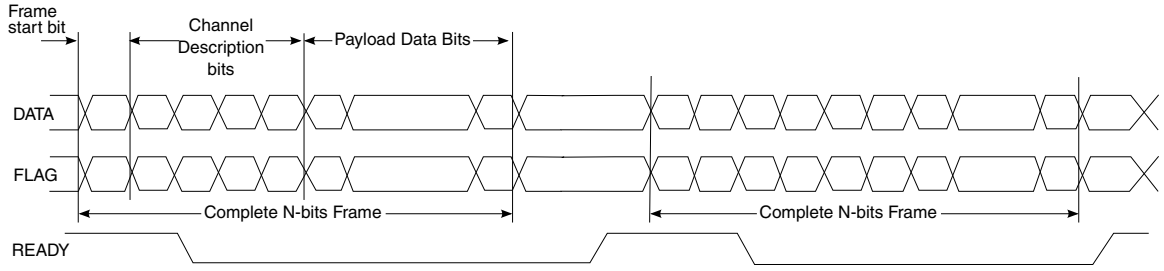

Figure 79. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

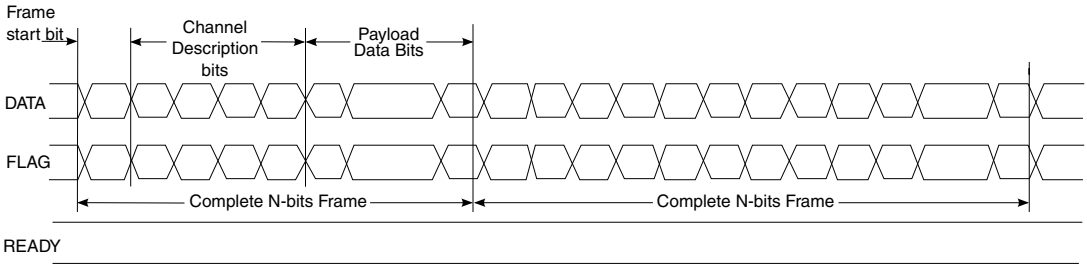

Figure 80. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 72. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns

Table 75. MLB 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	10	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	10.75	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 76; unless otherwise noted.

Table 76. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLB_CLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLB_CLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLB_CLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLB_CLK low time	t_{mckl}	6.1	—	ns	[2]
MLB_CLK high time	t_{mckh}	9.3	—	ns	—
MLB_SIG/MLB_DATA receiver input valid to MLB_CLK falling	t_{dsmcf}	1	—	ns	—
MLB_SIG/MLB_DATA receiver input hold from MLB_CLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLB_SIG/MLB_DATA output high impedance from MLB_CLK low	t_{mcfdz}	0	t_{mckl}	ns	[3]
Bus Hold from MLB_CLK low	t_{mdzh}	2	—	ns	—
MLB_SIG/MLB_DATA output valid from transition of MLB_CLK (low to high)	t_{delay}	—	7	ns	—
Transmitter MLBSIG (MLBDAT) output valid from transition of MLBCLK (low-to-high)	t_{delay}	—	6	ns	—

1 The controller can shut off MLB_CLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLB_CLK.

2 MLB_CLK low/high time includes the pulse width variation.

3 The MediaLB driver can release the MLB_DATA/MLB_SIG line as soon as MLB_CLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh}. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 77 lists the MediaLB 6-pin interface timing characteristics, and Figure 83 shows the MLB 6-pin delay, setup, and hold times.

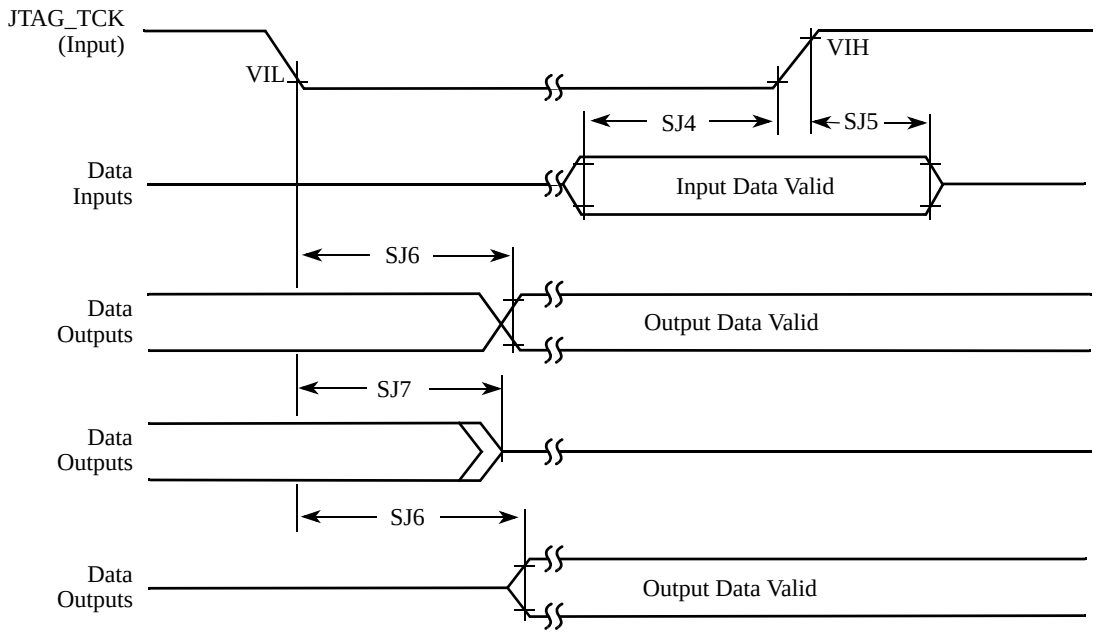

Figure 86. Boundary Scan (JTAG) Timing Diagram

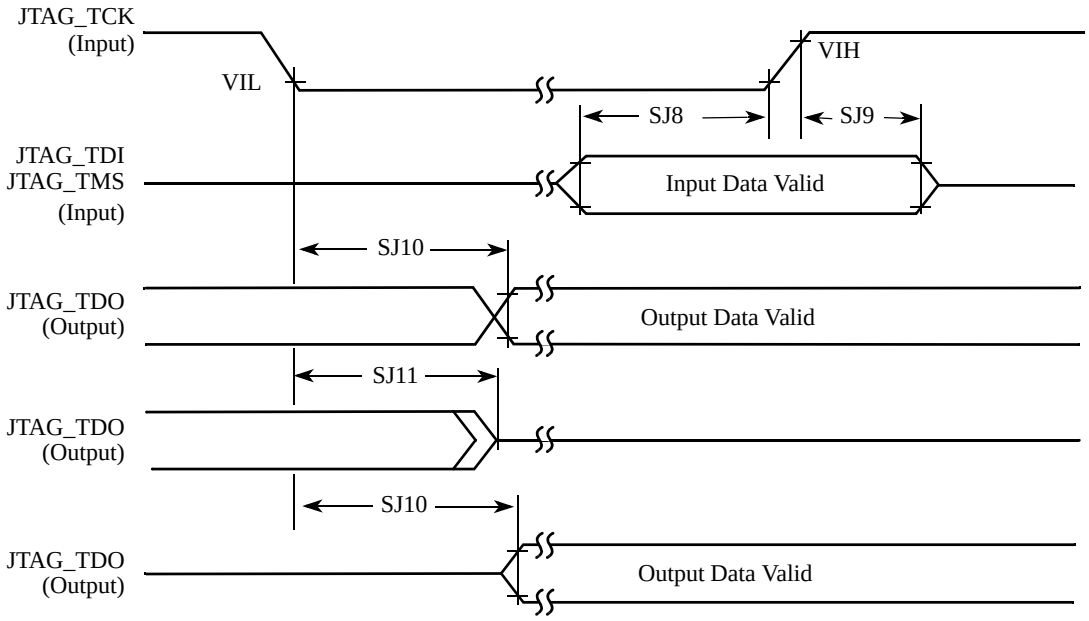

Figure 87. Test Access Port Timing Diagram

Table 85. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	-10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	-10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 97. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
EIM_EB1	K23	NVCC_EIM	GPIO	ALT0	EIM_EB1	Output	High
EIM_EB2	E22	NVCC_EIM	GPIO	ALT5	GPIO2_IO30	Input	100 kΩ pull-up
EIM_EB3	F23	NVCC_EIM	GPIO	ALT5	GPIO2_IO31	Input	100 kΩ pull-up
EIM_LBA	K22	NVCC_EIM	GPIO	ALT0	EIM_LBA	Output	High
EIM_OE	J24	NVCC_EIM	GPIO	ALT0	EIM_OE	Output	High
EIM_RW	K20	NVCC_EIM	GPIO	ALT0	EIM_RW	Output	High
EIM_WAIT	M25	NVCC_EIM	GPIO	ALT0	EIM_WAIT	Input	100 kΩ pull-up
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	GPIO1_IO25	Input	100 kΩ pull-up
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	GPIO1_IO31	Input	100 kΩ pull-up
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	GPIO1_IO22	Input	100 kΩ pull-up
ENET_REF_CLK[3]	V22	NVCC_ENET	GPIO	ALT5	GPIO1_IO23	Input	100 kΩ pull-up
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	GPIO1_IO24	Input	100 kΩ pull-up
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	GPIO1_IO27	Input	100 kΩ pull-up
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	GPIO1_IO26	Input	100 kΩ pull-up
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	GPIO1_IO28	Input	100 kΩ pull-up
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	GPIO1_IO30	Input	100 kΩ pull-up
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	GPIO1_IO29	Input	100 kΩ pull-up
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO00	Input	100 kΩ pull-down
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO01	Input	100 kΩ pull-up
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	GPIO7_IO11	Input	100 kΩ pull-up
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	GPIO7_IO12	Input	100 kΩ pull-up
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	GPIO7_IO13	Input	100 kΩ pull-up
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	GPIO4_IO05	Input	100 kΩ pull-up
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	GPIO1_IO02	Input	100 kΩ pull-up
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	GPIO1_IO03	Input	100 kΩ pull-up
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	GPIO1_IO04	Input	100 kΩ pull-up
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	GPIO1_IO05	Input	100 kΩ pull-up
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO06	Input	100 kΩ pull-up
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	GPIO1_IO07	Input	100 kΩ pull-up
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	GPIO1_IO08	Input	100 kΩ pull-up
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	GPIO1_IO09	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI	—	—	HDMI_TX_CLK_N	—	—
HDMI_CLKP	J6	HDMI	—	—	HDMI_TX_CLK_P	—	—
HDMI_D0M	K5	HDMI	—	—	HDMI_TX_DATA0_N	—	—
HDMI_D0P	K6	HDMI	—	—	HDMI_TX_DATA0_P	—	—
HDMI_D1M	J3	HDMI	—	—	HDMI_TX_DATA1_N	—	—

Table 100. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite (continued)

	N	P	R	T	U	V	W	Y
1	CSI0_DAT4	CSI0_PIXCLK	GPIO_17	GPIO_2	LVDS0_TX0_P	LVDS0_TX2_P	LVDS0_TX3_P	LVDS1_TX0_N
2	CSI0_VSYNC	CSI0_DAT5	GPIO_16	GPIO_9	LVDS0_TX0_N	LVDS0_TX2_N	LVDS0_TX3_N	LVDS1_TX0_P
3	CSI0_DAT7	CSI0_DATA_EN	GPIO_7	GPIO_6	LVDS0_TX1_P	LVDS0_CLK_P	GND	LVDS1_CLK_N
4	CSI0_DAT6	CSI0_MCLK	GPIO_5	GPIO_1	LVDS0_TX1_N	LVDS0_CLK_N	KEY_ROW2	LVDS1_CLK_P
5	CSI0_DAT9	GPIO_19	GPIO_8	GPIO_0	KEY_COL3	KEY_ROW4	KEY_COL0	GND
6	CSI0_DAT8	GPIO_18	GPIO_4	KEY_COL4	KEY_ROW1	KEY_ROW0	KEY_COL2	DRAM_RESET
7	NVCC_CSI	NVCC_GPIO	GPIO_3	KEY_ROW3	KEY_COL1	NVCC_LVDS2P5	GND	DRAM_D20
8	GND	GND	GND	GND	GND	GND	GND	DRAM_D21
9	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_DRAM	GND	DRAM_D19
10	GND	GND	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND	DRAM_D25
11	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	GND	GND	NVCC_DRAM	GND	DRAM_SDCKE0
12	NC	GND	GND	GND	GND	NVCC_DRAM	GND	DRAM_A15
13	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	GND	DRAM_A7
14	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDSOC_CAP	VDDSOC_CAP	NVCC_DRAM	DRAM_A4	DRAM_A3
15	GND	GND	GND	GND	GND	NVCC_DRAM	GND	DRAM_SDBA1
16	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_DRAM	GND	DRAM_CS0
17	VDDPU_CAP	VDDPU_CAP	GND	GND	GND	NVCC_DRAM	GND	DRAM_D36
18	GND	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	DRAM_D37
19	DI0_DISP_CLK	NVCC_LCD	NVCC_ENET	GND	GND	GND	GND	DRAM_D40
20	DI0_PIN3	DISP0_DAT4	DISP0_DAT13	DISP0_DAT21	ENET_TXD0	ENET_MDC	ENET_TXD1	DRAM_D44
21	DI0_PIN15	DISP0_DAT3	DISP0_DAT10	DISP0_DAT16	ENET_CRS_DV	ENET_TX_EN	ENET_RXD0	DRAM_DQM7
22	EIM_BCLK	DISP0_DAT1	DISP0_DAT8	DISP0_DAT15	DISP0_DAT20	ENET_REF_CLK	ENET_RXD1	DRAM_D59
23	EIM_DA14	DISP0_DAT2	DISP0_DAT6	DISP0_DAT11	DISP0_DAT19	ENET_MDIO	ENET_RX_ER	DRAM_D62
24	EIM_DA15	DISP0_DAT0	DISP0_DAT7	DISP0_DAT12	DISP0_DAT17	DISP0_DAT22	DISP0_DAT23	GND
25	DI0_PIN2	DI0_PIN4	DISP0_DAT5	DISP0_DAT9	DISP0_DAT14	DISP0_DAT18	DRAM_D63	DRAM_D58
	N	P	R	T	U	V	W	Y

Table 102. i.MX 6Solo/6DualLite Data Sheet Document Past Revision Histories (continued)

Rev. Number	Date	Substantive Changes
Rev. 4	12/2014	• Table 1, "Example Orderable Part Numbers," on page 3: Speed Grade footnote added as follows: "If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz." • Figure 1, "Part Number Nomenclature—i.MX 6Solo and 6DualLite": Added Silicon Rev 1.3. to diagram • Table 2, Modules List, UART 1–5 Description changed: baud rate up from 5MHz to 5Mbps. • Added Figure 2, "Example Part Marking," on page 5. • Section 1.2, "Features": under, *Miscellaneous IPs and interfaces*: Changed *UARTs* bullet, from "up to 4.0 Mbps", to "up to 5.0 Mbps". • Table 8, "Operating Ranges," on page 29: — Changed *Run mode: VDD_ARM_IN* minimum value from 1.05 to 1.125V; for operation up to 396 MHz. and changed *LDO bypassed* maximum value from 1.225V to 1.21V; for *VDD_SOC_IN*. — Changed *PCIe supply voltages; PCIE_VP/PCIE_VPTX* maximum value from 1.225V to 1.21V • Table 10, "Maximum Supply Currents," on page 29; — Changed *VDD_ARM_IN* from single condition to include DualLite and Solo conditions with Maximum current values of 2200 and 1320 mA, respectively. — Added footnote for NVCC_LVDS2P5 supply. • Table 38, "Reset Timing Parameters": Removed footnote regarding SRC_POR_B rise and fall times. • Section 4.9.3, "External Interface Module (EIM)": Changed first paragraph to describe two systems clocks used with EIM: ACLK_EIM_SLOW_CLK_ROOT and ACLK_EXSC (for synchronous mode). • Table 31, "DDR I/O DDR3/DDR3L Mode AC Parameters"; Added footnote about extended range for Vix. • Table 48, "DDR3/DDR3L Timing Parameter Table," on page 76; Added DDR0, tCK(avg) and parameter values. Changed symbol names DDR1 through DDR7 to include avg or base; changed minimum parameter values for DDR4–DDR7. Added footnote about tIS and tIH base values. • Figure 25, "DDR3 Command and Address Timing Parameters," on page 76; Added DDR0. • Table 49, "DDR3/DDR3L Write Cycle," on page 77; Changed symbol names of DDR17 and DDR18 to include base(AC150/DC100); Changed Units from tCK to tCK(avg). • Table 46, "LPDDR2 Write Cycle," on page 64; Changed LP21 min/max parameter values from -0.25/+0.25 to 0.75/1.25. • Table 42, "EIM Bus Timing Parameters," on page 55: Changed footnotes regarding the system clocks used with EIM: from *axi_clk* to *ACLK_EXSC* or *ACLK_EIM_SLOW_CLK_ROOT.* • Table 49, "DDR3/DDR3L Write Cycle," on page 77: Changed *DDR17* minimum value from 420 ps to 125 ps and *DDR18* from 345 ps to 150 ps. • Table 49, "DDR3/DDR3L Write Cycle," on page 77: Added footnote 4. • Table 69, "LVDS Display Bridge (LDB) Electrical Specification," on page 105: Corrected Units for Output Voltage High and Output Voltage Low from mV to V. • Table 71, "Electrical and Timing Information," on page 108: Moved rows *tSETUP[RX]* and *tHOLD[RX]* to be directly under *HS Line Receiver AC Specifications* heading row. • Table 96, "21 x 21 mm Supplies Contact Assignments," on page 140: Removed A1 pin. • Table 97, "21 x 21 mm Functional Contact Assignments," on page 142: Moved rows *DRAM_4*, *DRAM_5,* and *DRAM_6* out of the i.MX 6DualLite section (shaded gray) to the i.MX 6Solo section above DRAM_7 and (unshaded). • Table 99, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo," on page 156: Removed "NC" from A1 pin location. • Table 100, "21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite," on page 159: Removed "NC" from A1 pin location. •