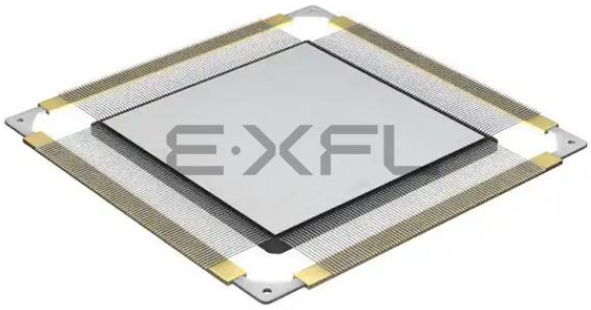

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	2MB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-40°C ~ 100°C (TC)
Mounting Type	Surface Mount
Package / Case	308-CBQFP
Supplier Device Package	308-CQFP (52x52)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad14060lbf-4

SPECIFICATIONS

Table 1. Recommended Operating Conditions

Parameter		B Grade Min	B Grade Max	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage (5 V)	4.75	5.25	4.75	5.25	V
	Supply Voltage (3.3 V)	3.15	3.6	3.15	3.6	V
T_{CASE}	Case Operating Temperature	−40	+100	0	+85	°C

ELECTRICAL CHARACTERISTICS (3.3 V, 5 V SUPPLY)

Table 2.

Parameter		Case Temp	Test Level	Test Condition	5 V Min	5 V Typ	5 V Max	3.3 V Min	3.3 V Typ	3.3 V Max	Unit
V_{IH1}	High Level Input Voltage[1]	Full	I	@ V_{DD} = max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	Full	I	@ V_{DD} = max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	Full	I	@ V_{DD} = min			0.8			0.8	V
V_{OH}	High Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OH} = −2.0 mA	4.1			2.4			V
V_{OL}	Low Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OL} = 4.0 mA			0.4			0.4	V
I_{IH}	High Level Input Current[5, 6, 7]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{IL}	Low Level Input Current[5]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{ILP}	Low Level Input Current[6]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{ILPX4}	Low Level Input Current[7]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{OZH}	Three-State Leakage Current[8, 9, 10, 11]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{OZL}	Three-State Leakage Current[8, 12]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{OZHP}	Three-State Leakage Current[12]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			350			350	µA
I_{OZLC}	Three-State Leakage Current[13]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			1.5			1.5	mA
I_{OZLA}	Three-State Leakage Current[14]	Full	I	@ V_{DD} = max, V_{IN} = 1.5 V (5 V), 2 V (3.3 V)			350			350	µA
I_{OZLAR}	Three-State Leakage Current[10]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			4.2			4.2	mA
I_{OZLS}	Three-State Leakage Current[9]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{OZLSX4}	Three-State Leakage Current[11]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{DDIN}	Supply Current (Internal)[15]	Full	IV	t_{CK} = 25 ns, V_{DD} = max		1.4	2.92		1.0	2.2	A
I_{DDIDLE}	Supply Current (Idle)[16]	Full	I	V_{DD} = max			800			760	mA
C_{IN}	Input Capacitance[17, 18]	25°C	V			15			15		pF

[1] Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{STBS}$, $\overline{IRQy_{2-0}}$, FLAGy0, FLAG1, FLAGy2, $\overline{HBG}$, CSy, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, RPBA, $\overline{CPAy}$, TFS0, TFSy1, RFS0, RFSy1, $LyxDAT_{3-0}$, LyxCLK, LyxACK, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, $\overline{BMSA}$, $\overline{BMSBCD}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DRy1, TCLK0, TCLKy1, RCLK0, RCLKy1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

[3] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, TIMEXPy, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPAy}$, DTO, DTy1, TCLK0, TCLKy1, RCLK0, RCLKy1, TFS0, TFSy1, RFS0, RFSy1, $LyxDAT_{3-0}$, LyxCLK, LyxACK, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$.

[4] See the Output Drive Currents section for typical drive current capabilities.

[5] Applies to input pins: $\overline{STBS}$, $\overline{IRQy_{2-0}}$, $\overline{HBR}$, $\overline{CSy}$, $\overline{DMAR1}$, $\overline{DMAR2}$, RPBA, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, CLKIN, $\overline{RESET}$, TCK.

[6] Applies to input pins with internal pull-ups: DR0, $\overline{DRy1}$, TDI.

[7] Applies to bused input pins with internal pull-ups: $\overline{TRST}$, TMS.

[8] Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership. $\overline{HBG}$ and $\overline{EMU}$ are not tested for leakage current.)

[9] Applies to three-statable pins with internal pull-ups: DTy1, TCLKy1, RCLKy1.

[10] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership.)

[11] Applies to bused three-statable pins with internal pull-ups: DT0, TCLK0, RCLK0.

[12] Applies to three-statable pins with internal pull-downs: $LyxDAT_{3-0}$, LyxCLK, LyxACK.

[13] Applies to $\overline{CPAy}$ pin.

[14] Applies to ACK pin, when the keeper latch is enabled.

[15] Applies to V_{DD} pins. Conditions of operation: each processor is executing radix-2 FFT butterfly with instruction in cache, one data operand is fetched from each internal memory block, and one DMA transfer is occurring from/to internal memory at t_{CK} = 25 ns.

[16] Applies to V_{DD} pins. Idle denotes AD14060/AD14060L state during execution of IDLE instruction.

[17] Applies to all signal pins.

[18] Guaranteed, but not tested.

Table 4. Reset

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Reset						
Timing Requirements:						
t_{WRST}	$\overline{RESET}$ Pulse Width Low[1]	4 t_{CK}		4 t_{CK}		ns
t_{SRST}	$\overline{RESET}$ Setup before CLKIN High[2]	14 + DT/2	t_{CK}	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while $\overline{RESET}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of the external clock oscillator).
[2] Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (that is, for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

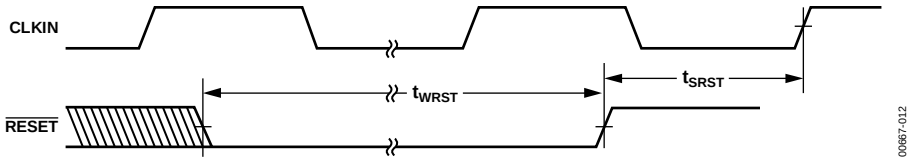


Figure 3. Reset

Table 5. Interrupts

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Interrupts						
Timing Requirements:						
t_{SIR}	$\overline{IRQ}$2-0 Setup before CLKIN High[1]	18 + 3 DT/4		18 + 3 DT/4		ns
t_{HIR}	$\overline{IRQ}$2-0 Hold before CLKIN High[1]		11.5 + 3 DT/4		11.5 + 3 DT/4	ns
t_{IPW}	$\overline{IRQ}$2-0 Pulse Width[2]	2 + t_{CK}		2 + t_{CK}		ns

[1] Only required for $\overline{IRQ}$x recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

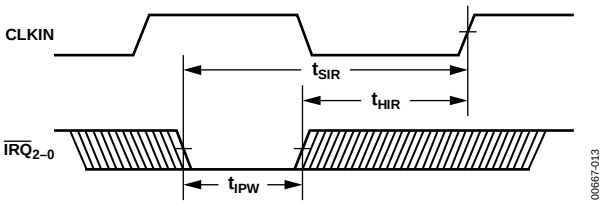


Figure 4. Interrupts

MEMORY READ—BUS MASTER

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the AD14060/AD14060L is the bus master accessing external memory space.

These switching characteristics also apply for bus master synchronous read/write timing (see the Synchronous Read/Write—Bus Master section). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Table 8. Specifications

Parameter		5 V		3.3 V		Unit
		Min	Max	Min	Max	
Timing Requirements:						
t_{DAD}	Address, Delay to Data Valid[1, 2]		17.5 + DT + W		17.5 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		11.5 + 5 DT/8 + W		11.5 + 5 DT/8 + W	ns
t_{HDA}	Data Hold from Address[3]	1		1		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.5		2.5		ns
t_{DAAK}	ACK Delay from Address[2, 4]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		7.5 + DT/2 + W		7.5 + DT/2 + W	ns
Switching Characteristics:						
t_{DRHA}	Address Hold after $\overline{RD}$ High	−0.5 + H		−0.5 + H		ns
t_{DARL}	Address to $\overline{RD}$ Low[2]	1.5 + 3 DT/8		1.5 + 3 DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5 DT/8 + W		12.5 + 5 DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 3 DT/8 + HI		8 + 3 DT/8 + HI		ns
t_{SADADC}	Address Setup before ADRCLK High[2]	−0.5 + DT/4		−0.5 + DT/4		ns

W = number of wait states specified in WAIT register × t_{CK}.
HI = t_{CK}, if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise, HI = 0.
H = t_{CK}, if an address hold cycle occurs as specified in WAIT register; otherwise, H = 0.

[1] Data delay/setup: User must meet t_{DAD}, t_{DRLD}, or synchronous specification, t_{SSDATI}.
[2] For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.
[3] Data hold: User must meet t_{HDA}, t_{HDRH}, or synchronous specification, t_{HDATI}. See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: User must meet t_{DSAK}, t_{DAAK}, or synchronous specification, t_{SACKC}.

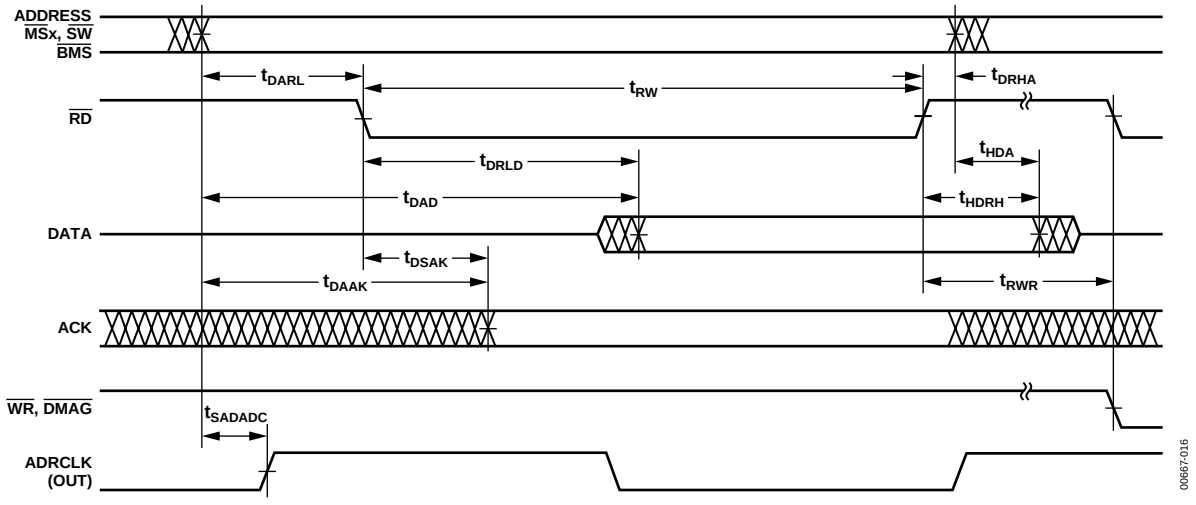


Figure 7. Memory Read—Bus Master

SYNCHRONOUS READ/WRITE—BUS MASTER

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP 2106x in multiprocessor memory space. These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see the Memory Read—Bus Master and Memory Write—Bus Master sections).

When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see the Synchronous Read/Write—Bus Slave section). The slave ADSP-2106x must also meet these bus master timing requirements for data and acknowledge setup and hold times.

Table 10. Specifications

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{SSDATI}	Data Setup before CLKIN	3 + DT/8		3 + DT/8		ns
t_{HSDATI}	Data Hold after CLKIN	4 – DT/8		4 – DT/8		ns
t_{DAAK}	ACK Delay after Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{SACKC}	ACK Setup before CLKIN[2]	6.5 + DT/4		6.5 + DT/4		ns
t_{HACKC}	ACK Hold after CLKIN	–0.5 – DT/4		–0.5 – DT/4		ns
Switching Characteristics:						
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$, Delay after CLKIN[1]		8 – DT/8		8 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$, Hold after CLKIN	–1 – DT/8		–1 – DT/8		ns
t_{DPGC}	PAGE Delay after CLKIN	9 + DT/8	17 + DT/8	9 + DT/8	17 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay after CLKIN	–2 – DT/8	+5 – DT/8	–2 – DT/8	+5 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay after CLKIN	–3 – 3 DT/16	+5 – 3 DT/16	–3 – 3 DT/16	+5 – 3 DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay after CLKIN	8 + DT/4	13.5 + DT/4	8 + DT/4	13.5 + DT/4	ns
t_{SDDATO}	Data Delay after CLKIN		20 + 5 DT/16		20.25 + 5 DT/16	ns
t_{DATTR}	Data Disable after CLKIN[3]	0 – DT/8	8 – DT/8	0 – DT/8	8 – DT/8	ns
t_{DADCCK}	ADRCLK Delay after CLKIN	4 + DT/8	11 + DT/8	4 + DT/8	11 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns

W = number of wait states specified in WAIT register × t_{CK}.

[1] For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.
[2] ACK delay/setup: User must meet t_{DAAK}, t_{DSAK}, or synchronous specification, t_{SACKC}.
[3] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

SYNCHRONOUS READ/WRITE—BUS SLAVE

Use these specifications for bus master access to a slave's IOP registers or internal memory in multiprocessor memory space. The bus master must meet these bus slave timing requirements.

Table 11. Specifications

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{SADRI}	Address, $\overline{SW}$ Setup before CLKIN	15.5 + DT/2		15.5 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold before CLKIN		4.5 + DT/2		4.5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup before CLKIN[1]	9.5 + 5 DT/16		9.5 + 5 DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold after CLKIN	−3.5 − 5 DT/16	+8 + 7 DT/16	−3.25 − 5 DT/16	+8 + 7 DT/16	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		3		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	5.5		5.5		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	1.5		1.5		ns
Switching Characteristics:						
t_{SDDATO}	Data Delay after CLKIN		20 + 5 DT/16		20.25 + 5 DT/16	ns
t_{DATTR}	Data Disable after CLKIN[2]	0 − DT/8	8 − DT/8	0 − DT/8	8 − DT/8	ns
t_{DACKAD}	ACK Delay after Address, $\overline{SW}$[3]		10		10	ns
t_{ACKTR}	ACK Disable after CLKIN[3]	−1 − DT/8	+7 − DT/8	−1 − DT/8	+7 − DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5 DT/16 when the multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.

[2] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

[3] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10.5 + DT/8 and less than 18.5 + 3 DT/4. If the address and $\overline{SW}$ inputs have setup times greater than 19 + 3 DT/4, then ACK is valid 15 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match responds with ACK regardless of the state of MMSWS or strobes. A slave three-states ACK every cycle with t_{ACKTR}.

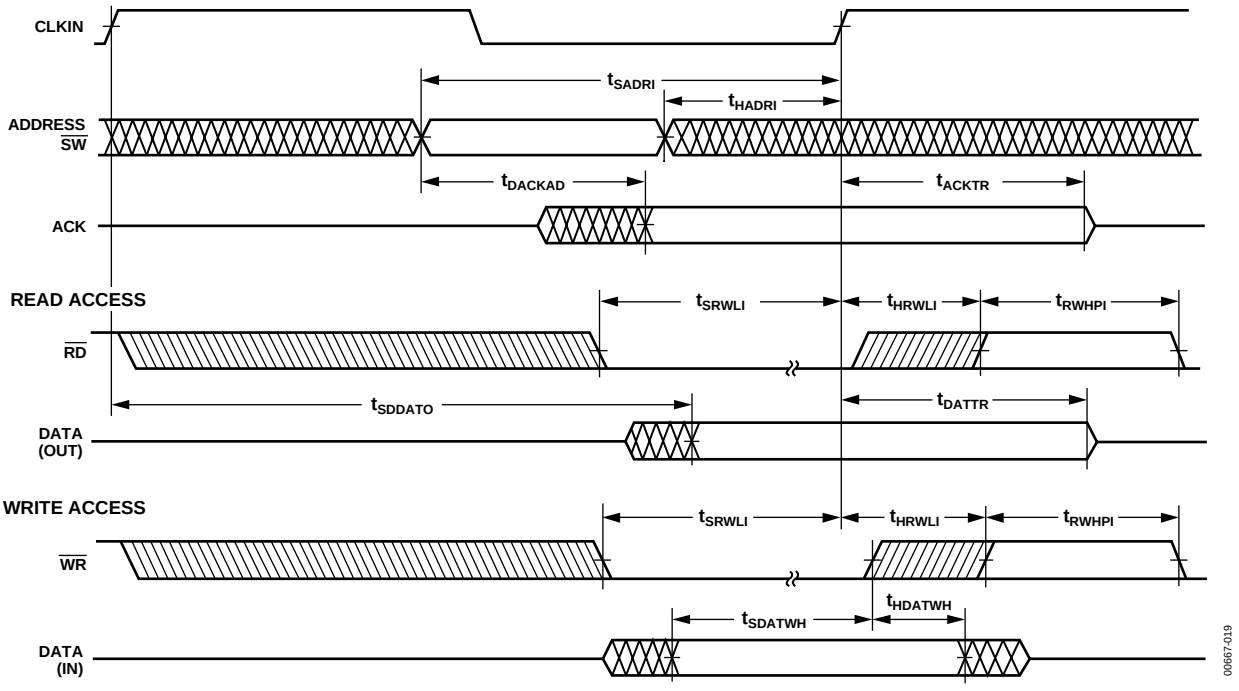


Figure 10. Synchronous Read/Write—Bus Slave

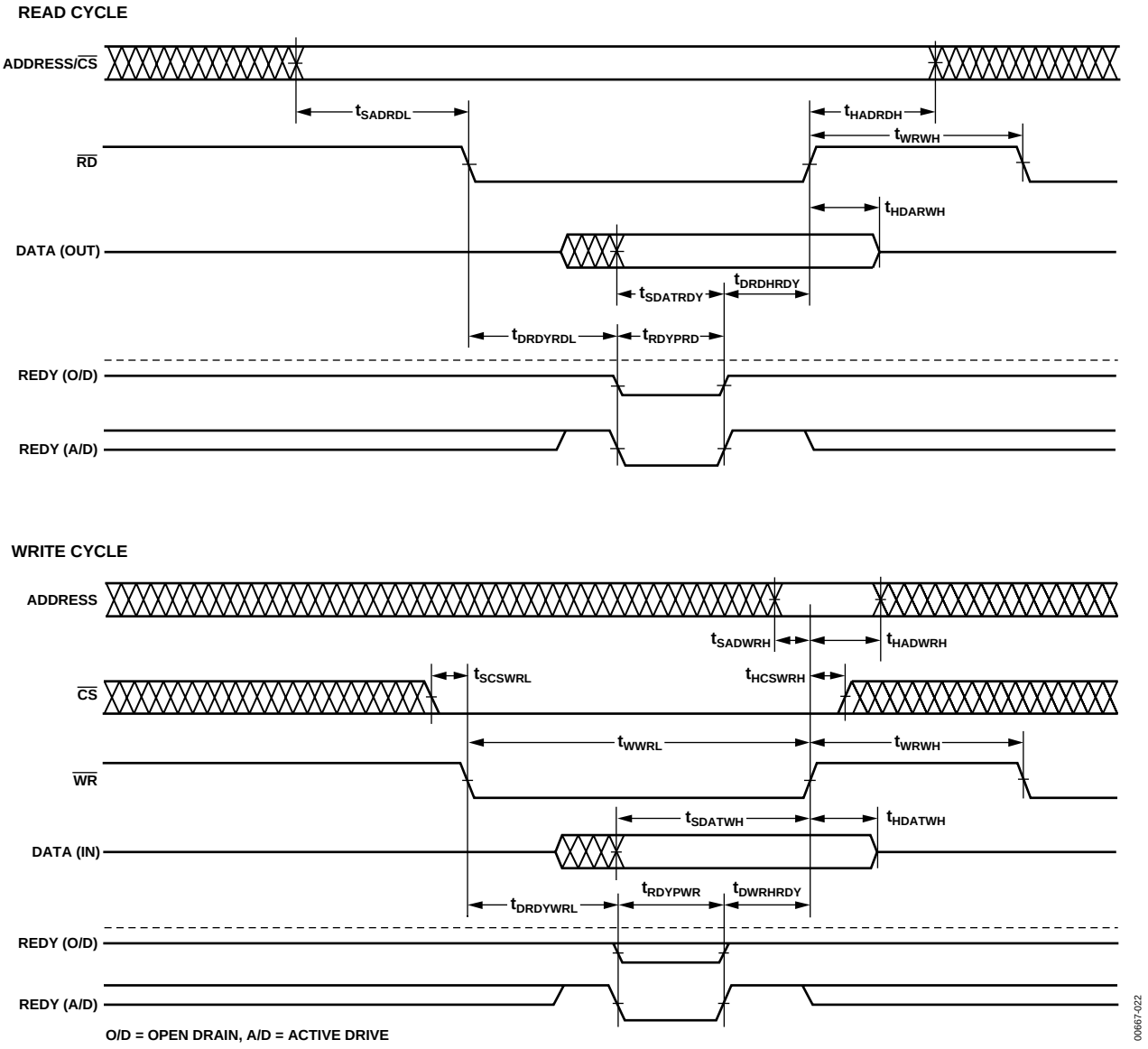


Figure 13. Asynchronous Read/Write—Host to ADSP-2106x

DMA HANDSHAKE

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMAR}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS}}_{3\text{-}0}$, ACK, and $\overline{\text{DMAG}}$ signals. For paced master mode, the data transfer is controlled by $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, and ACK (not $\overline{\text{DMAG}}$). For paced master mode, the memory read—bus master, memory write—bus master, and synchronous read/write—bus master timing specifications for $\text{ADDR}_{31\text{-}0}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}_{3\text{-}0}$, $\overline{\text{SW}}$, PAGE, $\text{DATA}_{47\text{-}0}$, and ACK also apply.

Table 15. Specifications

		5 V		3.3 V		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements:						
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup before CLKIN[1]	5		5		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup before CLKIN[1]	5		5		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6		6		ns
$t_{SDATDGL}$	Data Setup after $\overline{\text{DMAG}}$x Low[2]		9 + 5 DT/8		9 + 5 DT/8	ns
$t_{HDATIDG}$	Data Hold after $\overline{\text{DMAG}}$x High	2		2		ns
t_{DATDRH}	Data Valid after $\overline{\text{DMAG}}$x High[2]		15.5 + 7 DT/8		15.5 + 7 DT/8	ns
t_{DMARLL}	$\overline{\text{DMAG}}$x Low Edge to Low Edge	23 + 7 DT/8		23 + 7 DT/8		ns
t_{DMARH}	$\overline{\text{DMAG}}$x Width High	6		6		ns
Switching Characteristics:						
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay after CLKIN	9 + DT/4	16 + DT/4	9 + DT/4	16 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	6 + 3 DT/8		6 + 3 DT/8		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	12 + 5 DT/8		12 + 5 DT/8		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay after CLKIN	−2 − DT/8	+7 − DT/8	−2 − DT/8	+7 − DT/8	ns
$t_{VDATDGH}$	Data Valid before $\overline{\text{DMAG}}$x High[3]	7.5 + 9 DT/16		7.5 + 9 DT/16		ns
$t_{DATRDGH}$	Data Disable after $\overline{\text{DMAG}}$x High[4]	−1	+7.5	−1	+7.5	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low before $\overline{\text{DMAG}}$x Low	−0.5	+2.5	−0.75	+2.5	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low before $\overline{\text{WR}}$ High	9.5 + 5 DT/8 + W		9.5 + 5 DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High before $\overline{\text{DMAG}}$x High	0.5 + DT/16	3.5 + DT/16	0.5 + DT/16	3.5 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x Low	−0.25	+2.5	0	2.5	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x High	11 + 9 DT/16 + W		11 + 9 DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High before $\overline{\text{DMAG}}$x High	0	3.5	0	3.5	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAG}}$x Low	4.5 + 3 DT/8 + HI		4.5 + 3 DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAG}}$x High	16 + DT		16 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAG}}$x High	−1.5		−1.5		ns

W = number of wait states specified in WAIT register × t_{CK}.
HI = t_{CK}, if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise, HI = 0.

[1] Required only for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement, if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.
[3] $t_{VDATDGH}$ is valid, if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 7.5 + 9 DT/16 + ($n \times t_{CK}$), where n equals the number of extra cycles that the access is prolonged.
[4] See the System Hold Time Calculation Example section for the calculation of hold times given capacitive and dc loads.

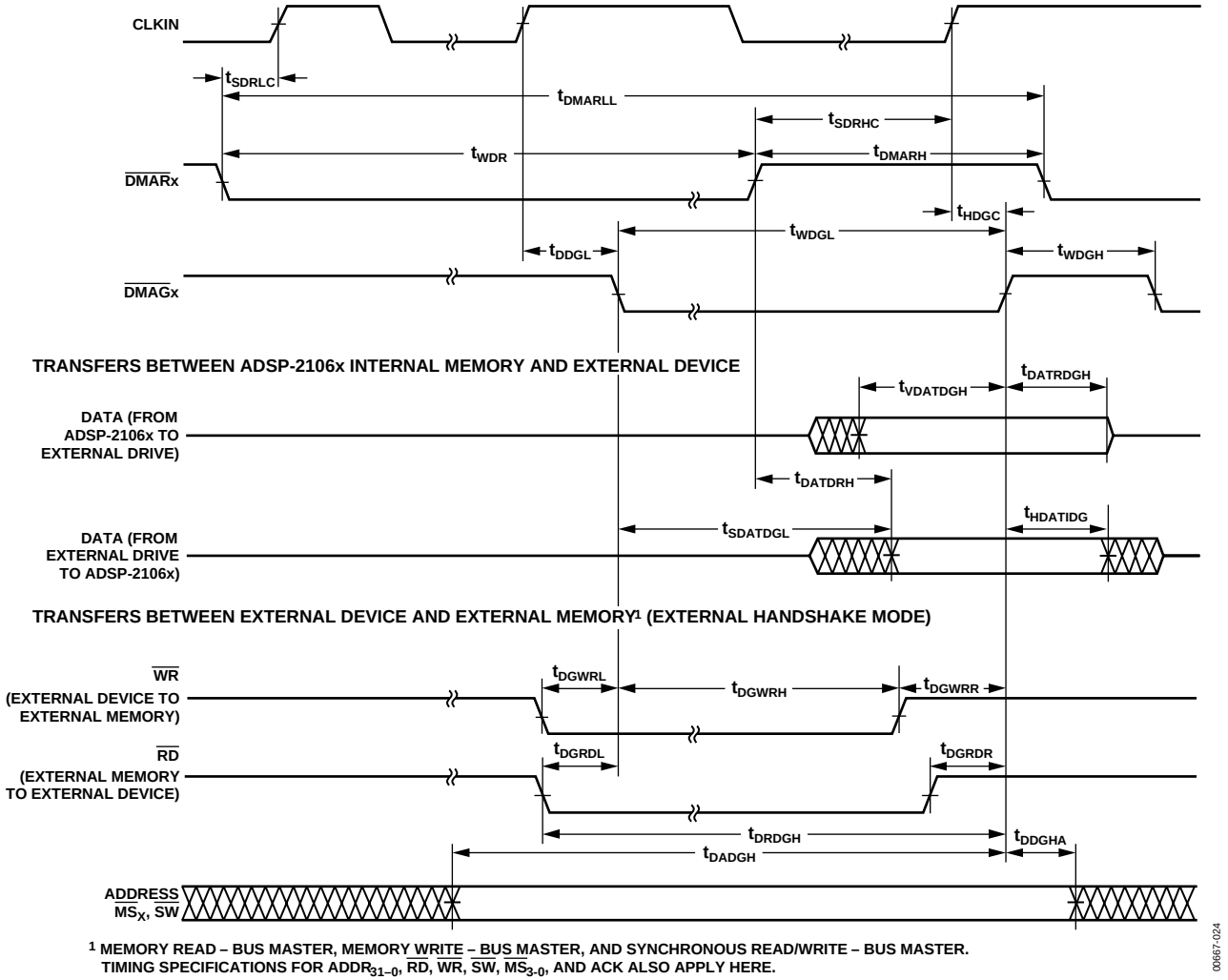


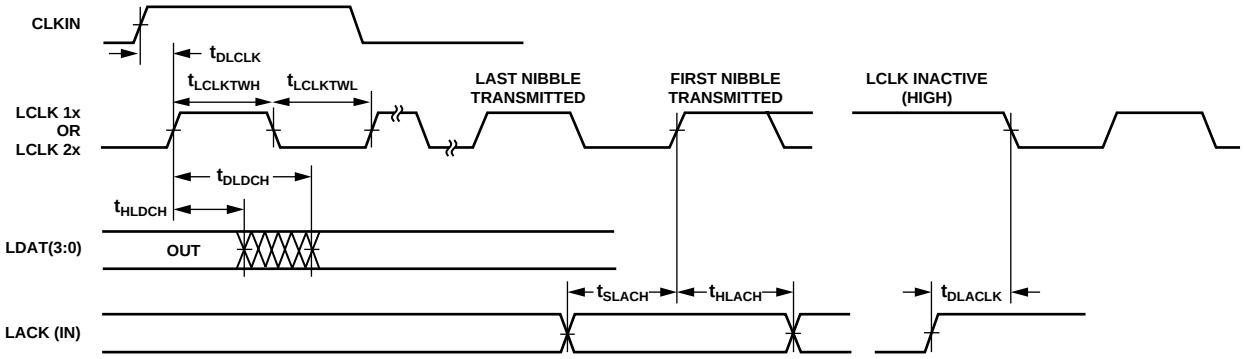
Figure 15. DMA Handshake Timing

Table 17. 2× CLK Speed Operation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup before LCLK Low	2.75		2.25		ns
t_{HLDCL}	Data Hold after LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2× Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low	4.6		5.25		ns
$t_{LCLKRWH}$	LCLK Width High	4.25		4.5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay after CLKIN High	18 + DT/2	31.5 + DT/2	18 + DT/2	30.5 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High[1]	6	17.8	6	19	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup before LCLK High	20.25		19		ns
t_{HLACH}	LACK Hold after LCLK High	−6.5		−6.5		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay after CLKIN		9		9	ns
t_{DLDCH}	Data Delay after LCLK High		3.25		2.75	ns
t_{HLDCH}	Data Hold after LCLK High	−2		−2		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/4) - 1$	$(t_{CK}/4) + 1.5$	$(t_{CK}/4) - 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	$(t_{CK}/4) - 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{CK}/4) + 9$	$(3 \times t_{CL}/4) + 17$	$(t_{CK}/4) + 9$	$(3 \times t_{CL}/4) + 17$	ns

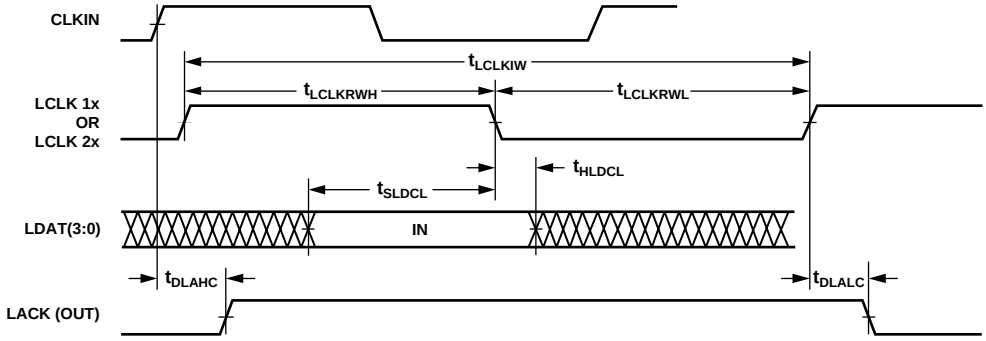
[1] LACK goes low with t_{DLALC} relative to the rising edge of LCLK after the first nibble is received. LACK does not go low, if the receiver's link buffer is not about to fill.

TRANSMIT



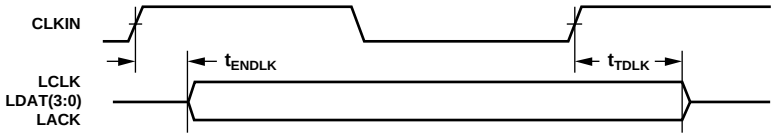
THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



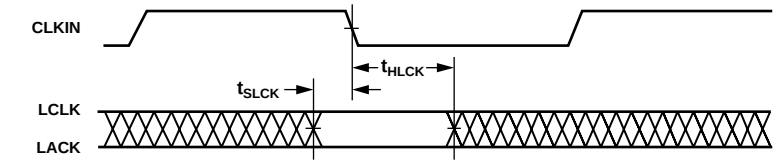
LACK GOES LOW ONLY AFTER THE SECOND NIBBLE IS RECEIVED.

LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME



00667-025

Figure 16. Link Ports

Table 19. JTAG Test Access Port and Emulation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Unit
Timing Requirements:						
t_{TCK}	TCK Period	t_{CK}		t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5				ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		6		ns
t_{SSYS}	System Inputs Setup before TCK Low[1]	7		8		ns
t_{HSYS}	System Inputs Hold after TCK Low[1]	18.5		19		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	4 t_{CK}		4 t_{CK}		ns
Switching Characteristics:						
t_{DTDO}	TDO Delay from TCK Low		13.5		13.5	ns
t_{DSYS}	System Outputs Delay after TCK Low[2]		20		20	ns

[1] System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, RPBA, $\overline{IRQ_{2-0}}$, FLAG2-0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPA}$, $FLAG_{2-0}$, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

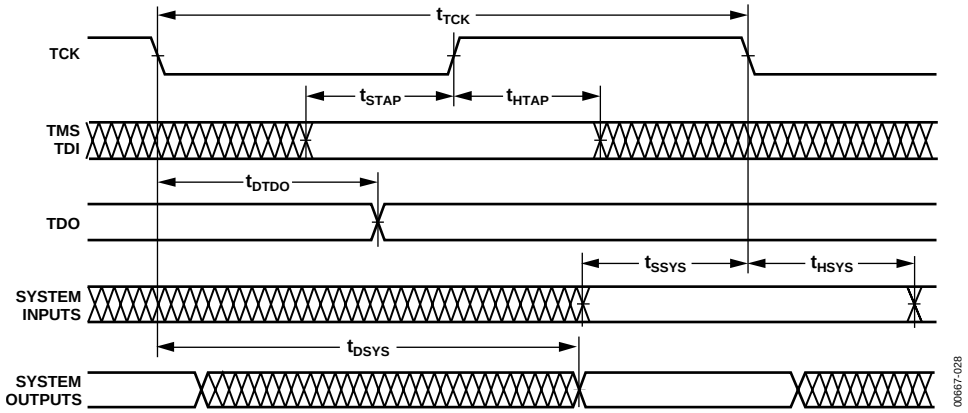


Figure 19. IEEE 11499.1 JTAG Test Access Port

ABSOLUTE MAXIMUM RATINGS

Table 20.

Parameters	Ratings
Supply Voltage (5 V)	−0.3 V to +7 V
Supply Voltage (3.3 V)	−0.3 V to +4.6 V
Input Voltage	−0.5 V to V_{DD} + 0.5 V
Output Voltage Swing	−0.5 V to V_{DD} + 0.5 V
Load Capacitance	200 pF
Junction Temperature under Bias	130°C
Storage Temperature Range	−65°C to +150°C
Lead	280°C

Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

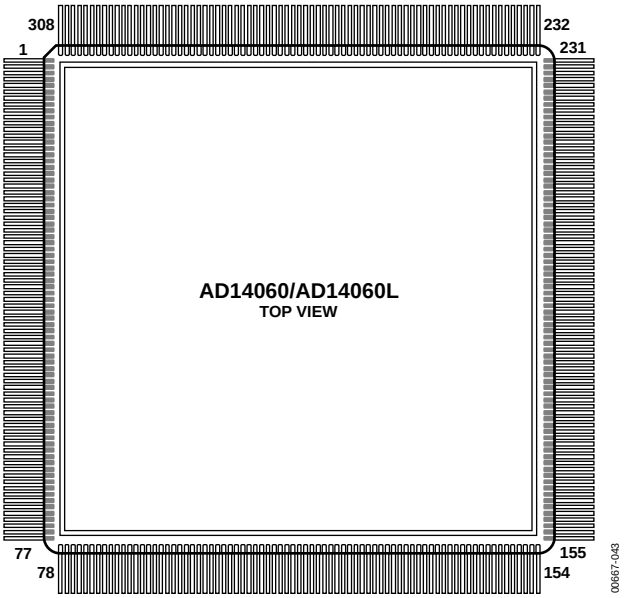


Figure 20. 308-Lead CQFP Pin Configuration

Pin	Type[1]	Function
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic chain starting at SHARC_A. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan chain path, from SHARC_D.
$\overline{\text{TRST}}$	I/A	Test Reset (JTAG) (common to all SHARCs). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the AD14060/AD14060L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	Emulation Status (common to all SHARCs). Must be connected to the ADSP-2106x EZ-ICE target board connector only.
V_{DD}	P	Power Supply. Nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices (26 pins).
GND	G	Power Supply Return (28 pins).

FLAG3 is connected internally, common to SHARC_A, B, C, and D.
ID pins are hardwired internally as shown in Figure 1.

[1] I = input; P = power supply; (A/D) = active drive; O = output; S = synchronous; (O/D) = open drain; G = ground; A = asynchronous; T = three-state, when $\overline{\text{SBTS}}$ is asserted, or when the AD14060/AD14060L is a bus slave.
[2] Link Ports 0, 2, and 5 are connected internally, as described in the Link Port I/O section.
[3] Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

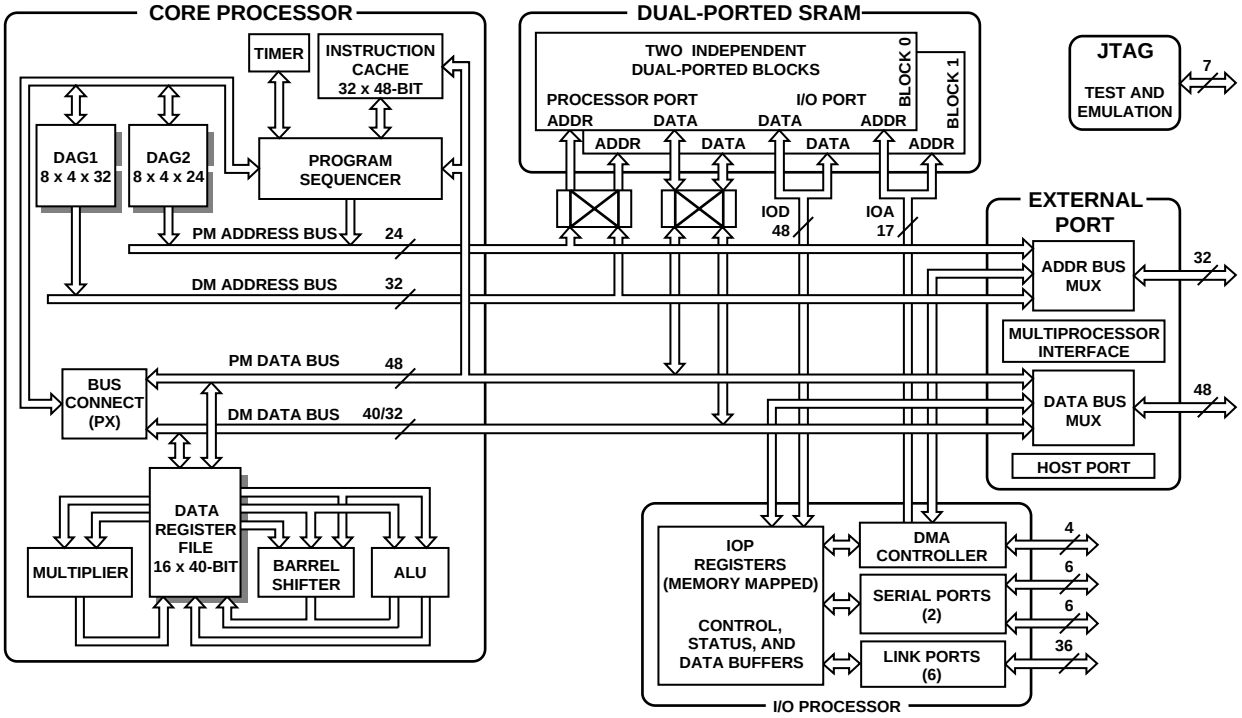


Figure 21. ADSP-21060 Processor Block Diagram (Core of AD10460)

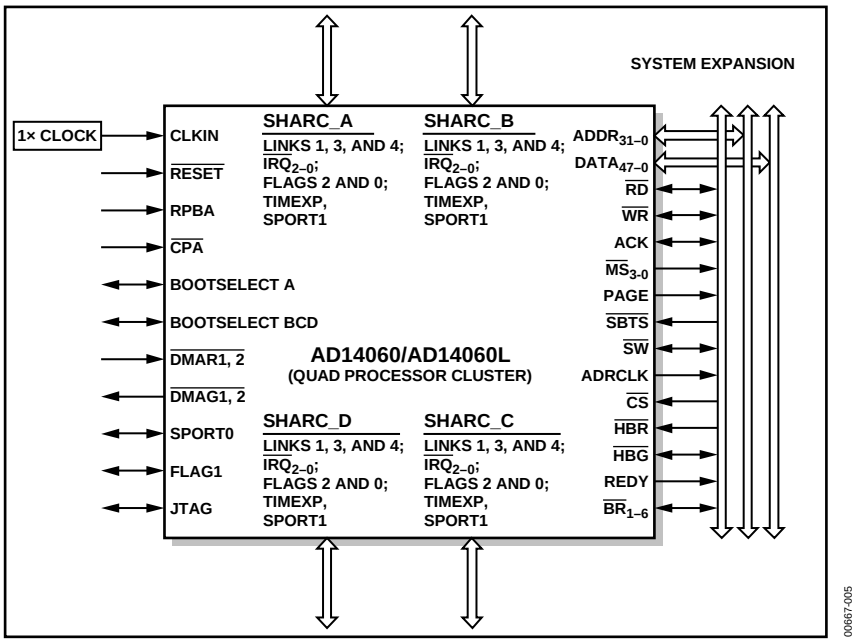


Figure 22. Complete Shared Memory Multiprocessing System

Multiprocessor EPROM Booting

The following methods boot the multiprocessor system from an EPROM:

- **SHARC_A is booted, which then boots the others.**

  The EBOOT pin on the SHARC_A must be set high for EPROM booting. All other ADSP-21060s should be configured for host booting (EBOOT = 0, LBOOT = 0, and $\overline{\text{BMS}}$ = 1), which leaves them in the idle state at startup and allows SHARC_A to become bus master and boot itself. Only the $\overline{\text{BMS}}$ pin of SHARC_A is connected to the chip select of the EPROM. When SHARC_A has finished booting, it can boot the remaining ADSP-21060s by writing to their external port DMA Buffer 0 (EPB0) via multiprocessor memory space.

- **All ADSP-21060s boot in turn from a single EPROM.**

  The $\overline{\text{BMS}}$ signals from each ADSP-21060 can be wire-OR'ed together to drive the chip select pin of the EPROM. Each ADSP-21060 can boot in turn, according to its priority. When the last one has finished booting, it must inform the others (which can be in the idle state) that program execution can begin.

Multiprocessor Link-Port Booting

Booting can also be accomplished from a single source through the link ports. Link Buffer 4 must always be used for booting. To simultaneously boot all the ADSP-21060s, a parallel common connection is available through Link Port 4 on each of the processors. Or, using the daisy-chain connection that exists between the processors' link ports, each ADSP-21060 can boot the next one in turn. In this case, the link assignment register (LAR) must be programmed to configure the internal link ports with Link Buffer 4.

Multiprocessor Booting from External Memory

If external memory contains a program after reset, then SHARC_A should be set up for no-boot mode. It begins executing from Address 0x0040 0004 in external memory. When booting has completed, the other ADSP-21060s can be booted by SHARC_A, if they are set up for host booting; or they can begin executing out of external memory, if they are set up for no-boot mode. Multiprocessor bus arbitration allows this booting to occur in an orderly manner.

HOST PROCESSOR INTERFACE

The AD14060/AD14060L's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds of up to the full clock rate of the module are supported. The host interface is accessed through the AD14060/AD14060L external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the AD14060/AD14060L's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the SHARCs, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DIRECT MEMORY ACCESS (DMA) CONTROLLER

The SHARCs' on-chip DMA control logic allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to each SHARC's processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between SHARC internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the SHARC's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32- or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the SHARCs: two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other SHARCs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the SHARCs using DMA transfers. Asynchronous off-module peripherals can control two DMA channels using DMA request/grant lines ($\overline{\text{DMAR}}$1-2, $\overline{\text{DMAG}}$1-2). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

APPLICATIONS

DEVELOPMENT TOOLS

The AD14060/AD14060L is supported with a complete set of software and hardware development tools, including an in-circuit emulator and development software.

Analog Devices, Inc. (ADI) uses VisualDSP++®, which is an easy-to-use integrated software development and debugging environment (IDDE) that efficiently manages projects from start to finish from within a single interface.

The ADSP-21262 EZ-KIT LITE™ provides developers with a cost-effective method for initial evaluation of the ADSP-2106x SHARC processor architecture for applications via a USB-based PC-hosted tool set. With this EZ-KIT LITE, users can learn about ADI's ADSP-2106x hardware and software development and can quickly prototype applications.

The EZ-KIT LITE includes an ADSP-2106x processor desktop evaluation board, along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. VisualDSP++ development and debugging software, along with the USB-based debugger interface, enables users to perform standard debugging functions (such as read and write memory, read and write registers, load and execute executables, set and clear breakpoints, and single-step assembly, C, and C++ source code).

The ADI cost-effective universal serial bus (USB)-based emulator and high performance (HP) universal serial bus (USB)-based emulator each provide an easy, portable, non-intrusive, target-based debugging solution for ADI JTAG processors and DSPs. These powerful USB-based emulators perform a wide range of emulation functions, including single-step and full speed execution with predefined breakpoints, and viewing and altering of register and memory contents. With the ability to automatically detect and support multiple I/O voltages, the USB and HP USB emulators enable users to communicate with all the ADI JTAG processors and DSPs using either a full speed USB 1.1 or high speed USB 2.0 port on the host PC. Applications and data can be easily and rapidly tested and transferred between the emulators and the separately available VisualDSP++ development and debugging environment (sold separately).

The plug-and-play architecture of the USB allows the host operating system to automatically detect and configure the emulators. The USB can be connected to and disconnected from the host without opening the PC or turning off the power to the PC. A 3-meter cable is included to connect the emulators to the host PC, providing abundant accessibility to hard-to-reach targets.

The HP USB-based emulator supports the background telemetry channel (BTC), a nonintrusive method for exchanging data between the host and target application without affecting the target system's real-time characteristics. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface. The emulator does not affect target system loading or timing.

Further details and ordering information are available on the analog.com Web site.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards, multiprocessor SHARC VME boards, and daughter card modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC module specification. Third-party software tools include an Ada compiler, DSP libraries, operating systems, and block diagram design tools.

QUAD-SHARC DEVELOPMENT BOARD

The BlackTip-MCM, AD14060 development board with software is available from Bittware Research Systems, Inc. This board has one AD14060 BITSI interface, and PROM and SRAM expansion options on an ISA card. It is supported by Bittware's SHARC software development package. To contact Bittware, call 1-800-848-0436.

OTHER PACKAGE DETAILS

The AD14060/AD14060L contains 16 on-module 0.018 µF bypass capacitors. It is recommended that, in the target system, at least four additional capacitors of 0.018 µF value be placed around the module, one near each of the four corners.

The top surface (lid) of the AD14060/AD14060L is electrically connected to GND on the industrial and military grade parts.

TARGET BOARD CONNECTOR FOR EMULATOR PROBE

The ADSP-2106x emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The emulator probe requires that the AD14060/AD14060L's CLKIN (optional), TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$, and GND signals be made accessible on the target system via a 14-pin connector (pin strip header) similar to Figure 26. The emulator probe plugs directly into this connector for chip-on-board emulation. You must add this connector to your target board design, if you intend to use the ADSP-2106x emulator. The length of the traces between the connector and the AD14060/AD14060L's JTAG pins should be as short as possible.

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2\ t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2\ t_{CK})$, but selects can switch on each cycle.

Example

Estimate P_{EXT} with the following assumptions: a system with one bank of external data memory RAM (32-bit); four 128k × 8 RAM chips are used, each with a load of 10 pF; external data memory writes occur every other cycle; a rate of $1/(4\ t_{CK})$ with 50% of the pins switching; and an instruction cycle rate is 40 MHz (t_{CK} = 25 ns) and V_{DD} = 5.0 V.

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 25.A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all 1s to all 0s. It is uncommon for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L\ \Delta V}{I_L}$$

The output disable time, t_{DIS}, is the difference between $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 30. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time, t_{ENA}, is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the output enable/disable diagram (Figure 30). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

System Hold Time Calculation Example

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the previous equation. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV is 0.4 V. C_L is the total bus capacitance per data line, and I_L is the total leakage or three-state current per data line. The hold time is t_{DECAY} plus the minimum disable time (t_{HDWD} for the write cycle).

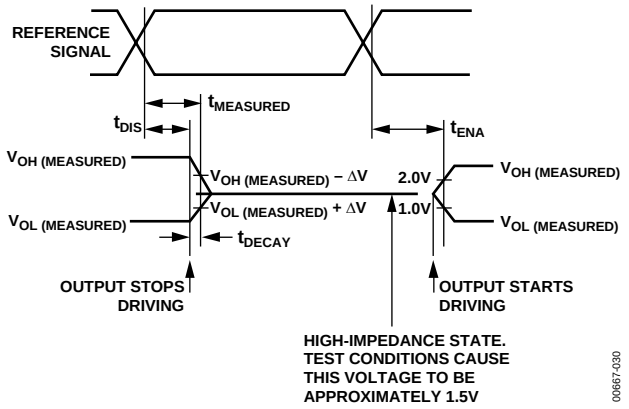


Figure 30. Output Enable/Disable

Table 25. P_{EXT} Calculations

Pin Type	Number of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 55 pF	× 20 MHz	× 25 V	= 0.206 W
$\overline{MSO}$	1	0	× 55 pF	× 20 MHz	× 25 V	= 0.00 W
$\overline{WR}$	1	–	× 55 pF	× 40 MHz	× 25 V	= 0.055 W
Data	32	50	× 25 pF	× 20 MHz	× 25 V	= 0.200 W
ADRCLK	1	–	× 15 pF	× 40 MHz	× 25 V	= 0.015 W

P_{EXT} (5 V) = 0.476 W.
P_{EXT} (3.3 V) = 0.207 W.

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 31). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 33 and Figure 34 show how output rise time varies with capacitance. Figure 35 graphically shows how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the Output Disable Time section.) The graphs in Figure 33, Figure 34, and Figure 35 might not be linear outside the ranges shown.

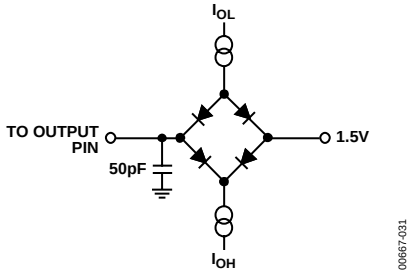


Figure 31. Equivalent Device Loading for AC Measurement (Includes All Fixtures)

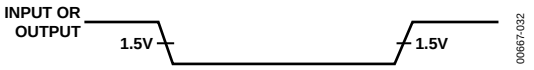


Figure 32. Voltage Reference Levels for AC Measurements (except Output Enable/Disable)

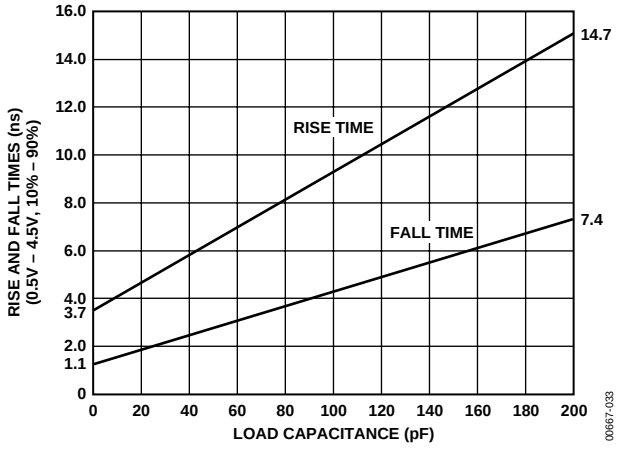


Figure 33. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

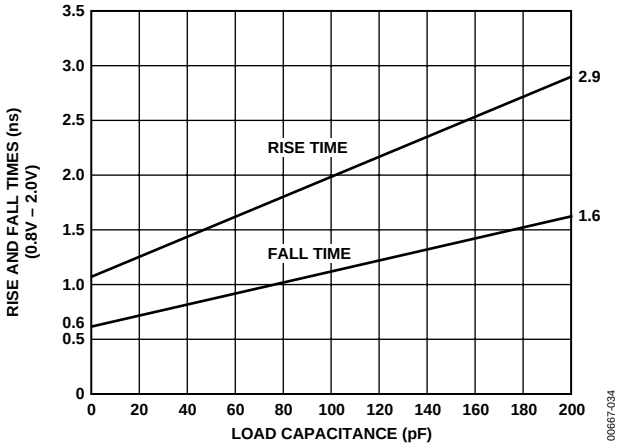


Figure 34. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

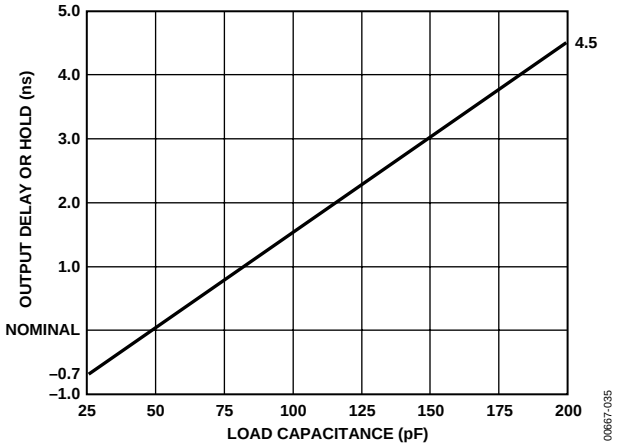


Figure 35. Typical Output Delay or Hold vs. Load Capacitance at Maximum Case Temperature (V_{DD} = 5 V)

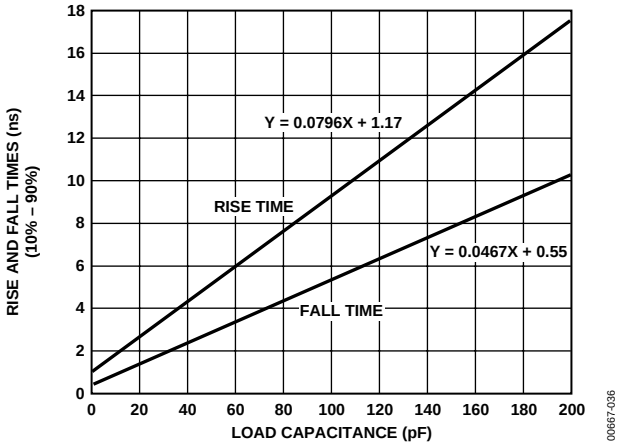


Figure 36. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

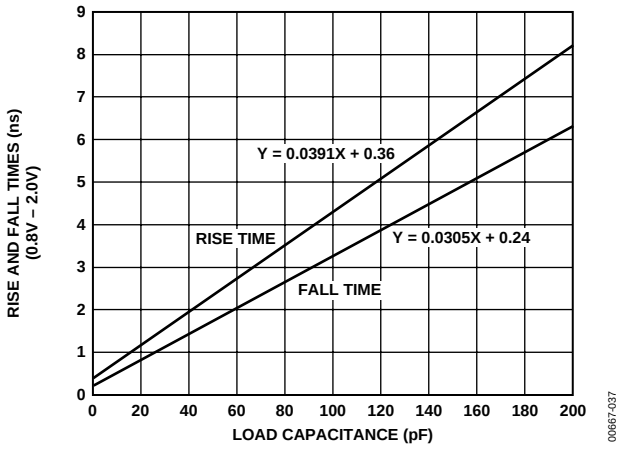


Figure 37. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

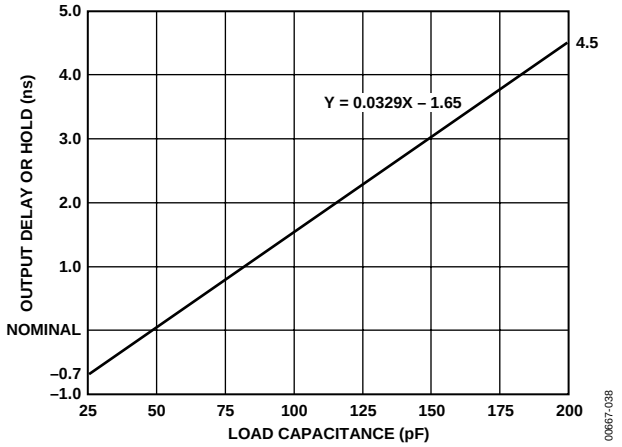


Figure 38. Typical Output Delay or Hold vs. Load Capacitance at Maximum Case Temperature (V_{DD} = 3.3 V)

ASSEMBLY RECOMMENDATIONS

Socket Information

Standard sockets and carriers are available for the AD14060/AD14060L, if needed. Socket part number IC53-3084-262 and carrier part number ICC-308-1 are available from Yamaichi Electronics.

Trim and Form

The AD14060/AD14060L is shipped as shown in Figure 43 with untrimmed and unformed leads and with the nonconductive tie bar in place. This avoids disturbance of lead spacing and coplanarity prior to assembly. Optimally, the leads should be trimmed, formed, and solder-dipped just prior to placement on the board.

Trim/form can be accomplished with a universal trim/form, a customer-designed trim/form, or with the Analog Devices developed tooling described as follows.

A trim/form tool specific to the AD14060/AD14060L has been developed and is available for use by all parties at

Tintronics Industries
2122-A Metro Circle
Huntsville, AL 35801
256-650-0220
Contact Person: Tom Rice

The package outline and dimensions resulting from this tool are shown in Figure 39. (Alternatively, the package can be trimmed/formed for cavity-down placement.)

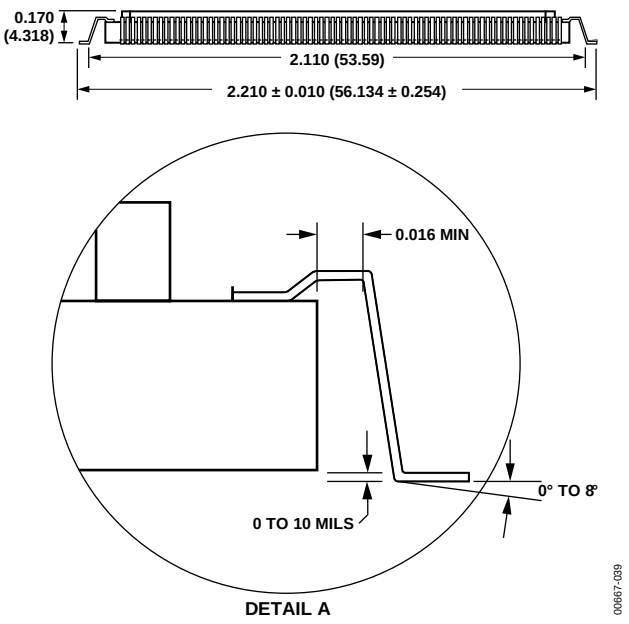


Figure 39. Package and Lead Profile Dimensions shown in inches and (millimeters)