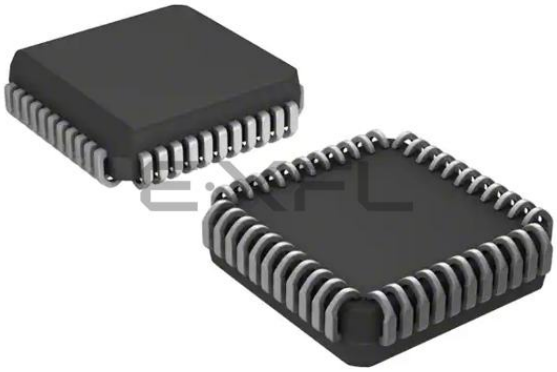

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51mb2ba-02-529

- Low EMI (inhibit ALE)
- Watchdog timer with programmable prescaler for different time ranges (compatible with 8xC66x with added prescaler)

3. Differences between P87C51MX2/02 part and previous revisions of P87C51MX2

The P87C51MX2/02 offers several advantages over the previous generation of P87C51MX2 parts. Right now, SPI module is available, two more general purpose digital pins on P4 are present and additional power control features are implemented (advanced peripheral clock control). New memory interface mode and code size optimization options are available with the use of MXCON register.

No changes are necessary when porting and loading code written for existing P87C51MX2 to the new P87C51MX2/02.

4. Ordering information

Table 1: Ordering information

Type number	Memory		Temp Range (°C)	V_{DD} voltage range	Frequency		Package		
	OTP	RAM			V_{DD} = 2.7 to 5.5 V	V_{DD} = 4.5 to 5.5 V	Name	Description	Version
P87C51MB2BA/02	64 kB	2048 B	0 to +70	2.7 to 5.5 V	0 to 12 MHz	0 to 24 MHz	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P87C51MC2BA/02	96 kB	3072 B	0 to +70	2.7 to 5.5 V	0 to 12 MHz	0 to 24 MHz	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

7.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	43 - 36	I/O	**Port 0:** Port 0 is an open drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0 - P1.7	2 - 9	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled LOW will source current because of the internal pull-ups.
	2	I/O	• **P1.0, T2** – Timer/Counter 2 external count input/Clock out
	3	I	• **P1.1, T2EX** – Timer/Counter 2 Reload/Capture/Direction Control
	4	I	• **P1.2, ECI** – External Clock Input to the PCA
	5	I/O	• **P1.3, CEX0** – Capture/Compare External I/O for PCA module 0
	6	I/O	• **P1.4, CEX1** – Capture/Compare External I/O for PCA module 1 (with pull-up on pin)
		I/O	• **MOSI** – SPI Master Out/Slave In (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled)
	7	I/O	• **P1.5, CEX2** – Capture/Compare External I/O for PCA module 2 (with pull-up on pin)
		I/O	• **SPICLK** – SPI Clock (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled)
	8	I/O	• **P1.6, CEX3** – Capture/Compare External I/O for PCA module 3
	9	I/O	• **P1.7, CEX4** – Capture/Compare External I/O for PCA module

Table 2: Pin description…*continued*

Symbol	Pin	Type	Description
P2.0 - P2.7	24 - 31	I/O	**Port 2:** Port 2 is a 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 2 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled LOW will source current because of the internal pull-ups. (See Section 10 "Static characteristics", I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR) or 23-bit addresses (MOVX @EPTR, EMOV). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @ Ri), port 2 emits the contents of the P2 Special Function Register. Note that when 23-bit address is used, address bits A16-A22 will be outputted to P2.0-P2.6 when ALE is HIGH, and address bits A8-A14 are outputted to P2.0-P2.6 when ALE is LOW. Address bit A15 is outputted on P2.7 regardless of ALE.
P3.0 - P3.7	11,13 -19	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled LOW will source current because of the internal pull-ups.
	11	I	• **P3.0, RXD0** – Serial input port 0
	13	O	• **P3.1, TXD0** – Serial output port 0
	14	I	• **P3.2, INT0** – External interrupt 0
	15	I	• **P3.3, INT1** – External interrupt 1
	16	I	• **P3.4, T0** – Timer0 external input
	17	I	• **P3.5, T1** – Timer1 external input
	18	O	• **P3.6, $\overline{WR}$** – External data memory write strobe
	19	O	• **P3.7, $\overline{RD}$** – External data memory read strobe
P4.0 - P4.1	12,34	I/O	**Port 4:** Port 4 is an 2-bit bidirectional I/O port with internal pull-ups on all pins. Port 4 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. (Note: When SPEN, i.e.,SPCTL.6, is '1', the pull-ups at these port pins are disabled.)
	12	I	• **P4.0, RXD1** – Serial input port 1 (with pull-up on pin)
		I/O	• **MISO** – SPI Master In/Slave Out (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)

8. Functional description

8.1 Memory arrangement

P87C51MB2 has 64 kbytes of OTP (MX universal map range: 80:0000-80:FFFF), while P87C51MC2 has 96 kbytes of OTP (MX universal map range: 80:0000-81:7FFF).

The P87C51MB2 and P87C51MC2 have 2 kbytes and 3 kbytes of on-chip RAM respectively:

Table 3: Memory arrangement

Data memory		Size (bytes) and MX universal memory map range	
Type	**Description**	**P87C51MB2**	**P87C51MC2**
DATA	memory that can be addressed both directly and indirectly; can be used as stack	128 (7F:0000-7F:007F)	128 (7F:0000-7F:001F)
IDATA	superset of DATA; memory that can be addressed indirectly (where direct address for upper half is for SFR only); can be used as stack	256 (7F:0000-7F:00FF)	256 (7F:0000-7F:00FF)
EDATA	superset of DATA/IDATA; memory that can be addressed indirectly using Universal Pointers (PR0,1); can be used as stack	512 (7F:0000-7F:01FF)	512 (7F:0000-7F:01FF)
XDATA	memory (on-chip 'External Data') that is accessed via the MOVX/EMOV instructions using DPTR/EPTR	1536 (00:0000-00:05FF)	2560 (00:0000-00:09FF)

For more detailed information, please refer to the *P87C51Mx2 User Manual* or the *51MX Architecture Specification*.

8.2 Special Function Registers

Special Function Register (SFR) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0', or '1' can **only** be written and read as follows:
  - '-' MUST be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' MUST be written with '0', and will return a '0' when read.
  - '1' MUST be written with '1', and will return a '1' when read.

Table 4: Special Function Registers

Name	Description	SFR Addr.	Bit functions and addresses								Reset value
			MSB							LSB	
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0	
ACC [1]	Accumulator	E0H									00H
AUXR [2]	Auxiliary Function Register	8EH	-	-	-	-	-	-	EXTRAM	AO	00H [6]
AUXR1 [2]	Auxiliary Function Register 1	A2H	-	-	-	LPEP	GF2	0	-	DPS	00H [6]
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0	
B [1]	B Register	F0H									00H
BRGCON [2]	Baud Rate Generator Control	85H [3]	-	-	-	-	-	-	S0BRGS	BRGEN	00H [6]
BRGR0 [2][5]	Baud Rate Generator Rate LOW	86H [3]									00H
BRGR1 [2][5]	Baud Rate Generator Rate HIGH	87H [3]									00H
CCAP0H [2]	Module 0 Capture HIGH	FAH									XXH
CCAP1H [2]	Module 1 Capture HIGH	FBH									XXH
CCAP2H [2]	Module 2 Capture HIGH	FCH									XXH
CCAP3H [2]	Module 3 Capture HIGH	FDH									XXH
CCAP4H [2]	Module 4 Capture HIGH	FEH									XXH
CCAP0L [2]	Module 0 Capture LOW	EAH									XXH
CCAP1L [2]	Module 1 Capture LOW	EBH									XXH
CCAP2L [2]	Module 2 Capture LOW	ECH									XXH
CCAP3L [2]	Module 3 Capture LOW	EDH									XXH
CCAP4L [2]	Module 4 Capture LOW	EEH									XXH
CCAPM0 [2]	Module 0 Mode	DAH	-	ECOM_0	CAPP_0	CAPN_0	MAT_0	TOG_0	PWM_0	ECCF_0	00H [6]
CCAPM1 [2]	Module 1 Mode	DBH	-	ECOM_1	CAPP_1	CAPN_1	MAT_1	TOG_1	PWM_1	ECCF_1	00H [6]
CCAPM2 [2]	Module 2 Mode	DCH	-	ECOM_2	CAPP_2	CAPN_2	MAT_2	TOG_2	PWM_2	ECCF_2	00H [6]
CCAPM3 [2]	Module 3 Mode	DDH	-	ECOM_3	CAPP_3	CAPN_3	MAT_3	TOG_3	PWM_3	ECCF_3	00H [6]
CCAPM4 [2]	Module 4 Mode	DEH	-	ECOM_4	CAPP_4	CAPN_4	MAT_4	TOG_4	PWM_4	ECCF_4	00H [6]
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8	
CCON [1] [2]	PCA Counter Control	D8H	CF	CR	-	CCF4	CCF3	CCF2	CCF1	CCF0	00H [6]
CH [2]	PCA Counter HIGH	F9H									00H
CL [2]	PCA Counter LOW	E9H									00H
CMOD [2]	PCA Counter Mode	D9H	CIDL	WDTE	-	-	-	CPS1	CPS0	ECF	00H [6]

Table 4: Special Function Registers *...continued*

Name	Description	SFR Addr.	Bit functions and addresses MSB							LSB	Reset value
DPTR	Data Pointer (2 bytes)										00H
DPH	Data Pointer HIGH	83H									00H
DPL	Data Pointer LOW	82H									00H
EPTR	Extended Data Pointer (3 bytes)										
EPL [2]	Extended Data Pointer LOW	FCH[3]									00H
EPM [2]	Extended Data Pointer Middle	FDH[3]									00H
EPH [2]	Extended Data Pointer HIGH	FEH[3]									00H
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**	
IEN0 [1]	Interrupt Enable 0	A8H	$\overline{EA}$	EC	ET2	ES0/ ES0R	ET1	EX1	ET0	EX0	00H
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	$\overline{EA}$	**E9**	**E8**	
IEN1 [1]	Interrupt Enable 1	E8H	-	-	-	-	ESPI	ES1T	ES0T	ES1/ ES1R	00H[6]
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**	
IP0 [1]	Interrupt Priority	B8H	-	PPC	PT2	PS0/ PS0R	PT1	PX1	PT0	PX0	00H
IP0H	Interrupt Priority 0 HIGH	B7H	-	PPCH	PT2H	PS0H/ PS0RH	PT1H	PX1H	PT0H	PX0H	00H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**	
IP1 [1]	Interrupt Priority 1	F8H	-	-	-	-	PSPI	PS1T	PS0T	PS1/ PS1R	00H[6]
IP1H	Interrupt Priority 1 HIGH	F7H	-	-	-	-	PSPIH	PS1TH	PS0TH	PS1H/ PS1RH	00H[6]
MXCON [2]	MX Control Register	FFH[3]	-	-	-	ECRM	EAM1	EAM0	ESMM	EIFM	00H[6]
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**	
P0 [1]	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1 [1]	Port 1	90H	CEX4	CEX3	CEX2/ SPICLK	CEX1/ MOSI	CEX0	ECI	$\overline{T}$2EX	$\overline{T}$2	FFH

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Table 4: Special Function Registers *...continued*

Name	Description	SFR Addr.	Bit functions and addresses								Reset value
			MSB							LSB	
S1STAT [2]	Serial Port 1 Status	84H[3]	DBMOD_1	INTLO_1	CIDIS_1	DBISEL1	FE_1	BR_1	OE_1	STINT_1	00H[6]
SPCTL [2]	SPI Control Register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	PSC1	PSC0	00H[6]
SPCFG [2]	SPI Configuration Register	E1H	SPIF	SPWCOL	-	-	-	-	-	-	00H[6]
SPDAT [2]	SPI Data	E3H									00H
SP	Stack Pointer (or Stack Pointer LOW Byte When EDATA Supported)	81H									07H
SPE [2]	Stack Pointer HIGH	FBH[3]									00H
		Bit address	**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**	
TCON [1]	Timer Control Register	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON [1] [2]	Timer2 Control Register	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
T2MOD [2]	Timer2 Mode Control	C9H	-	-	ENT2	TF2DE	T2GATE	T2PWME	T2OE	DCEN	00H[6]
TH0	Timer 0 HIGH	8CH									00H
TH1	Timer 1 HIGH	8DH									00H
TH2	Timer 2 HIGH	CDH									00H
TL0	Timer 0 LOW	8AH									00H
TL1	Timer 1 LOW	8BH									00H
TL2	Timer 2 LOW	CCH									00H
TMOD	Timer 0 and 1 Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
WDTRST [2]	Watchdog Timer Reset	A6H									FFH
WDCON [2]	Watchdog Timer Control	8FH[3]	-	-	-	-	-	WDPRE2	WDPRE1	WDPRE0	00H[6]

[1] SFRs are bit addressable.

[2] SFRs are modified from or added to the 80C51 SFRs.

[3] Extended SFRs accessed by preceding the instruction with MX escape (opcode A5h).

[4] Power on reset is 10H. Other reset is 00H.

[5] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is '0'. If any of them is written if BRGEN = 1, result is unpredictable.

[6] The unimplemented bits (labeled '-') in the SFRs are X's (unknown) at all times. '1's should **not** be written to these bits, as they may be used for other purposes in future derivatives. The reset values shown for these bits are '0's although they are unknown when read.

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8.3 Security bits

The P87C51Mx2 has security bits to protect users' firmware codes. With none of the security bits programmed, the code in the program memory can be verified. When only security bit 1 (see Table 5) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. $\overline{EA}$ is latched on Reset and all further programming of EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Table 5: EPROM security bits

Security Bits[1][2]				
	Bit 1	**Bit 2**	**Bit 3**	**Protection description**
1	U	U	U	No program security features enabled. EEPROM is programmable and verifiable.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verification is disabled.
4	P	P	P	Same as 3, external execution is disabled.

[1] P - programmed. U - unprogrammed.

[2] Any other combination of security bits is not defined.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	operating temperature	under bias	0	+70	°C
T_{stg}	storage temperature range		–65	+150	°C
V_I	input voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}		0	+13	V
	input voltage on any other pin to V_{SS}		–0.5	V_{DD}+ 0.5 V	V
I_I, I_O	maximum I_{OL} per I/O pin		-	20	mA
P	power dissipation	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to the Limiting values:

a) Stresses above those listed under Limiting values may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Section 10 "Static characteristics" and Section 11 "Dynamic characteristics" of this specification is not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 7: Static characteristics

T_{amb} = 0 °C to +70 °C for commercial, unless otherwise specified; V_{DD} = 2.7 V to 5.5 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IL}	Input low voltage		–0.5		$0.2V_{DD}$–0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, 4, $\overline{EA}$)		$0.2V_{DD}$+0.9		V_{DD}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{DD}$		V_{DD}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3, 4[8]	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	-		0.4	V
		V_{DD} = 2.7 V, I_{OL} = 1.6 mA				
V_{OL1}	Output LOW voltage, port 0, ALE, $\overline{PSEN}$[7][8]	V_{DD} = 4.5 V, I_{OL} = 3.2 mA	-		0.4	V
		V_{DD} = 2.7 V, I_{OL} = 3.2 mA				
V_{OH}	Output high voltage, ports 1, 2, 3, 4	V_{DD} = 4.5 V, I_{OH} = –30 A	V_{DD} – 0.7		-	V
		V_{DD} = 2.7 V, I_{OH} = –10 A			-	
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{DD} = 4.5 V, I_{OH} = –3.2 mA	V_{DD} – 0.7		-	V
		V_{DD} = 2.7 V, I_{OH} = –3.2 mA				
I_{IL}	Logical 0 input current, ports 1, 2, 3, 4	V_{IN} = 0.4 V	–1		–75	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, 4[8]	4.5 V < V_{DD} < 5.5 V, V_{IN} = 2.0 V [4]	-		–650	µA
I_{L1}	Input leakage current, port 0	0.45 < V_{IN} < V_{DD}–0.3	-		10	µA
I_{CC}	Power supply current	[5]	-			
	Active mode[5]	V_{DD} = 5.5 V	-		7 + 2.7 /MHz × f_{osc}	mA
		V_{DD} = 3.6 V	-		4 + 1.3 /MHz × f_{osc}	
	Idle mode[5]	V_{DD} = 5.5 V	-		4 + 1.3 /MHz × f_{osc}	mA
		V_{DD} = 3.6 V	-		1 + 1.0 /MHz × f_{osc}	
	Power-down mode or clock stopped (see Figure 16 for conditions)	V_{DD} = 5.0 V	-	20	-	µA
		V_{DD} = 5.5 V	-		100	µA
R_{RST}	Internal reset pull-down resistor		40		225	kΩ
C_{10}	Pin capacitance[10] (except $\overline{EA}$)		-		15	pF

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), 5 V, unless otherwise stated.

[2] Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} of ALE and ports 1, 3 and 4. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading >100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.

[3] Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{DD}–0.7 V specification when the address bits are stabilizing.

[4] Pins of ports 1, 2, 3 and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2 V for 4.5 V < V_{DD} < 5.5 V.

[5] See Figure 13 through Figure 16 for I_{CC} test conditions. f_{osc} is the oscillator frequency in MHz.

[6] This value applies to T_{amb} = 0 °C to +70 °C.

[7] Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[8] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per port pin: 15 mA

b) Maximum I_{OL} per 8-bit port: 26 mA

c) Maximum total I_{OL} for all outputs: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[9] ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.

[10] Pin capacitance is characterized but not tested.

11. Dynamic characteristics

Table 8: Dynamic characteristics

T_{amb} = 0 to +70 °C for commercial unless otherwise specified. Formulae including t_{CLCL} assume oscillator signal with 50/50 duty cycle.[1][2][3]

Symbol	Fig	Parameter	2.7 V < V_{DD} < 5.5 V				4.5 V < V_{DD} < 5.5 V				Unit
			Variable clock[4]		f_{OSC} = 12 MHz[4]		Variable clock[4]		f_{OSC} = 24 MHz[4]		
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{OSC}	4	Oscillator frequency	0	12		-	0	24		-	MHz
t_{CLCL}	4	Clock cycle	-	-	83	-		-	41.5	-	ns
t_{LHLL}	4	ALE pulse width	t_{CLCL}–15	-	68	-	t_{CLCL}–15	-	26	-	ns
t_{AVLL}	4, 5, 6	Address valid to ALE LOW	0.5t_{CLCL}–15	-	8	-	0.5t_{CLCL}–15	-	5	-	ns
t_{LLAX}	4, 5, 6	Address hold after ALE LOW	0.5t_{CLCL}–25	-	16	-	0.5t_{CLCL}–15	-	5	-	ns
t_{LLIV}	4	ALE LOW to valid instruction in	-	0.5t_{CLCL}–25		121	-	2t_{CLCL} – 30		53	ns
t_{LLPL}	4	ALE LOW to $\overline{PSEN}$ LOW	0.5t_{CLCL}–25	-	16	-	0.5t_{CLCL}–12	-	8	-	ns
t_{PLPH}	4	$\overline{PSEN}$ pulse width	1.5t_{CLCL}–25	-	100	-	1.5t_{CLCL}–20	-	42	-	ns
t_{PLIV}	4	$\overline{PSEN}$ LOW to valid instruction in	-	1.5t_{CLCL}–45	-	80	-	1.5t_{CLCL}–35		27	ns
t_{PXIX}	4	Input instruction hold after $\overline{PSEN}$	0	-	0	-	0	-	0	-	ns
t_{PXIZ}	4	Input instruction float after $\overline{PSEN}$	-	0.5t_{CLCL}–10	-	31	-	0.5t_{CLCL}–5	-	15	ns
t_{AVIV}	4	Address to valid instruction in (non-Extended Addressing Mode)	-	2.5t_{CLCL}–35	-	173	-	2.5t_{CLCL}–30	-	74	ns
t_{AVIV1}	4	Address (A16-A22) to valid instruction in (Extended Addressing Mode)	-	1.5t_{CLCL}–44	-	81	-	1.5t_{CLCL}–34	-	28	ns
t_{PLAZ}	4	$\overline{PSEN}$ LOW to address float	-	16	-	16	-	8	-	8	ns

Table 8: Dynamic characteristics *...continued*

T_{amb} = 0 to +70 °C for commercial unless otherwise specified. Formulae including t_{CLCL} assume oscillator signal with 50/50 duty cycle.[1][2][3]

Symbol	Fig	Parameter	2.7 V < V_{DD} < 5.5 V				4.5 V < V_{DD} < 5.5 V				Unit
			Variable clock[4]		f_{OSC} = 12 MHz[4]		Variable clock[4]		f_{OSC} = 24 MHz[4]		
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Memory											
t_{RLRH}	5	$\overline{RD}$ pulse width	$3t_{CLCL}-25$	-	225	-	$3t_{CLCL}-20$	-	105	-	ns
t_{WLWH}	6	$\overline{WR}$ pulse width	$3t_{CLCL}-25$	-	225	-	$3t_{CLCL}-20$	-	105	-	ns
t_{RLDV}	5	$\overline{RD}$ LOW to valid data in	-	$2.5t_{CLCL}-55$	-	153	-	$2.5t_{CLCL}-40$	-	64	ns
t_{RHDX}	5	Data hold after $\overline{RD}$	0	-	0	-	0	-	0	-	ns
t_{RHDZ}	5	Data float after $\overline{RD}$	-	$t_{CLCL}-20$	-	63	-	$t_{CLCL}-15$	-	26	ns
t_{LLDV}	5	ALE LOW to valid data in	-	$4t_{CLCL}-50$	-	283	-	$4t_{CLCL}-35$	-	131	ns
t_{AVDV}	5	Address to valid data in (non-Extended Addressing Mode)	-	$4.5t_{CLCL}-40$	-	335	-	$4.5t_{CLCL}-30$	-	157	ns
t_{AVDV1}	5	Address (A16-A22) to valid data in (Extended Addressing Mode)	-	$3.5t_{CLCL}-45$	-	246	-	$3.5t_{CLCL}-35$	-	110	ns
t_{LLWL}	5, 6	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	$1.5t_{CLCL}-5$	$1.5t_{CLCL}+20$	120	145	$1.5t_{CLCL}-10$	$1.5t_{CLCL}+20$	52	82	ns
t_{AVWL}	5, 6	Address valid to $\overline{WR}$ or $\overline{RD}$ LOW (non-Extended Addressing Mode)	$2t_{CLCL}-5$	-	161	-	$2t_{CLCL}-5$	-	78	-	ns
t_{AVWL1}	5, 6	Address (A16-A22) valid to $\overline{WR}$ or $\overline{RD}$ LOW (Extended Addressing Mode)	$t_{CLCL}-10$	-	73	-	$t_{CLCL}-10$	-	31	-	ns
t_{QVWX}	6	Data valid to $\overline{WR}$ transition	$0.5t_{CLCL}-20$	-	21	-	$0.5t_{CLCL}-15$	-	5	-	ns
t_{WHQX}	6	Data hold after $\overline{WR}$	$0.5t_{CLCL}-25$	-	16	-	$0.5t_{CLCL}-11$	-	9	-	ns
t_{QVWH}	6	Data valid to WR HIGH	$3.5t_{CLCL}-10$	-	281	-	$3.5t_{CLCL}-10$	-	135	-	ns

Table 8: Dynamic characteristics *...continued*

T_{amb} = 0 to +70 °C for commercial unless otherwise specified. Formulae including t_{CLCL} assume oscillator signal with 50/50 duty cycle.[1][2][3]

Symbol	Fig	Parameter	2.7 V < V_{DD} < 5.5 V				4.5 V < V_{DD} < 5.5 V				Unit
			Variable clock[4]		f_{OSC} = 12 MHz[4]		Variable clock[4]		f_{OSC} = 24 MHz[4]		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SPILEAD}$	10, 11	Enable lead time (Slave)									ns
		2.0 MHz	250	-	250	-	250	-	250	-	
		3.0 MHz	240	-	240	-	240	-	240	-	
t_{SPILAG}	10, 11	Enable lag time (Slave)									ns
		2.0 MHz	250	-	250	-	250	-	250	-	
		3.0 MHz	240	-	240	-	240	-	240	-	
$t_{SPICLKH}$	8, 9, 10, 11	SPICLK HIGH time									ns
		Master	340	-	340	-	340	-	340	-	
		Slave	190	-	190	-	190	-	190	-	
$t_{SPICLKL}$	8, 9, 10, 11	SPICLK LOW time									ns
		Master	340	-	340	-	340	-	340	-	
		Slave	190	-	190	-	190	-	190	-	
t_{SPIDSU}	8, 9, 10, 11	Data setup time (Master or Slave)	100	-	100	-	100	-	100	-	ns
t_{SPIDH}	8, 9, 10, 11	Data hold time (Master or Slave)	100	-	100	-	100	-	100	-	ns
t_{SPIA}	10, 11	Access time (Slave)	0	120	0	120	0	120	0	120	ns
t_{SPIDIS}	10, 11	Disable time (Slave)									ns
		2.0 MHz	0	240	-	240	0	240	-	240	
		3.0 MHz	0	167	-	167	0	167	-	167	
t_{SPIDV}	8, 9, 10, 11	Enable to output data valid									ns
		2.0 MHz	-	240	-	240	-	240	-	240	
		3.0 MHz	-	167	-	167	-	167	-	167	
t_{SPIOH}	8, 9, 10, 11	Output data hold time	0	-	0	-	0	-	0	-	ns

11.1 Explanation of AC symbols

Each timing symbol has five characters. The first character is always ‘t’ (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A — Address

C — Clock

D — Input data

H — Logic level HIGH

I — Instruction (program memory contents)

L — Logic level LOW, or ALE

P — $\overline{\text{PSEN}}$

Q — Output data

R — $\overline{\text{RD}}$ signal

t — Time

V — Valid

W — $\overline{\text{WR}}$ signal

X — No longer a valid logic level

Z — Float

Examples:

$\mathbf{t_{AVLL}}$ **—** Time for address valid to ALE LOW

$\mathbf{t_{LLPL}}$ **—** Time for ALE LOW to $\overline{\text{PSEN}}$ LOW

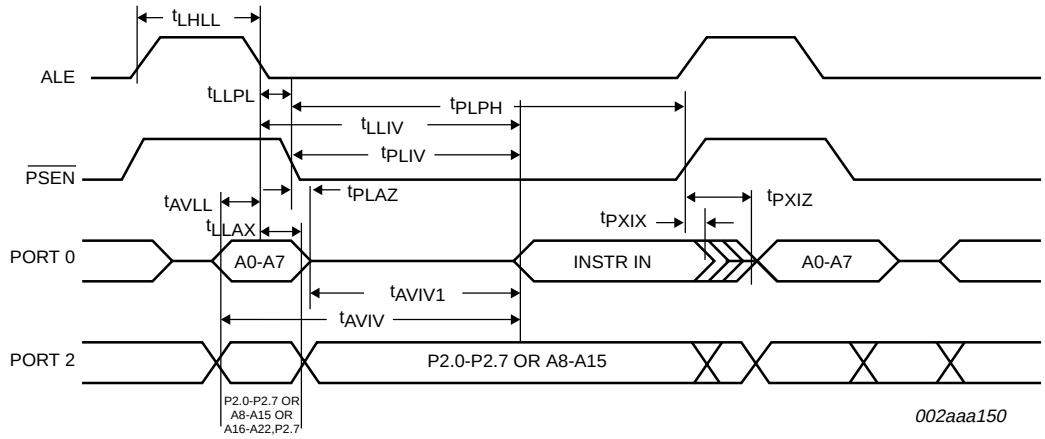


Fig 4. External program memory read cycle (extended memory cycle).

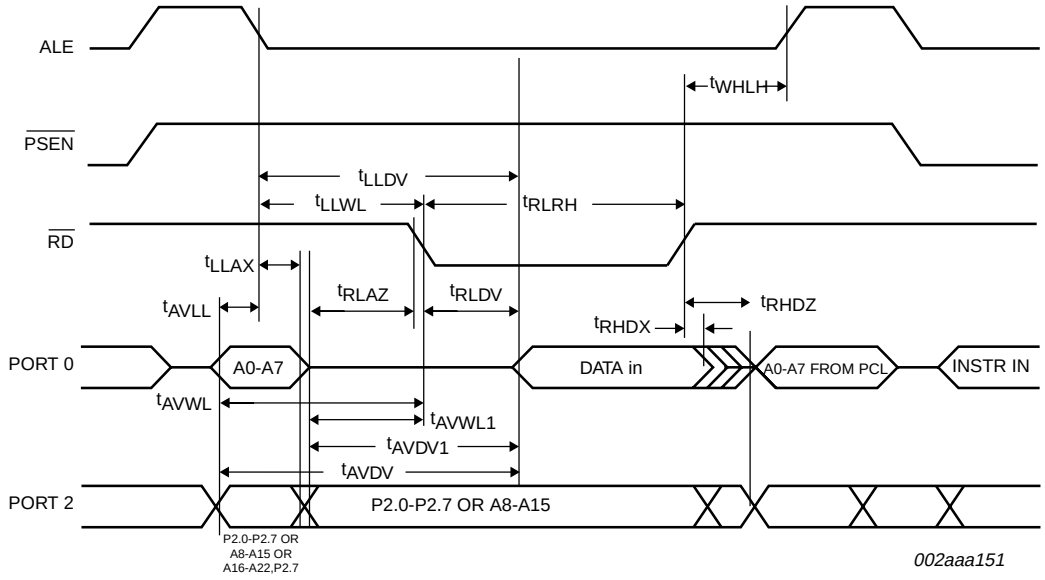


Fig 5. External data memory read cycle.

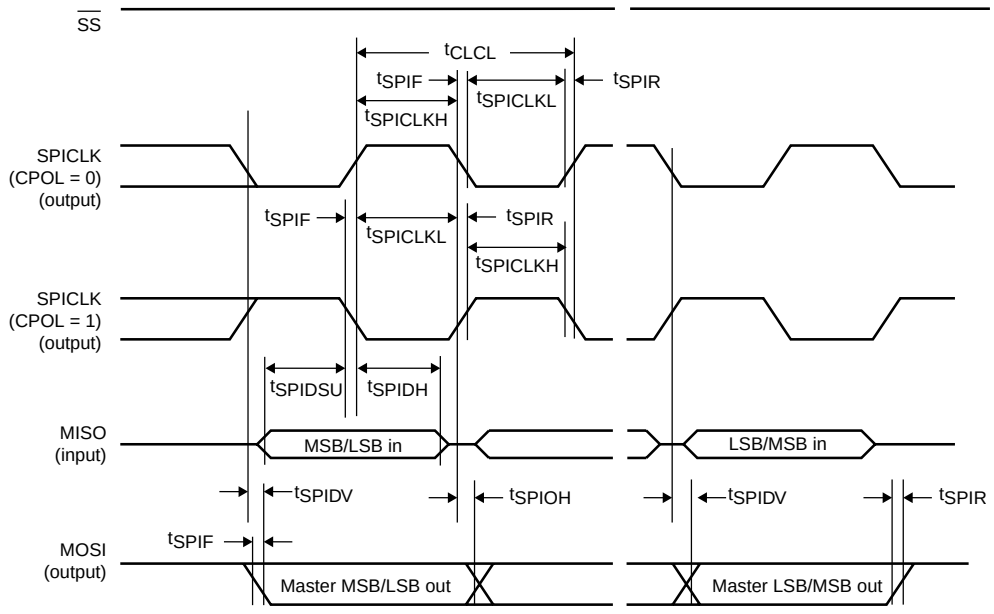


Fig 8. SPI master timing (CPHA = 0).

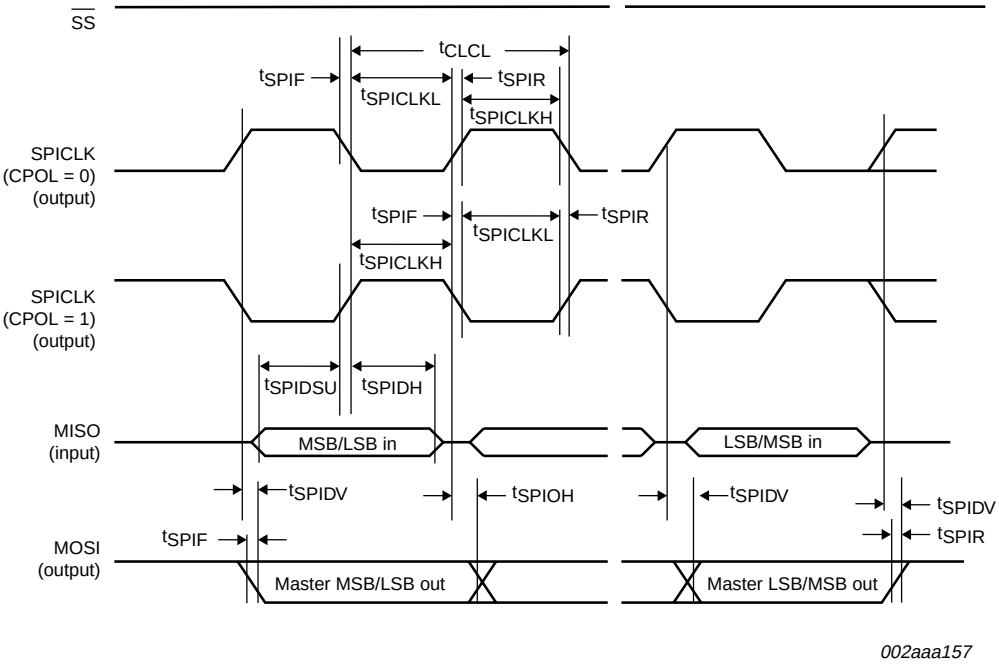
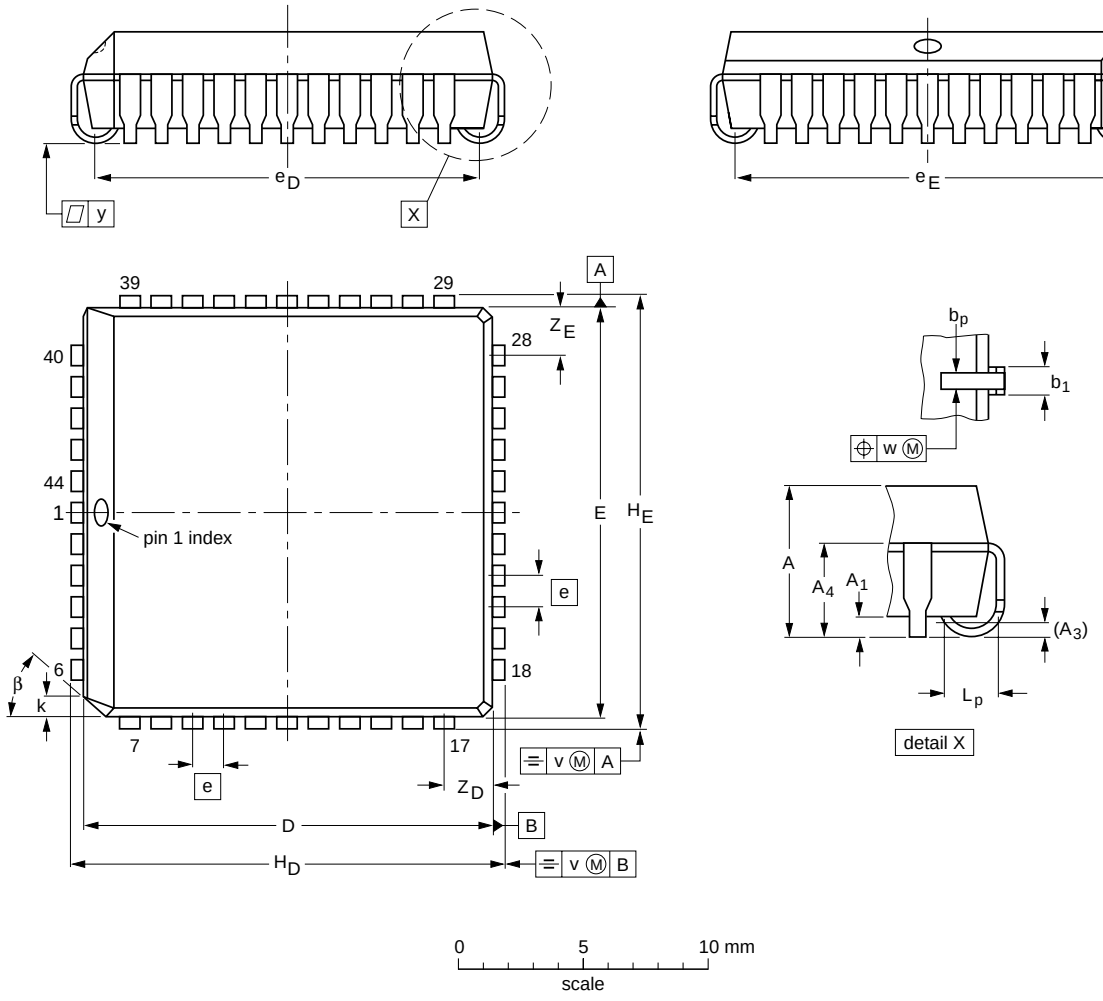


Fig 9. SPI master timing (CPHA = 1).

12. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 17. SOT187-2.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 10: Revision history

Rev	Date	CPCN	Description
03	20031113	-	**Product data (9397 750 12302); ECN 853-2426 01-A14402 dated 6 November 2003** Modifications: • Figure 5 “External data memory read cycle.” on page 24; added t_{RLDV}, removed ‘non-extended memory cycle’ from figure title. • Figure 6 “External data memory write cycle.” on page 25; removed ‘non-extended memory cycle’ from figure title.
02	20030519	-	**Product data (9397 750 11517)**
_1	20010406	-	**Preliminary specification (9397 750 08199)**