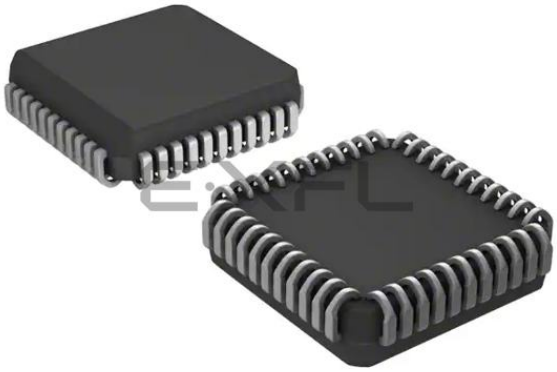

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87c51mc2ba-02-529

- New 23-bit extended data pointer and two 24-bit universal pointers greatly improve C compiler code efficiency in using pointers to access variables in different spaces

- 100% binary compatibility with the classic 80C51 so that existing code is completely reusable
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 kbytes (MC2) or 64 kbytes (MB2) of on-chip OTP
- 3 kbytes (MC2) or 2 kbytes (MB2) of on-chip RAM
- Programmable Counter Array (PCA)
- Two full-duplex enhanced UARTs and Serial Peripheral Interface (SPI) communication modules

2.2 Key benefits

- Increases program/data address range to 8 Mbytes each
- Enhances performance and efficiency for C programs
- Fully 80C51-compatible microcontroller
- Provides seamless and compelling upgrade path from classic 80C51
- Preserves 80C51 code base, investment/knowledge, and peripherals & ASICs
- Supported by wide range of 80C51 development systems and programming tools vendors
- The P87C51Mx2 makes it possible to develop applications at lower cost and with a reduced time-to-market

2.3 Complete features

- Fully static
- Up to 24 MHz CPU clock with 6 clock cycles per machine cycle
- 96 kbytes or 64 kbytes of on-chip OTP
- 3 kbytes or 2 kbytes of on-chip RAM
- 23-bit program memory space and 23-bit data memory space
- Four-level interrupt priority
- 34 I/O lines (5 ports)
- Three Timers: Timer0, Timer1 and Timer2
- Two full-duplex enhanced UARTs with baud rate generator
- Framing error detection
- Automatic address recognition
- Supports industry-standard Serial Peripheral Interface (SPI) with a baud rate up to 6 Mbits/s
- Power control modes
- Clock can be stopped and resumed
- Idle mode
- Power down mode with advanced clock control
- Second DPTR register
- Asynchronous port reset
- Programmable Counter Array (PCA) (compatible with 8xC51Rx+) with five Capture/Compare modules

- Low EMI (inhibit ALE)
- Watchdog timer with programmable prescaler for different time ranges (compatible with 8xC66x with added prescaler)

3. Differences between P87C51MX2/02 part and previous revisions of P87C51MX2

The P87C51MX2/02 offers several advantages over the previous generation of P87C51MX2 parts. Right now, SPI module is available, two more general purpose digital pins on P4 are present and additional power control features are implemented (advanced peripheral clock control). New memory interface mode and code size optimization options are available with the use of MXCON register.

No changes are necessary when porting and loading code written for existing P87C51MX2 to the new P87C51MX2/02.

4. Ordering information

Table 1: Ordering information

Type number	Memory		Temp Range (°C)	V_{DD} voltage range	Frequency		Package		
	OTP	RAM			V_{DD} = 2.7 to 5.5 V	V_{DD} = 4.5 to 5.5 V	Name	Description	Version
P87C51MB2BA/02	64 kB	2048 B	0 to +70	2.7 to 5.5 V	0 to 12 MHz	0 to 24 MHz	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2
P87C51MC2BA/02	96 kB	3072 B	0 to +70	2.7 to 5.5 V	0 to 12 MHz	0 to 24 MHz	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

5. Block diagram

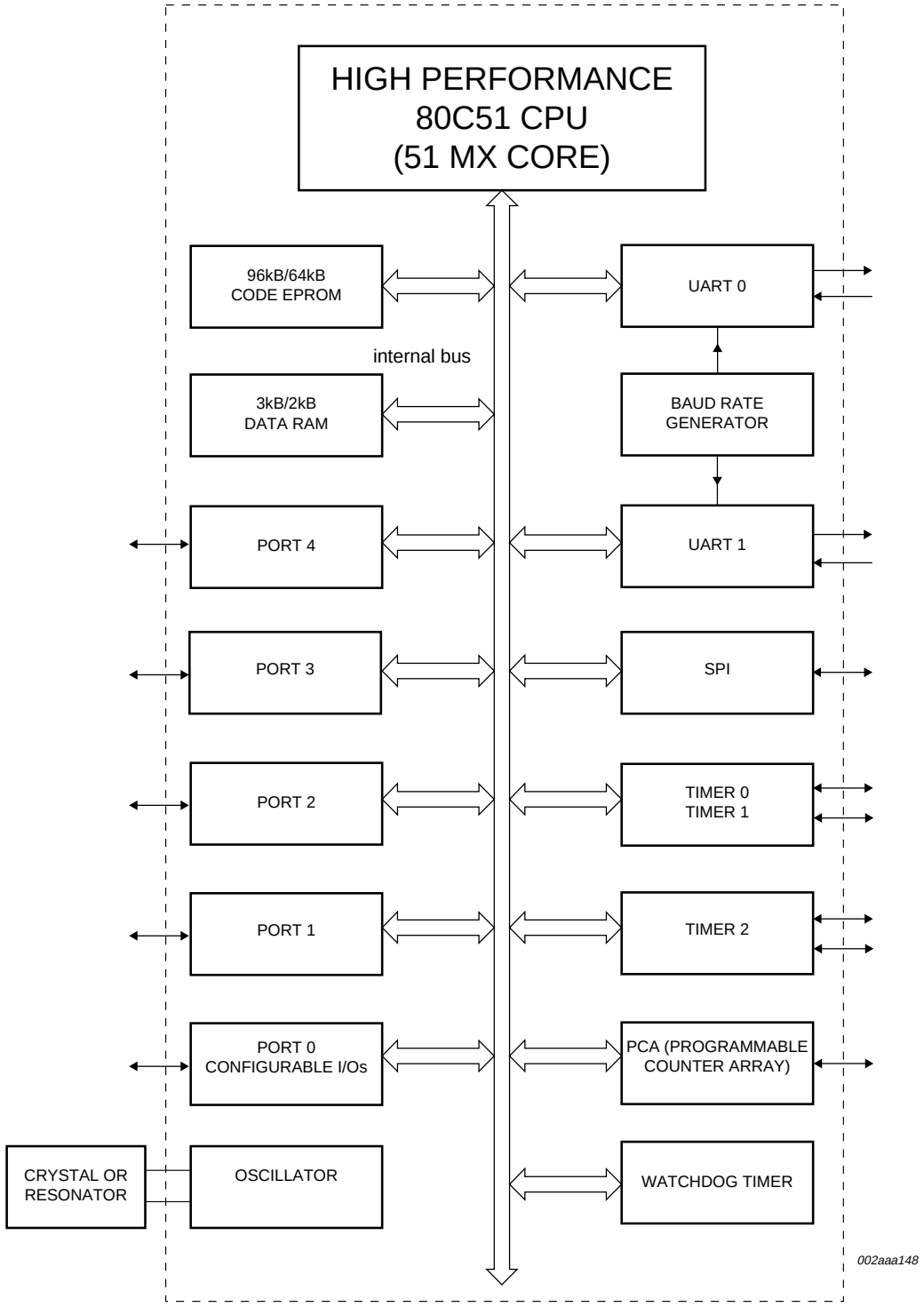

Fig 1. Block diagram.

6. Functional diagram

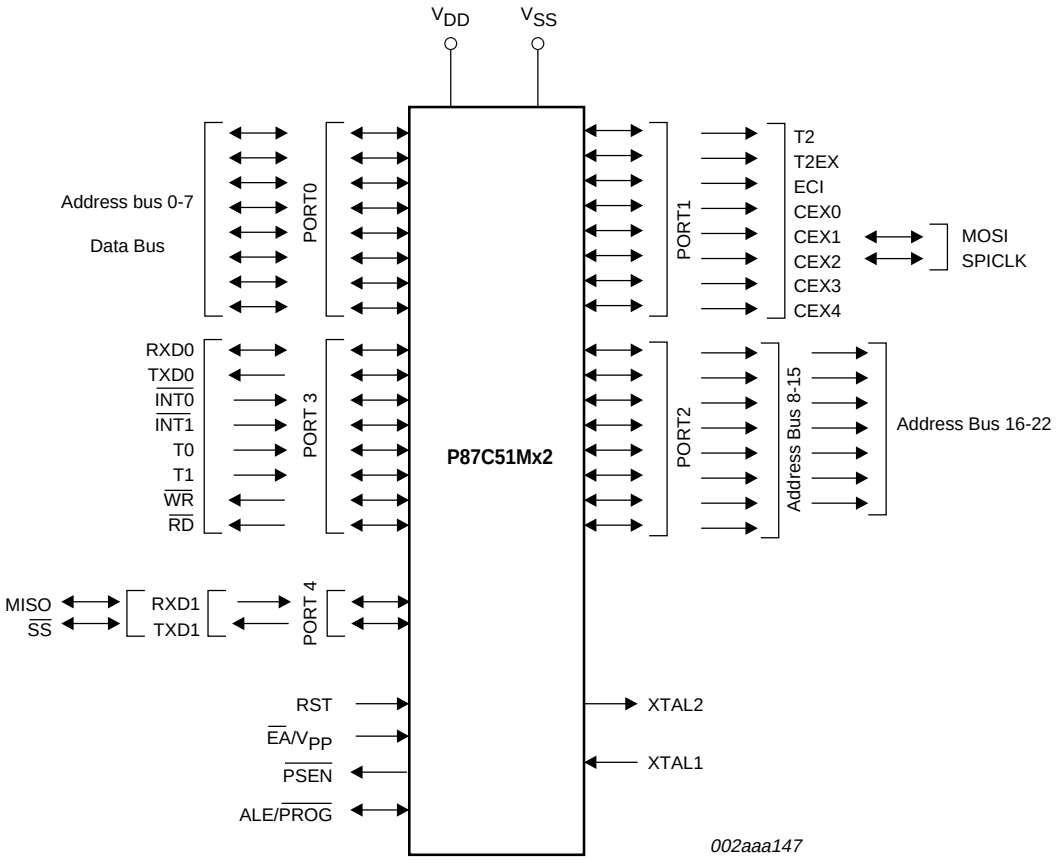

Fig 2. Functional diagram.

7.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
P0.0 - P0.7	43 - 36	I/O	**Port 0:** Port 0 is an open drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0 - P1.7	2 - 9	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled LOW will source current because of the internal pull-ups.
	2	I/O	• **P1.0, T2** – Timer/Counter 2 external count input/Clock out
	3	I	• **P1.1, T2EX** – Timer/Counter 2 Reload/Capture/Direction Control
	4	I	• **P1.2, ECI** – External Clock Input to the PCA
	5	I/O	• **P1.3, CEX0** – Capture/Compare External I/O for PCA module 0
	6	I/O	• **P1.4, CEX1** – Capture/Compare External I/O for PCA module 1 (with pull-up on pin)
		I/O	• **MOSI** – SPI Master Out/Slave In (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled)
	7	I/O	• **P1.5, CEX2** – Capture/Compare External I/O for PCA module 2 (with pull-up on pin)
		I/O	• **SPICLK** – SPI Clock (Selected when SPEN (SPCTL.6) is ‘1’, in which case the pull-up for this pin is disabled)
	8	I/O	• **P1.6, CEX3** – Capture/Compare External I/O for PCA module 3
	9	I/O	• **P1.7, CEX4** – Capture/Compare External I/O for PCA module

Table 2: Pin description…*continued*

Symbol	Pin	Type	Description
P2.0 - P2.7	24 - 31	I/O	**Port 2:** Port 2 is a 8-bit bidirectional I/O port with internal pull-ups on all pins. Port 2 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled LOW will source current because of the internal pull-ups. (See Section 10 "Static characteristics", I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR) or 23-bit addresses (MOVX @EPTR, EMOV). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @ Ri), port 2 emits the contents of the P2 Special Function Register. Note that when 23-bit address is used, address bits A16-A22 will be outputted to P2.0-P2.6 when ALE is HIGH, and address bits A8-A14 are outputted to P2.0-P2.6 when ALE is LOW. Address bit A15 is outputted on P2.7 regardless of ALE.
P3.0 - P3.7	11,13 -19	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled LOW will source current because of the internal pull-ups.
	11	I	• **P3.0, RXD0** – Serial input port 0
	13	O	• **P3.1, TXD0** – Serial output port 0
	14	I	• **P3.2, INT0** – External interrupt 0
	15	I	• **P3.3, INT1** – External interrupt 1
	16	I	• **P3.4, T0** – Timer0 external input
	17	I	• **P3.5, T1** – Timer1 external input
	18	O	• **P3.6, $\overline{WR}$** – External data memory write strobe
	19	O	• **P3.7, $\overline{RD}$** – External data memory read strobe
P4.0 - P4.1	12,34	I/O	**Port 4:** Port 4 is an 2-bit bidirectional I/O port with internal pull-ups on all pins. Port 4 pins that have 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. As inputs, port 4 pins that are externally pulled LOW will source current because of the internal pull-ups. (Note: When SPEN, i.e.,SPCTL.6, is '1', the pull-ups at these port pins are disabled.)
	12	I	• **P4.0, RXD1** – Serial input port 1 (with pull-up on pin)
		I/O	• **MISO** – SPI Master In/Slave Out (Selected when SFR bit SPEN (SPCTL.6) is '1', in which case the pull-up for this pin is disabled)

8. Functional description

8.1 Memory arrangement

P87C51MB2 has 64 kbytes of OTP (MX universal map range: 80:0000-80:FFFF), while P87C51MC2 has 96 kbytes of OTP (MX universal map range: 80:0000-81:7FFF).

The P87C51MB2 and P87C51MC2 have 2 kbytes and 3 kbytes of on-chip RAM respectively:

Table 3: Memory arrangement

Data memory		Size (bytes) and MX universal memory map range	
Type	**Description**	**P87C51MB2**	**P87C51MC2**
DATA	memory that can be addressed both directly and indirectly; can be used as stack	128 (7F:0000-7F:007F)	128 (7F:0000-7F:001F)
IDATA	superset of DATA; memory that can be addressed indirectly (where direct address for upper half is for SFR only); can be used as stack	256 (7F:0000-7F:00FF)	256 (7F:0000-7F:00FF)
EDATA	superset of DATA/IDATA; memory that can be addressed indirectly using Universal Pointers (PR0,1); can be used as stack	512 (7F:0000-7F:01FF)	512 (7F:0000-7F:01FF)
XDATA	memory (on-chip 'External Data') that is accessed via the MOVX/EMOV instructions using DPTR/EPTR	1536 (00:0000-00:05FF)	2560 (00:0000-00:09FF)

For more detailed information, please refer to the *P87C51Mx2 User Manual* or the *51MX Architecture Specification*.

8.2 Special Function Registers

Special Function Register (SFR) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0', or '1' can **only** be written and read as follows:
  - '-' MUST be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' MUST be written with '0', and will return a '0' when read.
  - '1' MUST be written with '1', and will return a '1' when read.

Table 4: Special Function Registers *...continued*

Name	Description	SFR Addr.	Bit functions and addresses MSB							LSB	Reset value
DPTR	Data Pointer (2 bytes)										00H
DPH	Data Pointer HIGH	83H									00H
DPL	Data Pointer LOW	82H									00H
EPTR	Extended Data Pointer (3 bytes)										
EPL [2]	Extended Data Pointer LOW	FCH[3]									00H
EPM [2]	Extended Data Pointer Middle	FDH[3]									00H
EPH [2]	Extended Data Pointer HIGH	FEH[3]									00H
		Bit address	**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**	
IEN0 [1]	Interrupt Enable 0	A8H	$\overline{EA}$	EC	ET2	ES0/ ES0R	ET1	EX1	ET0	EX0	00H
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	$\overline{EA}$	**E9**	**E8**	
IEN1 [1]	Interrupt Enable 1	E8H	-	-	-	-	ESPI	ES1T	ES0T	ES1/ ES1R	00H[6]
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**	
IP0 [1]	Interrupt Priority	B8H	-	PPC	PT2	PS0/ PS0R	PT1	PX1	PT0	PX0	00H
IP0H	Interrupt Priority 0 HIGH	B7H	-	PPCH	PT2H	PS0H/ PS0RH	PT1H	PX1H	PT0H	PX0H	00H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**	
IP1 [1]	Interrupt Priority 1	F8H	-	-	-	-	PSPI	PS1T	PS0T	PS1/ PS1R	00H[6]
IP1H	Interrupt Priority 1 HIGH	F7H	-	-	-	-	PSPIH	PS1TH	PS0TH	PS1H/ PS1RH	00H[6]
MXCON [2]	MX Control Register	FFH[3]	-	-	-	ECRM	EAM1	EAM0	ESMM	EIFM	00H[6]
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**	
P0 [1]	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1 [1]	Port 1	90H	CEX4	CEX3	CEX2/ SPICLK	CEX1/ MOSI	CEX0	ECI	$\overline{T}$2EX	$\overline{T}$2	FFH

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8.3 Security bits

The P87C51Mx2 has security bits to protect users' firmware codes. With none of the security bits programmed, the code in the program memory can be verified. When only security bit 1 (see Table 5) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. $\overline{EA}$ is latched on Reset and all further programming of EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Table 5: EPROM security bits

Security Bits[1][2]				
	Bit 1	**Bit 2**	**Bit 3**	**Protection description**
1	U	U	U	No program security features enabled. EEPROM is programmable and verifiable.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on Reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verification is disabled.
4	P	P	P	Same as 3, external execution is disabled.

[1] P - programmed. U - unprogrammed.

[2] Any other combination of security bits is not defined.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{amb}	operating temperature	under bias	0	+70	°C
T_{stg}	storage temperature range		–65	+150	°C
V_I	input voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}		0	+13	V
	input voltage on any other pin to V_{SS}		–0.5	V_{DD}+ 0.5 V	V
I_I, I_O	maximum I_{OL} per I/O pin		-	20	mA
P	power dissipation	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to the Limiting values:

a) Stresses above those listed under Limiting values may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Section 10 "Static characteristics" and Section 11 "Dynamic characteristics" of this specification is not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[6] This value applies to T_{amb} = 0 °C to +70 °C.

[7] Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100 pF, load capacitance for all other outputs = 80 pF.

[8] Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

a) Maximum I_{OL} per port pin: 15 mA

b) Maximum I_{OL} per 8-bit port: 26 mA

c) Maximum total I_{OL} for all outputs: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

[9] ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.

[10] Pin capacitance is characterized but not tested.

Table 8: Dynamic characteristics...*continued*

T_{amb} = 0 to +70 °C for commercial unless otherwise specified. Formulae including t_{CLCL} assume oscillator signal with 50/50 duty cycle.[1][2][3]

Symbol	Fig	Parameter	2.7 V < V_{DD} < 5.5 V				4.5 V < V_{DD} < 5.5 V				Unit
			Variable clock[4]		f_{OSC} = 12 MHz[4]		Variable clock[4]		f_{OSC} = 24 MHz[4]		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{RLAZ}	5	$\overline{RD}$ LOW to address float	-	0	-	0	-	0	-	0	ns
t_{WHLH}	5, 6	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	$0.5t_{CLCL}-20$	$0.5t_{CLCL}+10$	21	51	$0.5t_{CLCL}-11$	$0.5t_{CLCL}+10$	9	30	ns
External Clock											
t_{CHCX}	12	HIGH time	33	$t_{CLCL}-t_{CLCX}$	33	-	16	$t_{CLCL}-t_{CLCX}$	16	-	ns
t_{CLCX}	12	LOW time	33	$t_{CLCL}-t_{CHCX}$	33	-	16	$t_{CLCL}-t_{CHCX}$	16	-	ns
t_{CLCH}	12	Rise time	-	8	-	8	-	4	-	4	ns
t_{CHCL}	12	Fall Time	-	8	-	8	-	4	-	4	ns
Shift Register											
t_{XLXL}	7	Serial port clock cycle time	$6t_{CLCL}$	-	500	-	$t_{CLCL}-t_{CLCX}$	-	250	-	ns
t_{QVXH}	7	Output data setup to clock rising edge	$5t_{CLCL}-10$	-	406	-	$t_{CLCL}-t_{CHCX}$	-	198	-	ns
t_{XHQX}	7	Output data hold after clock rising edge	$t_{CLCL}-10$	-	68	-	$t_{CLCL}-15$	-	26	-	ns
t_{XHDX}	7	Input data hold after clock rising edge	0	-	0	-	0	-	0	-	ns
t_{XHDV}	7	Clock rising edge to input data valid	-	$5t_{CLCL}-55$	-	361	-	$5t_{CLCL}-35$	-	173	ns
SPI Interface											
f_{SPI}											MHz
			-	-	-	-	-	-	-	-	
			0	2.0	0	2.0	0	2.0	0	2.0	
			-	-	-	-	-	-	-	-	
			0	3.0	0	3.0	0	3.0	0	3.0	
t_{SPICYC}	8, 9, 10, 11	Cycle time									ns
		2.0 MHz (Master)	-	-	-	-	-	-	-	-	
		2.0 MHz (Slave)	500	-	500	-	500	-	500	-	
		3.0 MHz (Master)	-	-	-	-	-	-	-	-	
		3.0 MHz (Slave)	333	-	333	-	333	-	333	-	

Table 8: Dynamic characteristics *...continued*

T_{amb} = 0 to +70 °C for commercial unless otherwise specified. Formulae including t_{CLCL} assume oscillator signal with 50/50 duty cycle.[1][2][3]

Symbol	Fig	Parameter	2.7 V < V_{DD} < 5.5 V				4.5 V < V_{DD} < 5.5 V				Unit
			Variable clock[4]		f_{OSC} = 12 MHz[4]		Variable clock[4]		f_{OSC} = 24 MHz[4]		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SPILEAD}$	10, 11	Enable lead time (Slave)									ns
		2.0 MHz	250	-	250	-	250	-	250	-	
		3.0 MHz	240	-	240	-	240	-	240	-	
t_{SPILAG}	10, 11	Enable lag time (Slave)									ns
		2.0 MHz	250	-	250	-	250	-	250	-	
		3.0 MHz	240	-	240	-	240	-	240	-	
$t_{SPICLKH}$	8, 9, 10, 11	SPICLK HIGH time									ns
		Master	340	-	340	-	340	-	340	-	
		Slave	190	-	190	-	190	-	190	-	
$t_{SPICLKL}$	8, 9, 10, 11	SPICLK LOW time									ns
		Master	340	-	340	-	340	-	340	-	
		Slave	190	-	190	-	190	-	190	-	
t_{SPIDSU}	8, 9, 10, 11	Data setup time (Master or Slave)	100	-	100	-	100	-	100	-	ns
t_{SPIDH}	8, 9, 10, 11	Data hold time (Master or Slave)	100	-	100	-	100	-	100	-	ns
t_{SPIA}	10, 11	Access time (Slave)	0	120	0	120	0	120	0	120	ns
t_{SPIDIS}	10, 11	Disable time (Slave)									ns
		2.0 MHz	0	240	-	240	0	240	-	240	
		3.0 MHz	0	167	-	167	0	167	-	167	
t_{SPIDV}	8, 9, 10, 11	Enable to output data valid									ns
		2.0 MHz	-	240	-	240	-	240	-	240	
		3.0 MHz	-	167	-	167	-	167	-	167	
t_{SPIOH}	8, 9, 10, 11	Output data hold time	0	-	0	-	0	-	0	-	ns

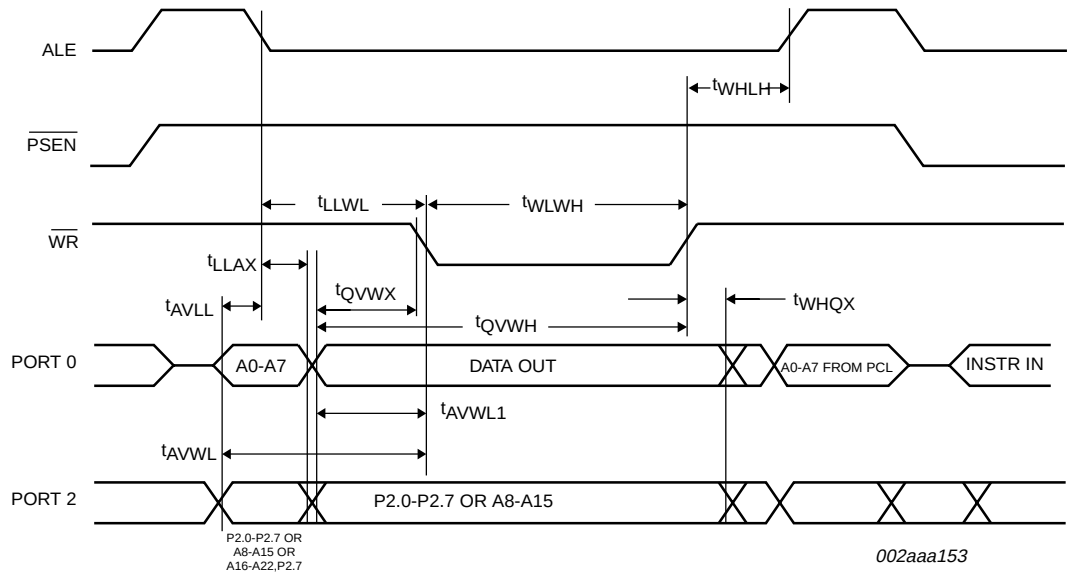


Fig 6. External data memory write cycle.

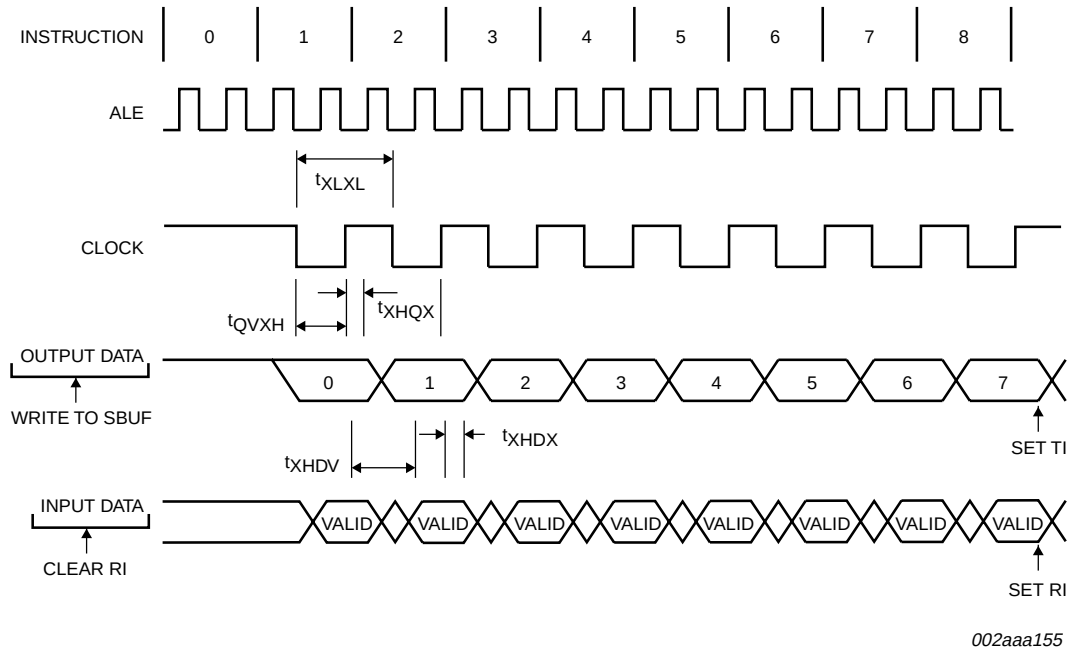


Fig 7. Shift register mode timing.

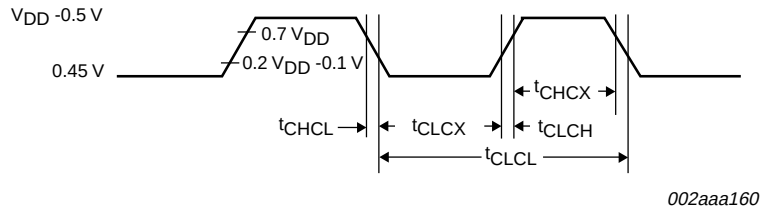


Fig 12. External clock drive.

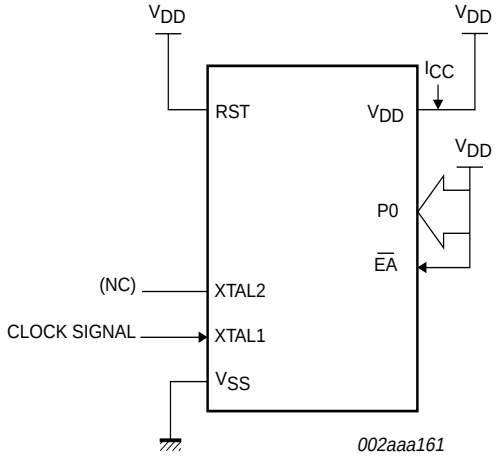


Fig 13. I_{CC} test condition, active mode (all other pins are disconnected).

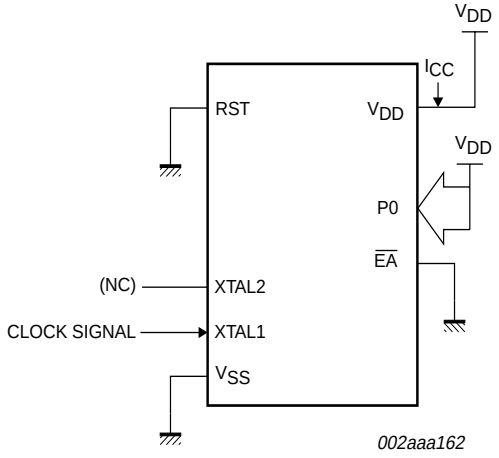
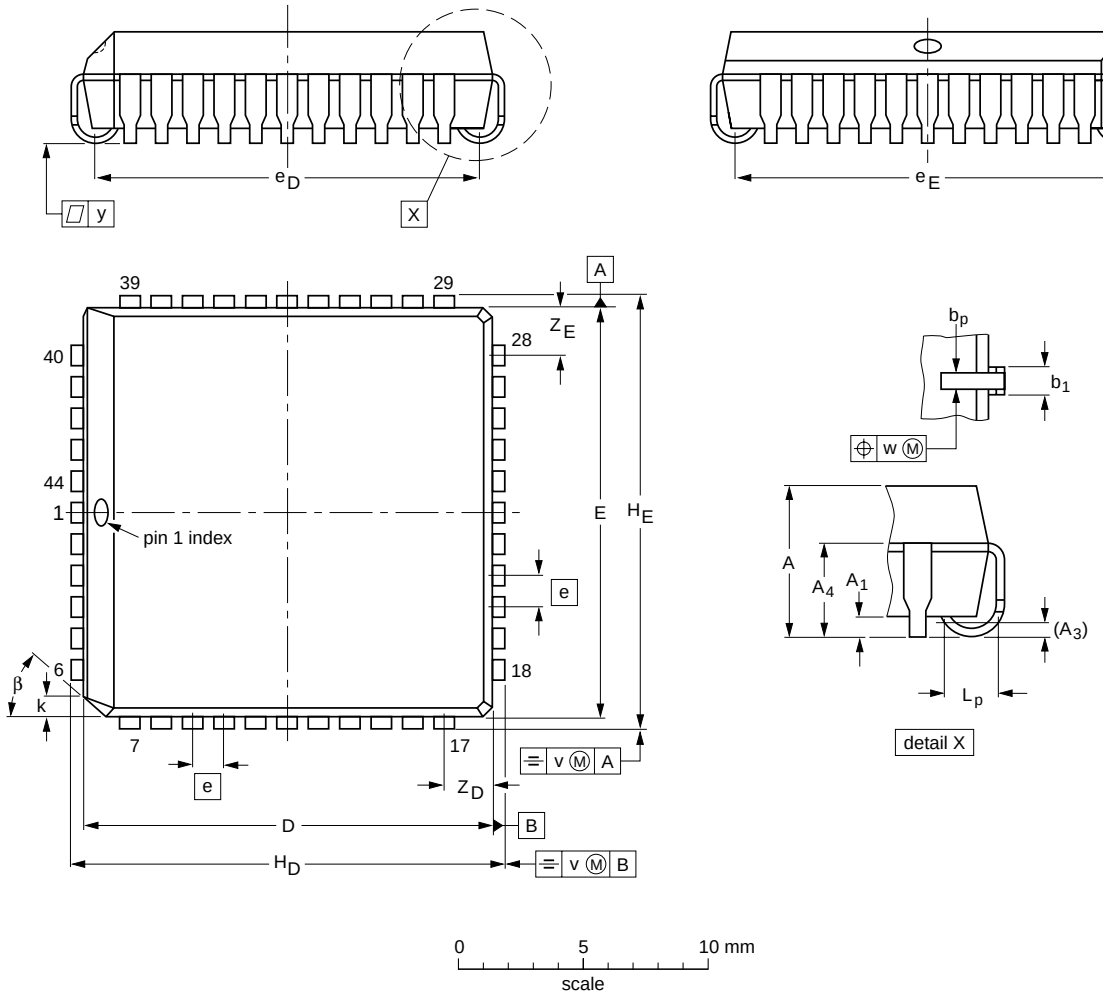


Fig 14. I_{CC} test condition, idle mode (all other pins are disconnected).

12. Package outline

PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 17. SOT187-2.

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Revision history

Table 10: Revision history

Rev	Date	CPCN	Description
03	20031113	-	**Product data (9397 750 12302); ECN 853-2426 01-A14402 dated 6 November 2003** Modifications: • Figure 5 “External data memory read cycle.” on page 24; added t_{RLDV}, removed ‘non-extended memory cycle’ from figure title. • Figure 6 “External data memory write cycle.” on page 25; removed ‘non-extended memory cycle’ from figure title.
02	20030519	-	**Product data (9397 750 11517)**
_1	20010406	-	**Preliminary specification (9397 750 08199)**

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