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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
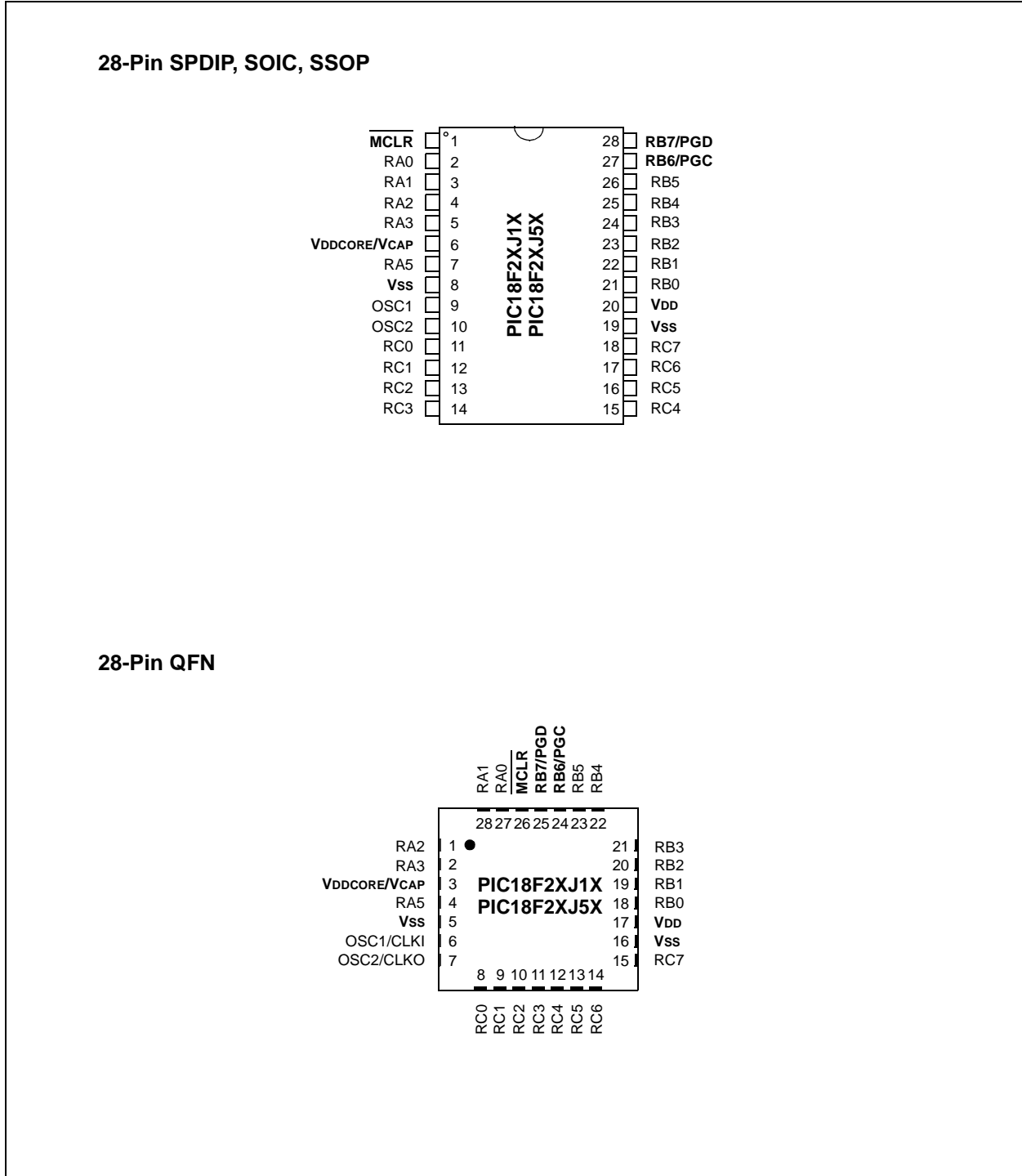
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2.15V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f25j50-i-sp

FIGURE 2-1:   **PIC18F2XJXX/4XJXX FAMILY PIN DIAGRAMS**

28-Pin SPDIP, SOIC, SSOP

$\overline{\text{MCLR}}$	1	28 RB7/PGD
RA0	2	27 RB6/PGC
RA1	3	26 RB5
RA2	4	25 RB4
RA3	5	24 RB3
VDDCORE/VCAP	6	23 RB2
RA5	7	22 RB1
Vss	8	21 RB0
OSC1	9	20 VDD
OSC2	10	19 Vss
RC0	11	18 RC7
RC1	12	17 RC6
RC2	13	16 RC5
RC3	14	15 RC4

PIC18F2XJ1X
PIC18F2XJ5X

28-Pin QFN

Top pins: RA1 (28), RA0 (27), $\overline{\text{MCLR}}$ (26), RB7/PGD (25), RB6/PGC (24), RB5 (23), RB4 (22)

RA2	1	21 RB3
RA3	2	20 RB2
VDDCORE/VCAP	3	19 RB1
RA5	4	18 RB0
Vss	5	17 VDD
OSC1/CLKI	6	16 Vss
OSC2/CLKO	7	15 RC7

PIC18F2XJ1X
PIC18F2XJ5X

Bottom pins: RC0 (8), RC1 (9), RC2 (10), RC3 (11), RC4 (12), RC5 (13), RC6 (14)

PIC18F2XJXX/4XJXX FAMILY

### 2.1.1 PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX DEVICES AND THE ON-CHIP VOLTAGE REGULATOR

PIC18**F**XXJXX devices have an internal core voltage regulator. On these devices ("PIC18**F**" in the part number), the regulator is always enabled. The regulator input is taken from the V_{DD} pins of the microcontroller. The output of the regulator is supplied to the V_{DDCORE}/V_{CAP} pin. On these devices, this pin simultaneously serves as both regulator output and microcontroller core power input pin. For these devices, the V_{DDCORE}/V_{CAP} pin should be tied only to a capacitor.

PIC18**LF**XXJXX devices do not have an internal core voltage regulator. On the low-voltage devices (LF), power must be externally supplied to both V_{DD} and V_{DDCORE}/V_{CAP}.

Whether or not the regulator is used, it is always good design practice to have sufficient capacitance on all supply pins. Examples are shown in Figure 2-3.

The specifications for core voltage and capacitance are listed in **Section 6.0 "AC/DC Characteristics Timing Requirements for Program/Verify Test Mode"**.

FIGURE 2-3: CONNECTIONS FOR THE ON-CHIP REGULATOR
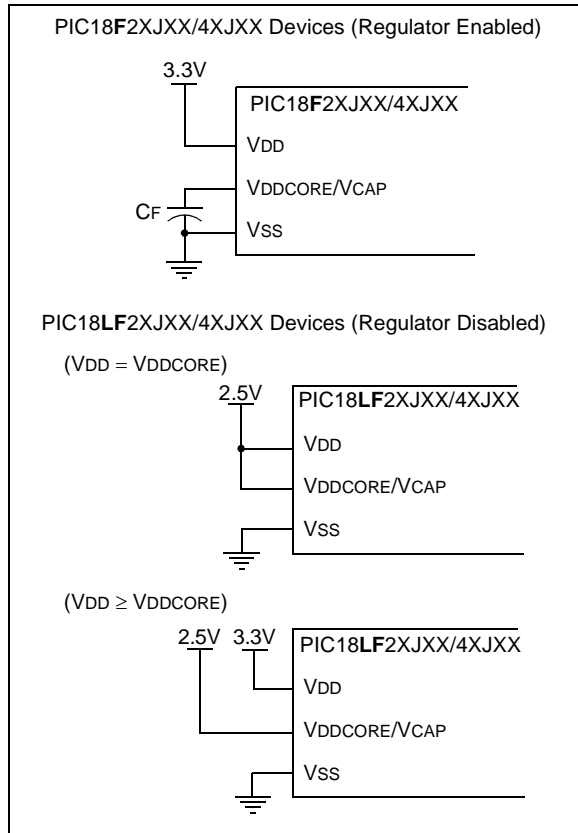
2.2 Memory Maps

The PIC18F2XJXX/4XJXX Family of devices offers program memory sizes of 16, 32, 64, and 128 Kbytes. The memory sizes for different members of the family are shown in Table 2-2. The overall memory maps for all the devices are shown in Figure 2-4.

TABLE 2-2: PROGRAM MEMORY SIZES FOR PIC18F2XJXX/4XJXX FAMILY DEVICES

Device*	Program Memory (Kbytes)	Location of Flash Configuration Words
PIC18F24J10	16	3FF8h:3FFFh
PIC18F44J10		
PIC18F24J11		
PIC18F44J11		
PIC18F24J50		
PIC18F44J50		
PIC18F25J10	32	7FF8h:7FFFh
PIC18F45J10		
PIC18F25J11		
PIC18F45J11		
PIC18F25J50		
PIC18F45J50		
PIC18F26J11	64	FFF8h:FFFFh
PIC18F46J11		
PIC18F26J13		
PIC18F46J13		
PIC18F26J50		
PIC18F46J50		
PIC18F26J53		
PIC18F46J53		
PIC18F27J13	128	1FFF8h:1FFFFh
PIC18F47J13		
PIC18F27J53		
PIC18F47J53		

* Includes PIC18F and PIC18LF devices.

For purposes of code protection, the program memory for every device is treated as a single block. Therefore, enabling code protection, thus protecting the entire code memory and not individual segments.

The Configuration Words for these devices are located at addresses 300000h through 300007h. These are implemented as three pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the last four words (or eight bytes) of the code space (also called the Flash Configuration Words) should be written with Configuration data and not executable code. The addresses of the Flash Configuration Words are listed in Table 2-2. Refer to section **Section 5.0 "Configuration Word"** for more information.

Locations 3FFFFEh and 3FFFFFh are reserved for the Device ID bits. These bits, which may be used by the programmer to identify what device type is being programmed, are described in **Section 5.1 "Device ID Word"**. These Device ID bits read out normally, even after code protection.

2.2.1   MEMORY ADDRESS POINTER

Memory in the device address space (000000h to 3FFFFFh) is addressed via the Table Pointer register, which in turn is comprised of three registers:
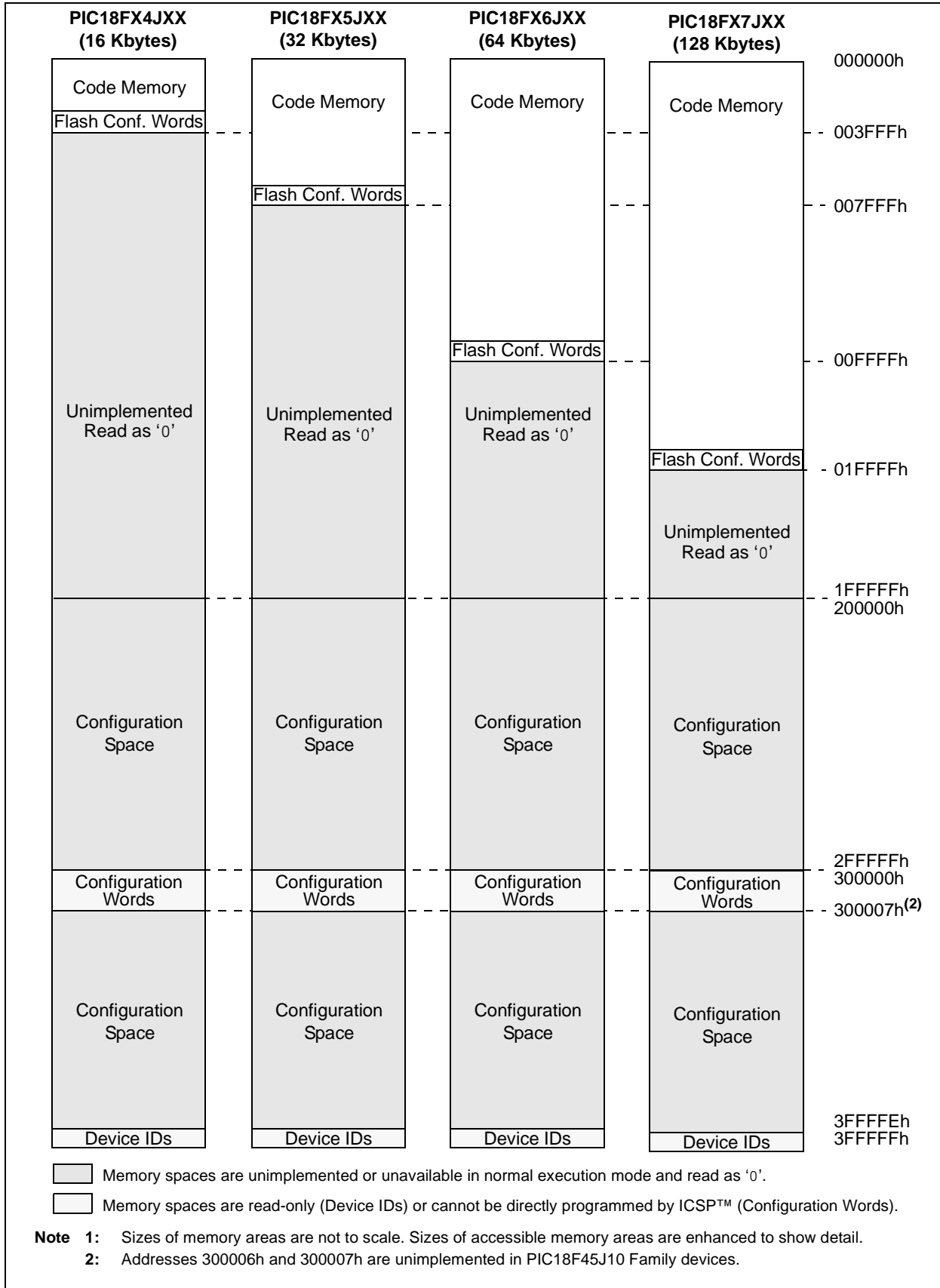
- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

PIC18F2XJXX/4XJXX FAMILY

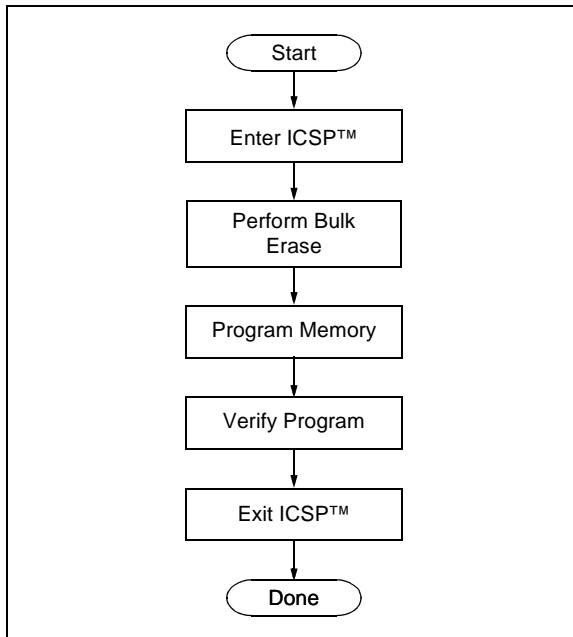**FIGURE 2-4:** MEMORY MAPS FOR PIC18F2XJXX/4XJXX FAMILY DEVICES[1]

Memory spaces are unimplemented or unavailable in normal execution mode and read as '0'.

Memory spaces are read-only (Device IDs) or cannot be directly programmed by ICSP™ (Configuration Words).

Note 1: Sizes of memory areas are not to scale. Sizes of accessible memory areas are enhanced to show detail.

2: Addresses 300006h and 300007h are unimplemented in PIC18F45J10 Family devices.

2.3 Overview of the Programming Process

Figure 2-5 shows the high-level overview of the programming process in which a Bulk Erase is performed first, then the code memory is programmed. Since only nonvolatile Configuration Words are within the code memory space, the Configuration Words are also programmed as code. Code memory (including the Configuration Words) is then verified to ensure that programming was successful.

FIGURE 2-5: HIGH-LEVEL PROGRAMMING FLOW

2.4 Entering and Exiting ICSP™ Program/Verify Mode

Entry into ICSP modes for PIC18F2XJXX/4XJXX Family devices is somewhat different than previous PIC18 devices. As shown in Figure 2-6, entering ICSP Program/Verify mode requires three steps:

1. Voltage is briefly applied to the $\overline{\text{MCLR}}$ pin.
2. A 32-bit key sequence is presented on PGD.
3. Voltage is reapplied to $\overline{\text{MCLR}}$ and held.

The programming voltage applied to $\overline{\text{MCLR}}$ is V_{IH}, or essentially, V_{DD}. There is no minimum time requirement for holding at V_{IH}. After V_{IH} is removed, an interval of at least P19 must elapse before presenting the key sequence on PGD.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000', which is more easily remembered as 4D434850h in hexadecimal. The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the Most Significant nibble must be shifted in first.

Once the key sequence is complete, V_{IH} must be applied to $\overline{\text{MCLR}}$ and held at that level for as long as Program/Verify mode is to be maintained. An interval of at least time, P20 and P12, must elapse before presenting data on PGD. Signals appearing on PGD before P12 has elapsed may not be interpreted as valid.

On successful entry, the program memory can be accessed and programmed in serial fashion. While in the Program/Verify mode, all unused I/Os are placed in the high-impedance state.

Exiting Program/Verify mode is done by removing V_{IH} from $\overline{\text{MCLR}}$, as shown in Figure 2-7. The only requirement for exit is that an interval, P16, should elapse between the last clock and program signals on PGC and PGD before removing V_{IH}.
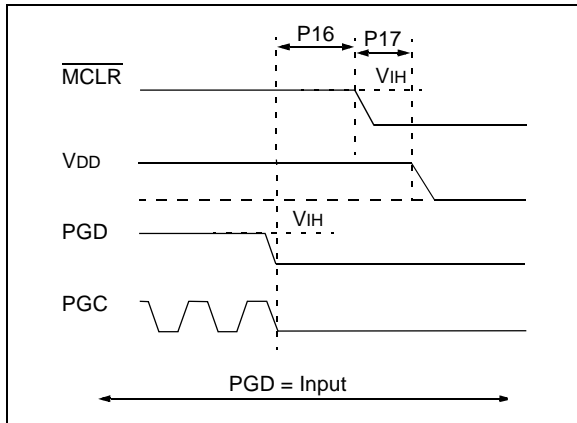
When V_{IH} is reapplied to $\overline{\text{MCLR}}$, the device will enter the ordinary operational mode and begin executing the application instructions.

FIGURE 2-6: ENTERING PROGRAM/VERIFY MODE
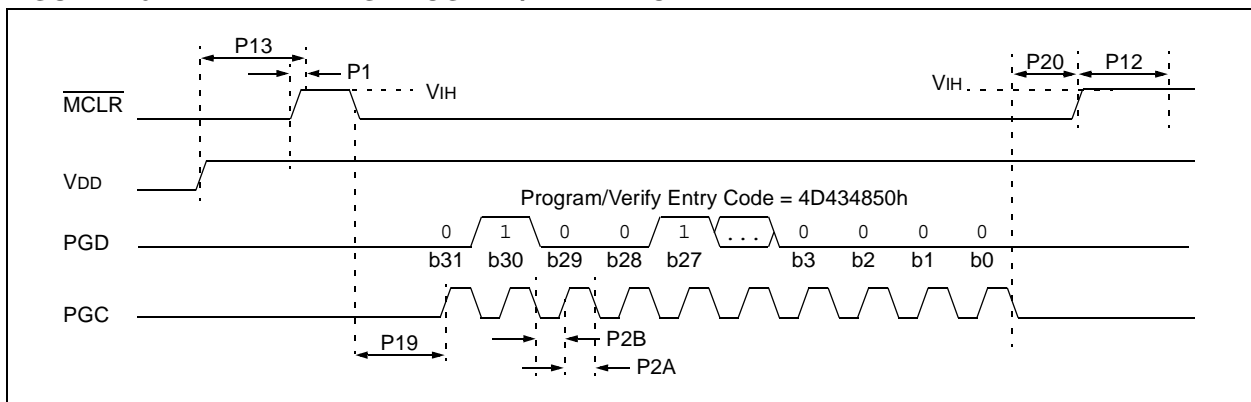
**FIGURE 2-7: EXITING PROGRAM/
VERIFY MODE**

PGD = Input

2.5 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC, and are Least Significant bit (LSb) first.

2.5.1 FOUR-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or eight bits of input data and eight bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown Most Significant bit (MSb) first. The command operand or "Data Payload" is shown <MSB><LSB>. Figure 2-8 demonstrates how to serially present a 20-bit command/operand to the device.

2.5.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

**TABLE 2-3: COMMANDS FOR
PROGRAMMING**

Description	4-Bit Command
Core Instruction (Shift in 16-bit instruction)	0000
Shift out TABLAT register	0010
Table Read	1000
Table Read, Post-Increment	1001
Table Read, Post-Decrement	1010
Table Read, Pre-Increment	1011
Table Write	1100
Table Write, Post-Increment by 2	1101
Table Write, Start Programming, Post-Increment by 2	1110
Table Write, Start Programming	1111

**TABLE 2-4: SAMPLE COMMAND
SEQUENCE**

4-Bit Command	Data Payload	Core Instruction
1101	3C 40	Table Write, post-increment by 2

FIGURE 2-8: TABLE WRITE, POST-INCREMENT TIMING (1101)

PGD = Input
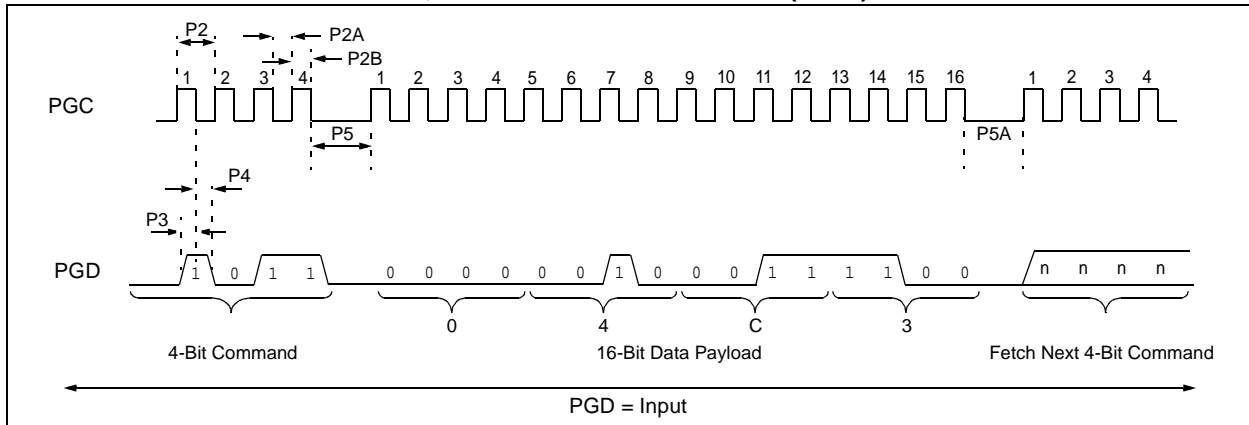
3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the memory within the device.

The EECON1 register is used to control Write or Row Erase operations. The WREN bit must be set to enable writes; this must be done prior to initiating a write sequence. It is strongly recommended that the WREN bit only be set immediately prior to a program or erase operation.

The FREE bit must be set in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit.

3.1 ICSP™ Erase

3.1.1 ICSP BULK ERASE

The PIC18F2XJXX/4XJXX Family devices may be Bulk Erased by writing 0180h to the table address, 3C0005h:3C0004h. The basic sequence is shown in Table 3-1 and demonstrated in Figure 3-1.

Since the code-protect Configuration bit is stored in the program code within code memory, a Bulk Erase operation will also clear any code-protect settings for the device.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the NOP command), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

TABLE 3-1: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	01 01	Write 01h to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	80 80	Write 80h TO 3C0004h to erase entire device.
0000	00 00	NOP
0000	00 00	Hold PGD low until erase completes.

FIGURE 3-1: BULK ERASE FLOW
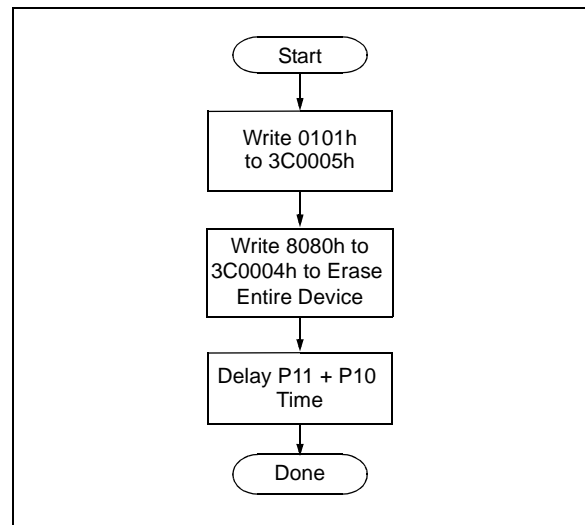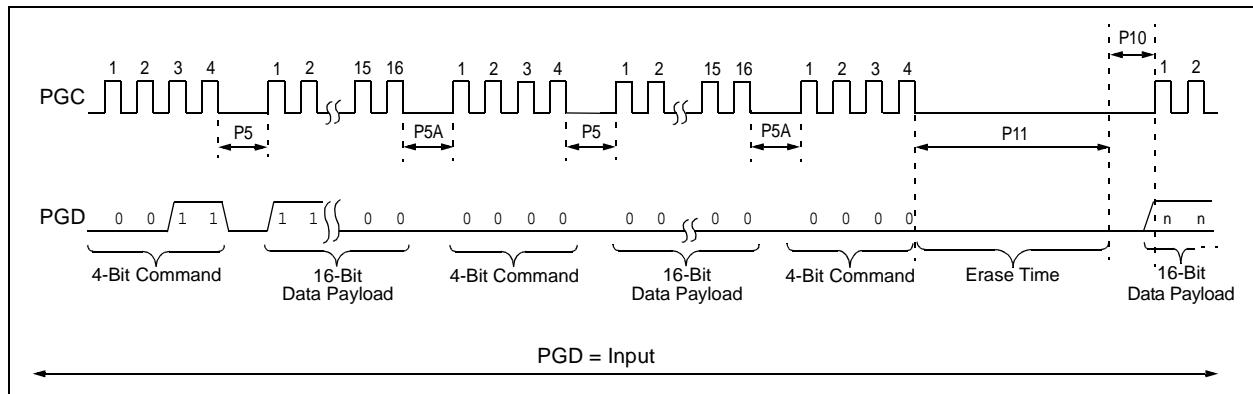

FIGURE 3-2: BULK ERASE TIMING

3.1.2 ICSP™ ROW ERASE

It is possible to erase one row (1024 bytes of data), provided the block is not code-protected or erase/write-protected. Rows are located at static boundaries beginning at program memory address 000000h, extending to the internal program memory limit. Refer to **Section 2.2 "Memory Maps"**).

The Row Erase duration is internally timed. After the WR bit in EECON1 is set, a NOP instruction is issued, where the 4th PGC is held high for the duration of the Row Erase time, P10.

The code sequence to Row Erase a PIC18F2XJXX/4XJXX Family device is shown in Table 3-2. The flowchart shown in Figure 3-4 depicts the logic necessary to completely erase a PIC18F2XJXX/4XJXX Family device. The timing diagram that details the Row Erase command and parameter P10 is shown in Figure 3-3.

Note 1:	If the last row of program memory is erased, bit 3 of CONFIG1H must also be programmed as '0'.
2:	The TBLPTR register can point at any byte within the row intended for erase.
3:	If code protection has been enabled, ICSP Bulk Erase (all program memory erased) operations can be used to disable code protection. ICSP Row Erase operations cannot be used to disable code protection.

TABLE 3-2: ERASE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable memory writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000	6A F8	CLRF TBLPTRU
0000	6A F7	CLRF TBLPTRH
0000	6A F6	CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000	88 A6	BSF EECON1, FREE
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP – hold PGC high for time P10.
Step 4: Repeat Step 3, with Address Pointer incremented by 1024, until all rows are erased.		

FIGURE 3-3: SET WR AND START ROW ERASE TIMING
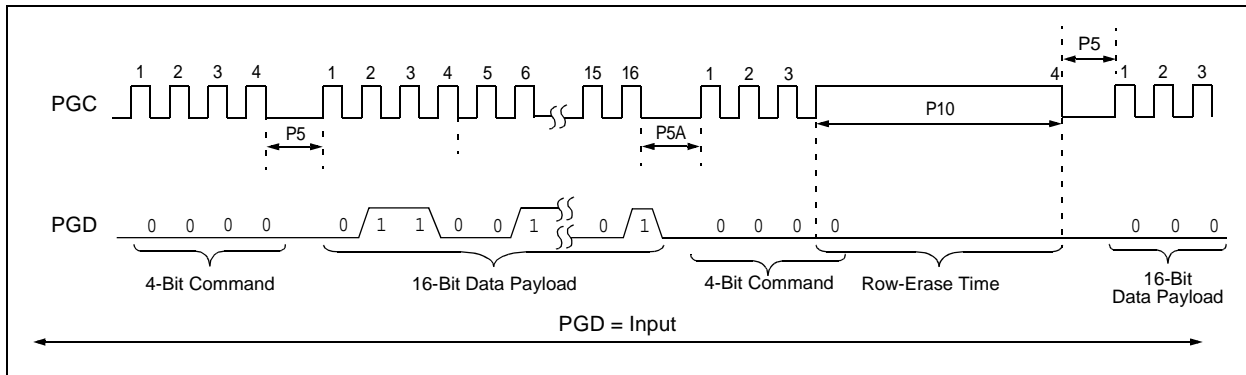
3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write buffer for all devices in the PIC18F2XJXX/4XJXX Family is 64 bytes. It can be mapped to any 64-byte block beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the 64-byte block of code memory indicated by the Table Pointer.

Write buffer locations are not cleared following a write operation; the buffer retains its data after the write is complete. This means that the buffer must be written with 64 bytes on each operation. If there are locations in the code memory that are to remain empty, the corresponding locations in the buffer must be filled with FFFFh. This avoids rewriting old data from the previous cycle.

The programming duration is internally timed. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

The code sequence to program a PIC18F2XJXX/4XJXX Family device is shown in Table 3-3. The flowchart shown in Figure 3-5 depicts the logic necessary to completely write a PIC18F2XJXX/4XJXX Family device. The timing diagram that details the Start Programming command and parameter P9 is shown in Figure 3-6.

> **Note 1:** The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

TABLE 3-3: WRITE CODE MEMORY CODE SEQUENCE

| 4-Bit Command	Data Payload	Core Instruction
Step 1: Enable writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Load write buffer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 3: Repeat for all but the last two bytes. Any unused locations should be filled with FFFFh.		
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
Step 4: Load write buffer for last two bytes.		
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9.
To continue writing data, repeat Steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop.		

4.2 Verify Code Memory and Configuration Word

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Because the Flash Configuration Words are stored at the end of program memory, it is verified with the rest of the code at this time.

The verify process is shown in the flowchart in Figure 4-2. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory"** for implementation details of reading code memory.

Note 1: Because the Flash Configuration Word contains the device code protection bit, code memory should be verified immediately after writing if code protection is enabled. This is because the device will not be readable or verifiable if a device Reset occurs after the Flash Configuration Words (and the CP0 bit) have been cleared.

FIGURE 4-2: **VERIFY CODE MEMORY FLOW**
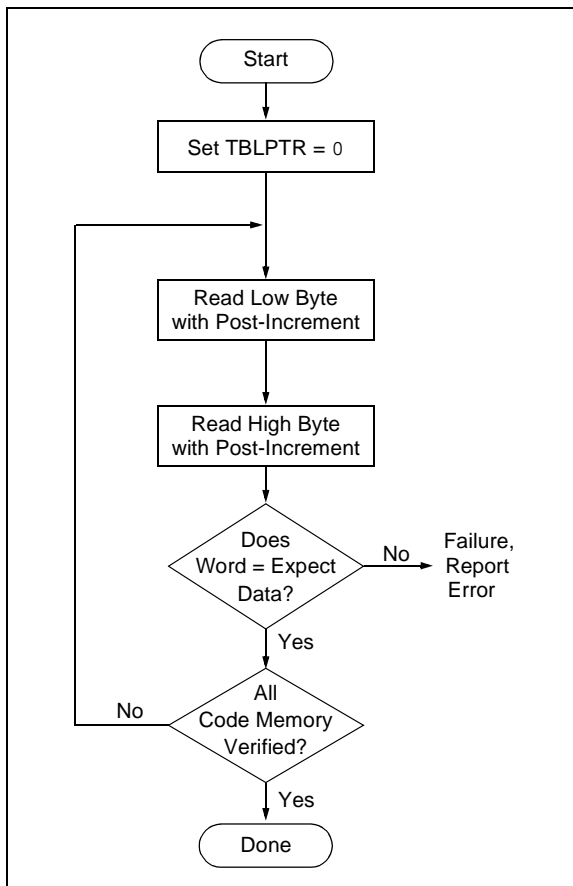
4.3 Blank Check

The term Blank Check means to verify that the device has no programmed memory cells. All memories, code memory and Configuration bits, must be verified. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as a '1', so Blank Checking a device merely means to verify that all bytes read as FFh. The overall process flow is shown in Figure 4-3.

Blank Checking is merely code verification with FFh expect data. For implementation details, refer to **Section 4.2 "Verify Code Memory and Configuration Word"**.

FIGURE 4-3: **BLANK CHECK FLOW**
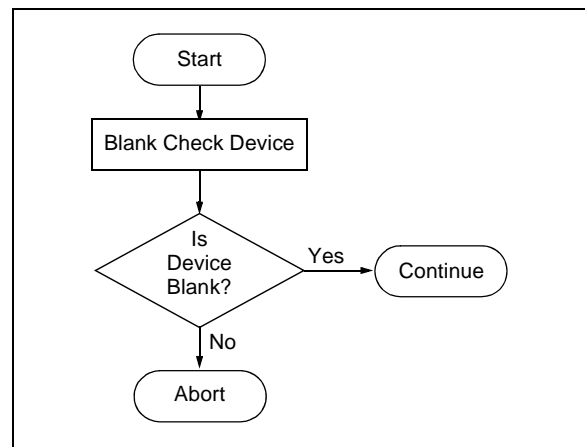
5.0 CONFIGURATION WORD

The Configuration Words of the PIC18F2XJXX/4XJXX Family devices are implemented as volatile memory registers. All of the Configuration registers (CONFIG1L, CONFIG1H, CONFIG2L, CONFIG2H, CONFIG3L, CONFIG3H, CONFIG4L, and CONFIG4H) are automatically loaded following each device Reset.

The data for these registers is taken from the four Flash Configuration Words located at the end of program memory. Configuration data is stored in order, starting with CONFIG1L in the lowest Flash address and ending with CONFIG4H in the highest. The mapping to specific Configuration Words is shown in Table 5-1. Users should always reserve these locations for Configuration Word data and write their application code accordingly.

The upper four bits of each Flash Configuration Word should always be stored in program memory as '1111'. This is done so these program memory addresses will always be '1111 xxxx xxxx xxxx' and interpreted as a NOP instruction if they were ever to be executed. Because the corresponding bits in the Configuration registers are unimplemented, they will not change the device's configuration.

The Configuration and Device ID registers are summarized in Table 5-2. A listing of the individual Configuration bits and their options is provided in Table 5-3.

TABLE 5-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS

Configuration Register	Flash Configuration Byte[1]	Configuration Register Address
CONFIG1L	XFF8h	300000h
CONFIG1H	XFF9h	300001h
CONFIG2L	XFFAh	300002h
CONFIG2H	XFFBh	300003h
CONFIG3L	XFFCh	300004h
CONFIG3H	XFFDh	300005h
CONFIG4L[2]	XFFEh	300006h
CONFIG4H[2]	XFFFh	300007h

Note 1: See Table 2-2 for the complete addresses within code space for specific devices and memory sizes.

2: Unimplemented in PIC18F45J10 family devices.

TABLE 5-2: PIC18F45J10 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDs

	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	DEBUG	XINST	STVREN	—	—	—	—	WDTEN	111- ---1
300001h	CONFIG1H	—[1]	—[1]	—[1]	—[1]	—[2]	CP0	—	—	---- 01--
300002h	CONFIG2L	IESO	FCMEN	—	—	—	FOSC2	FOSC1	FOSC0	11-- -111
300003h	CONFIG2H	—[1]	—[1]	—[1]	—[1]	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300005h	CONFIG3H	—[1]	—[1]	—[1]	—[1]	—	—	—	CCP2MX	---- ---1
3FFFFEh	DEVID1[3]	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	See Table
3FFFFFh	DEVID2[3]	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	See Table

Legend: – = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

2: This bit should always be maintained at '0'.

3: DEVID registers are read-only and cannot be programmed by the user.

TABLE 5-3: PIC18F45J10 FAMILY DEVICES: BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
DEBUG	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)
CP0	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
IESO	CONFIG2L	Internal/External Oscillator Switchover bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
FOSC2	CONFIG2L	Default Oscillator Select bit 1 = Clock designated by FOSC<1:0> is enabled as system clock when OSCCON<1:0> = 00 0 = INTRC is enabled as system clock when OSCCON<1:0> = 00
FOSC<1:0>	CONFIG2L	Primary Oscillator Select bits 11 = EC oscillator, PLL enabled and under software control, CLKO function on OSC2 10 = EC oscillator, CLKO function on OSC2 01 = HS oscillator, PLL enabled and under software control 00 = HS oscillator
WDTPS<3:0>	CONFIG2H	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
CCP2MX	CONFIG3H	CCP2 MUX bit 1 = CCP2 is multiplexed with RC1 0 = CCP2 is multiplexed with RB3

TABLE 5-5:   PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
CP0[4]	CONFIG1H	Code Protection bit `1 =` Program memory is not code-protected `0 =` Program memory is code-protected
CPDIV<1:0>[3]	CONFIG1H	CPU System Clock Selection bits `11 =` No CPU system clock divide `10 =` CPU system clock divided by 2 `01 =` CPU system clock divided by 3 `00 =` CPU system clock divided by 6
IESO	CONFIG2L[1,2]	Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit `1 =` Oscillator Switchover mode enabled `0 =` Oscillator Switchover mode disabled
FCMEN	CONFIG2L[1,2]	Fail-Safe Clock Monitor Enable bit `1 =` Fail-Safe Clock Monitor enabled `0 =` Fail-Safe Clock Monitor disabled
LPT1OSC	CONFIG2L[1,2]	Low-Power Timer1 Oscillator Enable bit `1 =` Timer1 oscillator configured for low-power operation `0 =` Timer1 oscillator configured for higher-power operation
T1DIG	CONFIG2L[1,2]	Secondary Clock Source T1OSCEN Enforcement bit[1] `1 =` Secondary oscillator clock source may be selected (OSCCON <1:0> = 01) regardless of T1OSCEN state `0 =` Secondary oscillator clock source may not be selected unless T1CON <3> = 1
FOSC<2:0>	CONFIG2L[1,2]	Oscillator Selection bits `111 =` EC+PLL (S/W controlled by PLLEN bit), CLKO on RA6 `110 =` EC oscillator (PLL always disabled) with CLKO on RA6 `101 =` HS+PLL (S/W controlled by PLLEN bit) `100 =` HS oscillator (PLL always disabled) `011 =` INTOSCPLLO, internal oscillator with PLL (S/W controlled by PLLEN bit), CLKO on RA6, port function on RA7 `010 =` INTOSCPLL, internal oscillator with PLL (S/W controlled by PLLEN bit), port function on RA6 and RA7 `001 =` INTOSCO, internal oscillator, INTOSC or INTRC (PLL always disabled), CLKO on RA6, port function on RA7 `000 =` INTOSC, internal oscillator INTOSC or INTRC (PLL always disabled), port function on RA6 and RA7
WDTPS<3:0>	CONFIG2H[1,2]	Watchdog Timer Postscale Select bits `1111 =` 1:32,768 `1110 =` 1:16,384 `1101 =` 1:8,192 `1100 =` 1:4,096 `1011 =` 1:2,048 `1010 =` 1:1,024 `1001 =` 1:512 `1000 =` 1:256 `0111 =` 1:128 `0110 =` 1:64 `0101 =` 1:32 `0100 =` 1:16 `0011 =` 1:8 `0010 =` 1:4 `0001 =` 1:2 `0000 =` 1:1

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on V_DD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F46J11 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

TABLE 5-5:   PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
DSWTPS<3:0>	CONFIG3L	Deep Sleep Watchdog Timer Postscale Select bits The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms. `1111` = 1:2,147,483,648 (25.7 days) `1110` = 1:536,870,912 (6.4 days) `1101` = 1:134,217,728 (38.5 hours) `1100` = 1:33,554,432 (9.6 hours) `1011` = 1:8,388,608 (2.4 hours) `1010` = 1:2,097,152 (36 minutes) `1001` = 1:524,288 (9 minutes) `1000` = 1:131,072 (135 seconds) `0111` = 1:32,768 (34 seconds) `0110` = 1:8,192 (8.5 seconds) `0101` = 1:2,048 (2.1 seconds) `0100` = 1:512 (528 ms) `0011` = 1:128 (132 ms) `0010` = 1:32 (33 ms) `0001` = 1:8 (8.3 ms) `0000` = 1:2 (2.1 ms)
DSWDTEN	CONFIG3L	Deep Sleep Watchdog Timer Enable bit `1` = DSWDT enabled `0` = DSWDT disabled
DSBOREN	CONFIG3L	Deep Sleep BOR Enable bit `1` = BOR enabled in Deep Sleep `0` = BOR disabled in Deep Sleep (does not affect operation in non Deep Sleep modes)
RTCOSC	CONFIG3L	RTCC Reference Clock Select bit `1` = RTCC uses T1OSC/T1CKI as reference clock `0` = RTCC uses INTRC as reference clock
DSWDTOSC	CONFIG3L	DSWDT Reference Clock Select bit `1` = DSWDT uses INTRC as reference clock `0` = DSWDT uses T1OSC/T1CKI as reference clock
MSSPMSK[1,2]	CONFIG3H	MSSP 7-Bit Address Masking Mode Enable bit `1` = 7-Bit Address Masking mode enable `0` = 5-Bit Address Masking mode enable
IOL1WAY	CONFIG3H	IOLOCK Bit One-Way Set Enable bit `1` = The IOLOCK bit (PPSCON<0>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time. `0` = The IOLOCK bit (PPSCON<0>) can be set and cleared as needed, provided the unlock sequence has been completed.
WPCFG[4]	CONFIG4L	Write/Erase Protect Configuration Words Page bit (valid when WPDIS = `0`) `1` = Configuration Words page is not erase/write-protected unless WPEND and WPFP<5:0> settings include the Configuration Words page `0` = Configuration Words page is erase/write-protected, regardless of WPEND and WPFP<5:0> settings
WPEND	CONFIG4L	Write/Erase Protect Region Select bit (valid when WPDIS = `0`) `1` = Flash pages, WPFP<5:0> to Configuration Words page, are write/erase-protected `0` = Flash pages, 0 to WPFP<5:0> are write/erase-protected

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
   2: The Configuration bits are reset to '1' only on V_DD Reset; it is reloaded with the programmed value at any device Reset.
   3: These bits are not implemented in PIC18F46J11 family devices.
   4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

TABLE 5-5: **PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)**

Bit Name	Configuration Words	Description
WPFP<5:0>	CONFIG4L	Write/Erase Protect Page Start/End Location bits Used with WPEND bit to define which pages in Flash will be write/erase-protected.
WPDIS	CONFIG4H	Write Protect Disable bit 1 = WPFP<5:0>, WPEND and WPCFG bits ignored; all Flash memory may be erased or written 0 = WPFP<5:0>, WPEND and WPCFG bits enabled; write/erase-protect active for the selected region(s)
DEV<2:0>	DEVID1	Device ID bits Used with the DEV<10:3> bits in the Device ID Register 2 to identify the part number.
REV<4:0>	DEVID1	Revision ID bits Indicate the device revision.
DEV<10:3>	DEVID2	Device ID bits Used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

    2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

    3: These bits are not implemented in PIC18F46J11 family devices.

    4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

TABLE 5-6: **PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDs**

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value[1]
300000h	CONFIG1L	$\overline{\text{DEBUG}}$	XINST	STVREN	CFGPLLEN	PLLDIV2	PLLDIV1	PLLDIV0	WDTEN	111- 1111
300001h	CONFIG1H	—[2]	—[2]	—[2]	—[2]	—[4]	CP0	CPDIV1[3]	CPDIV0[3]	---- 0111
300002h	CONFIG2L	IESO	FCMEN	CLKOEC	SOSCSEL1	SOSCSEL0	FOSC2	FOSC1	FOSC0	1111 1111
300003h	CONFIG2H	—[2]	—[2]	—[2]	—[2]	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300004h	CONFIG3L	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0	DSWDTEN	DSBOREN	RTCOSC	DSWDTOSC	1111 1111
300005h	CONFIG3H	—[2]	—[2]	—[2]	—[2]	MSSPMSK	PLLSEL	ADCSEL	IOL1WAY	---- 1111
300006h	CONFIG4L	WPCFG	WPFP6	WPFP5	WPFP4	WPFP3	WPFP2	WPFP1	WPFP0	1111 1111
300007h	CONFIG4H	—[2]	—[2]	—[2]	—[2]	LS48MHZ[3]	—	WPEND	WPDIS	---- 1-11
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0101 10xx

Legend: x = unknown, u = unchanged, – = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

    2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

    3: These bits are not implemented in PIC18F47J13 family devices.

    4: This bit should always be maintained at '0'.

TABLE 5-7: **PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS**

Bit Name	Configuration Words	Description
DEBUG	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Enhanced Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
CFGPLLEN	CONFIG1L	Enable PLL on Start-up bit 1 = PLL enabled on start-up. Not recommended for low-voltage designs. 0 = PLL disabled on start-up. Firmware may later enable PLL through OSCTUNE<6>.
PLLDIV<2:0>	CONFIG1L	96 MHz PLL Input Divider bits Divider must be selected to provide a 4 MHz input into the 96 MHz PLL. 111 =No divide – oscillator used directly (4 MHz input) 110 =Oscillator divided by 2 (8 MHz input) 101 =Oscillator divided by 3 (12 MHz input) 100 =Oscillator divided by 4 (16 MHz input) 011 =Oscillator divided by 5 (20 MHz input) 010 =Oscillator divided by 6 (24 MHz input) 001 =Oscillator divided by 10 (40 MHz input) 000 =Oscillator divided by 12 (48 MHz input)
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on the SWDTEN bit)
CP0[4]	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
CPDIV<1:0>[3]	CONFIG1H	CPU System Clock Selection bits 11 = No CPU system clock divide 10 = CPU system clock divided by 2 01 = CPU system clock divided by 3 00 = CPU system clock divided by 6
IESO	CONFIG2L[1,2]	Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L[1,2]	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
CLKOEC	CONFIG2L	EC Mode Clock Output Enable bit 1 = CLKO output signal active on the RA6 pin (EC mode only) 0 = CLKO output disabled
SOSCSEL<1:0>	CONFIG2L	Secondary Oscillator Circuit Selection bits 11 = High-power SOSC circuit selected 10 = Digital Input mode (SCLKI) 01 = Low-power SOSC circuit selected 00 = Reserved

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
   2: The Configuration bits are reset to '1' only on V_{DD} Reset; it is reloaded with the programmed value at any device Reset.
   3: These bits are not implemented in PIC18F47J13 family devices.
   4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
   5: Not implemented on PIC18F47J53 family devices.

TABLE 5-7: **PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)**

Bit Name	Configuration Words	Description
FOSC<2:0>	CONFIG2L[1,2]	Oscillator Selection bits 111 =EC+PLL (S/W controlled by PLLEN bit), CLKO on RA6 110 =EC oscillator (PLL always disabled) with CLKO on RA6 101 =HS+PLL (S/W controlled by PLLEN bit) 100 =HS oscillator (PLL always disabled) 011 =INTOSCPLLO, internal oscillator with PLL (S/W controlled by PLLEN bit), CLKO on RA6, port function on RA7 010 =INTOSCPLL, internal oscillator with PLL (S/W controlled by PLLEN bit), port function on RA6 and RA7 001 =INTOSCO, internal oscillator, INTOSC or INTRC (PLL always disabled), CLKO on RA6, port function on RA7 000 =INTOSC, internal oscillator INTOSC or INTRC (PLL always disabled), port function on RA6 and RA7
WDTPS<3:0>	CONFIG2H[1,2]	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
DSWTPS<3:0>	CONFIG3L	Deep Sleep Watchdog Timer Postscale Select bits The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms. 1111 = 1:2,147,483,648 (25.7 days) 1110 = 1:536,870,912 (6.4 days) 1101 = 1:134,217,728 (38.5 hours) 1100 = 1:33,554,432 (9.6 hours) 1011 = 1:8,388,608 (2.4 hours) 1010 = 1:2,097,152 (36 minutes) 1001 = 1:524,288 (9 minutes) 1000 = 1:131,072 (135 seconds) 0111 = 1:32,768 (34 seconds) 0110 = 1:8,192 (8.5 seconds) 0101 = 1:2,048 (2.1 seconds) 0100 = 1:512 (528 ms) 0011 = 1:128 (132 ms) 0010 = 1:32 (33 ms) 0001 = 1:8 (8.3 ms) 0000 = 1:2 (2.1 ms)
DSWDTEN	CONFIG3L	Deep Sleep Watchdog Timer Enable bit 1 = DSWDT enabled 0 = DSWDT disabled
DSBOREN	CONFIG3L	Deep Sleep BOR Enable bit 1 = BOR enabled in Deep Sleep 0 = BOR disabled in Deep Sleep (does not affect operation in non Deep Sleep modes)

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
  2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
  3: These bits are not implemented in PIC18F47J13 family devices.
  4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
  5: Not implemented on PIC18F47J53 family devices.

TABLE 5-7: **PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)**

Bit Name	Configuration Words	Description
RTCOSC	CONFIG3L	RTCC Reference Clock Select bit 1 = RTCC uses T1OSC/T1CKI as reference clock 0 = RTCC uses INTRC as reference clock
DSWDTOSC	CONFIG3L	DSWDT Reference Clock Select bit 1 = DSWDT uses INTRC as reference clock 0 = DSWDT uses T1OSC/T1CKI as reference clock
MSSPMSK[1,2]	CONFIG3H	MSSP 7-Bit Address Masking Mode Enable bit 1 = 7-Bit Address Masking mode enable 0 = 5-Bit Address Masking mode enable
PLLSEL[5]	CONFIG3H	PLL Selection bit 1 = 4x PLL selected 0 = 96 MHz PLL selected
ADCSEL	CONFIG3H	ADC Mode Selection bit 1 = 10-Bit ADC mode selected 0 = 12-Bit ADC mode selected
IOL1WAY	CONFIG3H	IOLOCK Bit One-Way Set Enable bit 1 = The IOLOCK bit (PPSCON<0>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time. 0 = The IOLOCK bit (PPSCON<0>) can be set and cleared as needed, provided the unlock sequence has been completed
WPCFG	CONFIG4L	Write/Erase Protect Configuration Words Page bit (valid when WPDIS = 0) 1 = Configuration Words page is not erase/write-protected unless WPEND and WPFP<6:0> settings include the Configuration Words page 0 = Configuration Words page is erase/write-protected, regardless of WPEND and WPFP<6:0>
WPFP<6:0>	CONFIG4L	Write/Erase Protect Page Start/End Location bits Used with WPEND bit to define which pages in Flash will be write/erase-protected.
WPEND	CONFIG4H	Write/Erase Protect Region Select bit (valid when WPDIS = 0) 1 = Flash pages, WPFP<6:0> to Configuration Words page, are write/erase-protected 0 = Flash pages, 0 to WPFP<6:0> are write/erase-protected
WPDIS	CONFIG4H	Write Protect Disable bit 1 = WPFP<6:0>, WPEND and WPCFG bits ignored; all Flash memory may be erased or written 0 = WPFP<6:0>, WPEND and WPCFG bits enabled; write/erase-protect active for the selected region(s)
LS48MHZ[3]	CONFIG4H	System Clock Selection bit 1 = System clock is expected at 48 MHz, FS/LS USB CLKEN's divide-by is set to 8 0 = System clock is expected at 24 MHz, FS/LS USB CLKEN's divide-by is set to 4
DEV<2:0>	DEVID1	Device ID bits Used with the DEV<10:3> bits in the Device ID Register 2 to identify the part number.
REV<4:0>	DEVID1	Revision ID bits Indicate the device revision.
DEV<10:3>	DEVID2	Device ID bits Used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
   2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
   3: These bits are not implemented in PIC18F47J13 family devices.
   4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
   5: Not implemented on PIC18F47J53 family devices.

PIC18F2XJXX/4XJXX FAMILY

Table 5-9 describes how to calculate the checksum for
each device.

TABLE 5-9: **CHECKSUM COMPUTATION**

Device	Code Protection	Checksum
PIC18F24J10 PIC18F44J10	Off	SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & 04h) + ([003FFA] & C7h) + ([003FFB] & 0Fh) + ([003FFD] & 01h)
	On	0000h
PIC18F24J11 PIC18F44J11	Off	SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & FCh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h)
	On	0000h
PIC18F24J50 PIC18F44J50	Off	SUM[000000:003FF7] + ([003FF8] & EFh) + ([003FF9] & FFh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h)
	On	0000h
PIC18F25J10 PIC18F45J10	Off	SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & 04h) + ([007FFA] & C7h) + ([007FFB] & 0Fh) + ([007FFD] & 01h)
	On	0000h
PIC18F25J11 PIC18F45J11	Off	SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & FCh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h)
	On	0000h
PIC18F25J50 PIC18F45J50	Off	SUM[000000:007FF7] + ([007FF8] & EFh) + ([007FF9] & FFh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h)
	On	0000h
PIC18F26J11 PIC18F46J11	Off	SUM[000000:00FFF7] + ([00FFF8] & E1h) + ([00FFF9] & FCh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h)
	On	0000h
PIC18F26J50 PIC18F46J50	Off	SUM[000000:00FFF7] + ([00FFF8] & EFh) + ([00FFF9] & FFh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h)
	On	0000h
PIC18F26J13 PIC18F46J13	Off	SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FCh) +([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FFh) + ([00FFFE] & BFh) + ([00FFFF] & F3h)
	On	0000h
PIC18F26J53 PIC18F46J53	Off	SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FFh) +([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FBh) + ([00FFFE] & BFh) + ([00FFFF] & FBh)
	On	0000h
PIC18F27J13 PIC18F47J13	Off	SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FCh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FFh) + ([01FFFE] & FFh) + ([01FFFF] & F3h)
	On	0000h
PIC18F27J53 PIC18F47J53	Off	SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FFh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FBh) + ([01FFFE] & FFh) + ([01FFFF] & FBh)
	On	0000h

Legend: [a] = Value at address a; SUM[a:b] = Sum of locations a to b inclusive; + = Addition; & = Bitwise AND. All addresses are hexadecimal.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
P1	T_R	$\overline{MCLR}$ Rise Time to Enter Program/Verify mode	—	1.0	µs	
P2	T_{PGC}	Serial Clock (PGC) Period	100	—	ns	
P2A	T_{PGCL}	Serial Clock (PGC) Low Time	50	—	ns	
P2B	T_{PGCH}	Serial Clock (PGC) High Time	50	—	ns	
P3	T_{SET1}	Input Data Setup Time to Serial Clock ↓	20	—	ns	
P4	T_{HLD1}	Input Data Hold Time from PGC ↓	20	—	ns	
P5	T_{DLY1}	Delay Between 4-Bit Command and Command Operand	50	—	ns	
P5A	T_{DLY1A}	Delay Between 4-Bit Command Operand and Next 4-Bit Command	50	—	ns	
P6	T_{DLY2}	Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	T_{DLY5}	Delay to allow Block Programming to occur	3.4	—	ms	PIC18F2XJ10/PIC18F4XJ10
			1.2	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ5X/PIC18F4XJ5X
P10	T_{DLY6}	Delay to allow Row Erase to occur	49	—	ms	PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53
			54	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50
P11	T_{DLY7}	Delay to allow Bulk Erase to occur	475	—	ms	PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53
			524	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50
P12	T_{HLD2}	Input Data Hold Time from $\overline{MCLR}$ ↑	400	—	µs	
P13	T_{SET2}	V_{DD} ↑ Setup Time to $\overline{MCLR}$ ↑	100	—	ns	
P14	T_{VALID}	Data Out Valid from PGC ↑	25	—	ns	
P16	T_{DLY8}	Delay between Last PGC ↓ and $\overline{MCLR}$ ↓	20	—	ns	
P17	T_{HLD3}	$\overline{MCLR}$ ↓ to V_{DD} ↓	3	—	µs	
P19	T_{KEY1}	Delay from First $\overline{MCLR}$ ↓ to First PGC ↑ for Key Sequence on PGD	4	—	ms	
P20	T_{KEY2}	Delay from Last PGC ↓ for Key Sequence on PGD to Second $\overline{MCLR}$ ↑	50	—	ns	

Note 1: External power must be supplied to the V_{DDCORE}/V_{CAP} pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 "PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX Devices and the On-Chip Voltage Regulator"** for more information.

2: V_{DD} must also be supplied to the AV_{DD} pins during programming. AV_{DD} and AV_{SS} should always be within ±0.3V of V_{DD} and V_{SS}, respectively.