



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

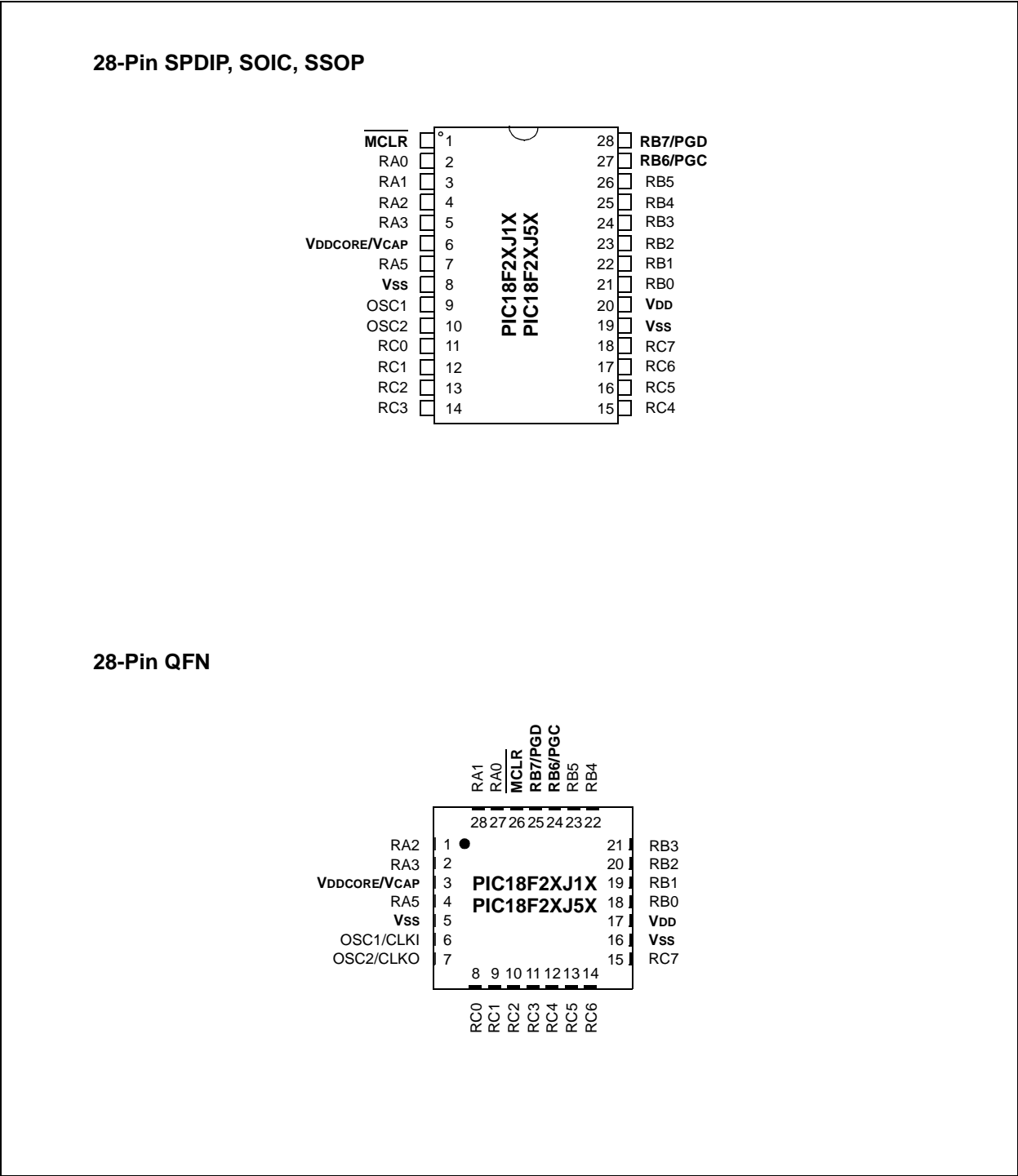
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf46j50t-i-ml

PIC18F2XJXX/4XJXX FAMILY

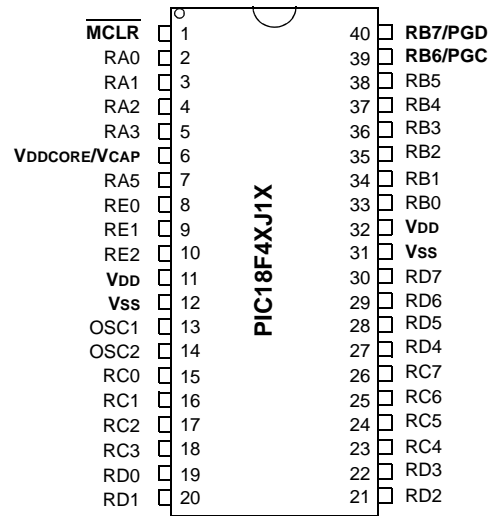
FIGURE 2-1: PIC18F2XJXX/4XJXX FAMILY PIN DIAGRAMS



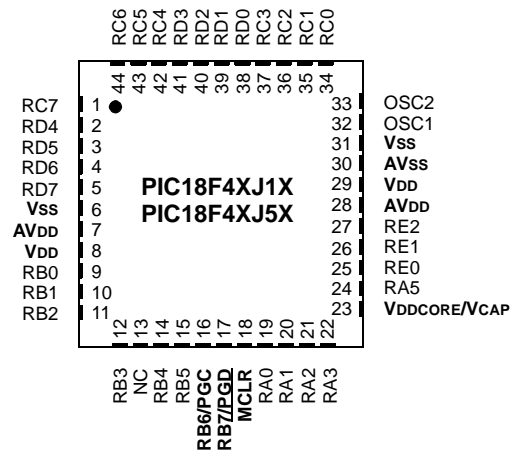
PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-2: PIC18F2XJXX/4XJXX FAMILY PIN DIAGRAMS (CONTINUED)

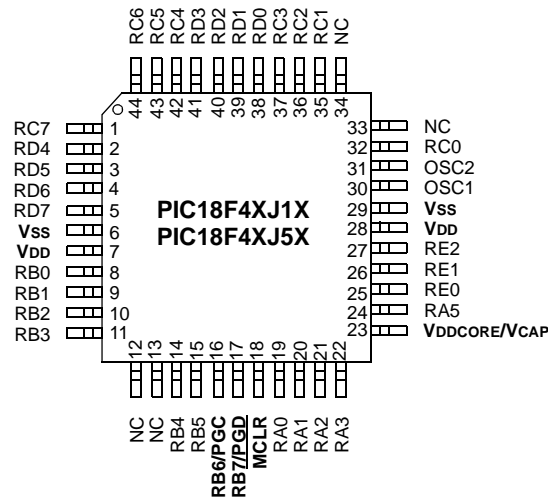
40-Pin PDIP



44-Pin QFN



44-Pin TQFP



PIC18F2XJXX/4XJXX FAMILY

The Configuration Words for these devices are located at addresses 300000h through 300007h. These are implemented as three pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the last four words (or eight bytes) of the code space (also called the Flash Configuration Words) should be written with Configuration data and not executable code. The addresses of the Flash Configuration Words are listed in Table 2-2. Refer to section **Section 5.0 “Configuration Word”** for more information.

Locations 3FFFEh and 3FFFFh are reserved for the Device ID bits. These bits, which may be used by the programmer to identify what device type is being programmed, are described in **Section 5.1 “Device ID Word”**. These Device ID bits read out normally, even after code protection.

2.2.1 MEMORY ADDRESS POINTER

Memory in the device address space (000000h to 3FFFFFFh) is addressed via the Table Pointer register, which in turn is comprised of three registers:

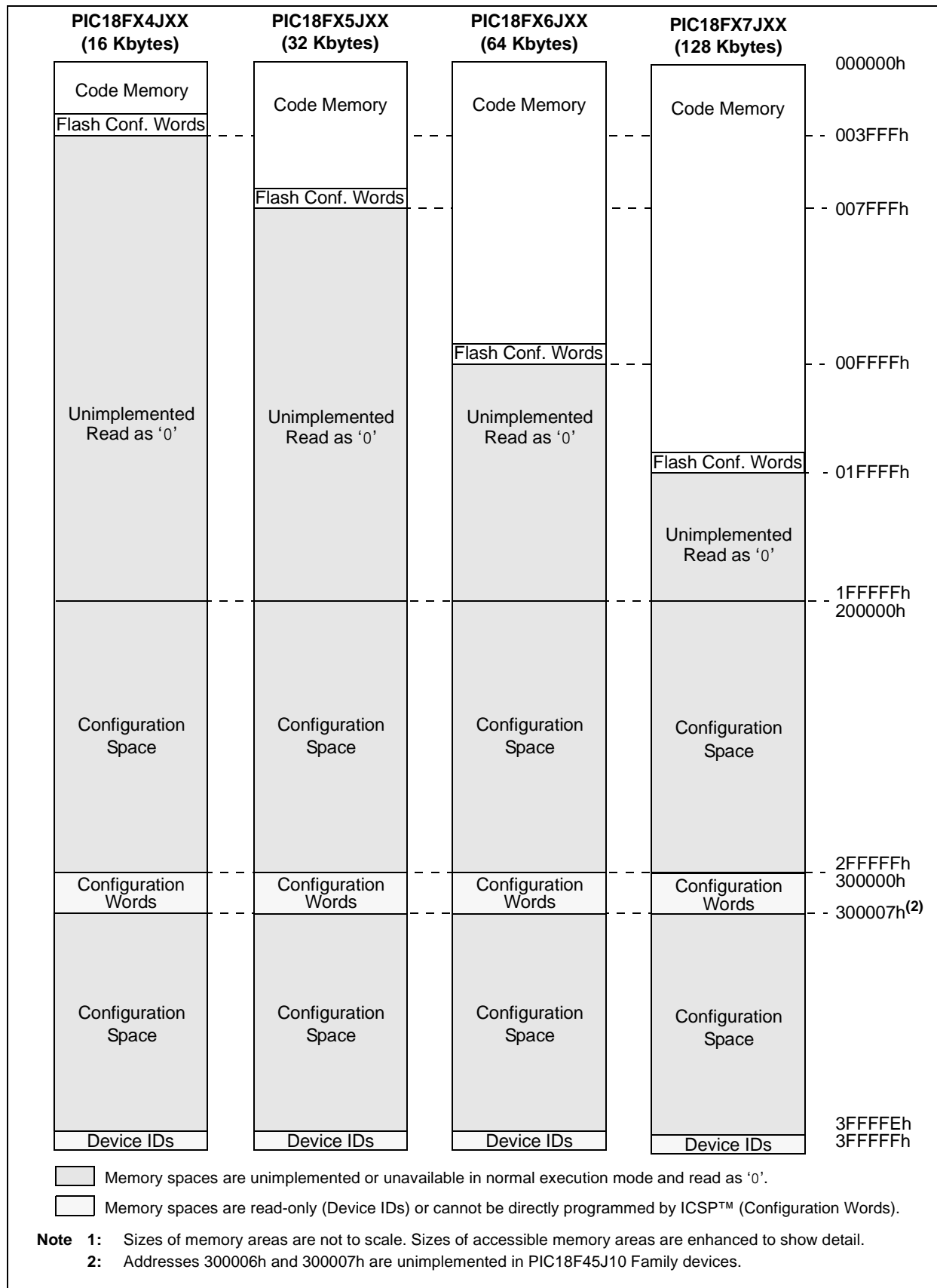
- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

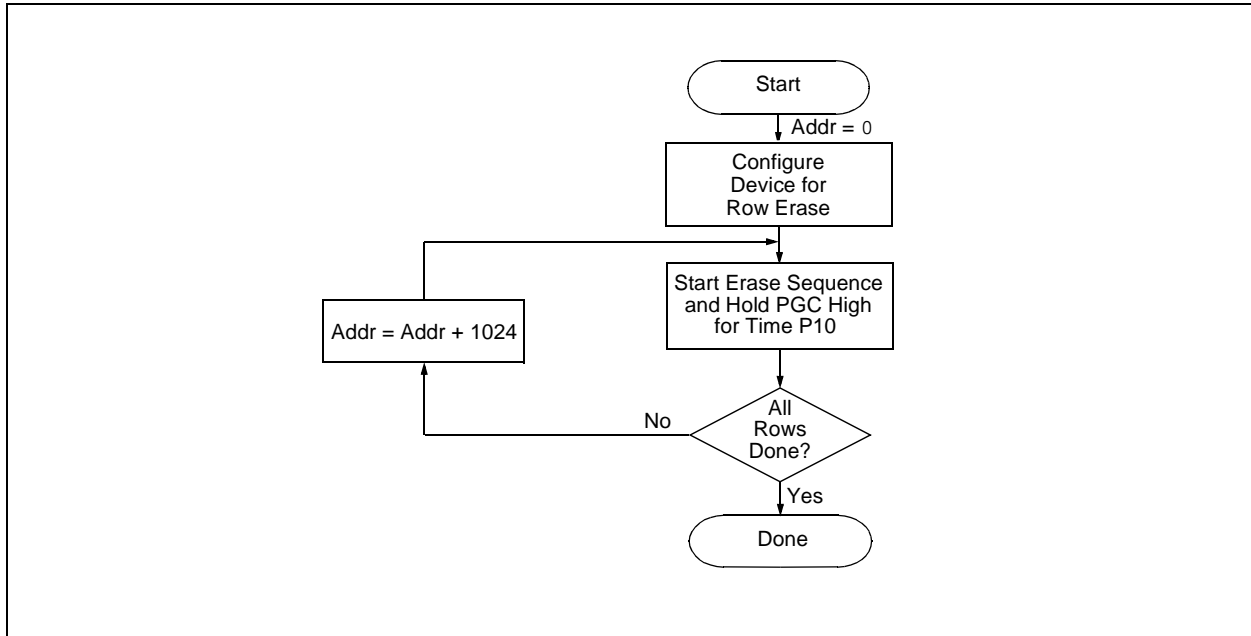
PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-4: MEMORY MAPS FOR PIC18F2XJXX/4XJXX FAMILY DEVICES⁽¹⁾



PIC18F2XJXX/4XJXX FAMILY

FIGURE 3-4: SINGLE ROW ERASE CODE MEMORY FLOW



PIC18F2XJXX/4XJXX FAMILY

FIGURE 3-5: PROGRAM CODE MEMORY FLOW

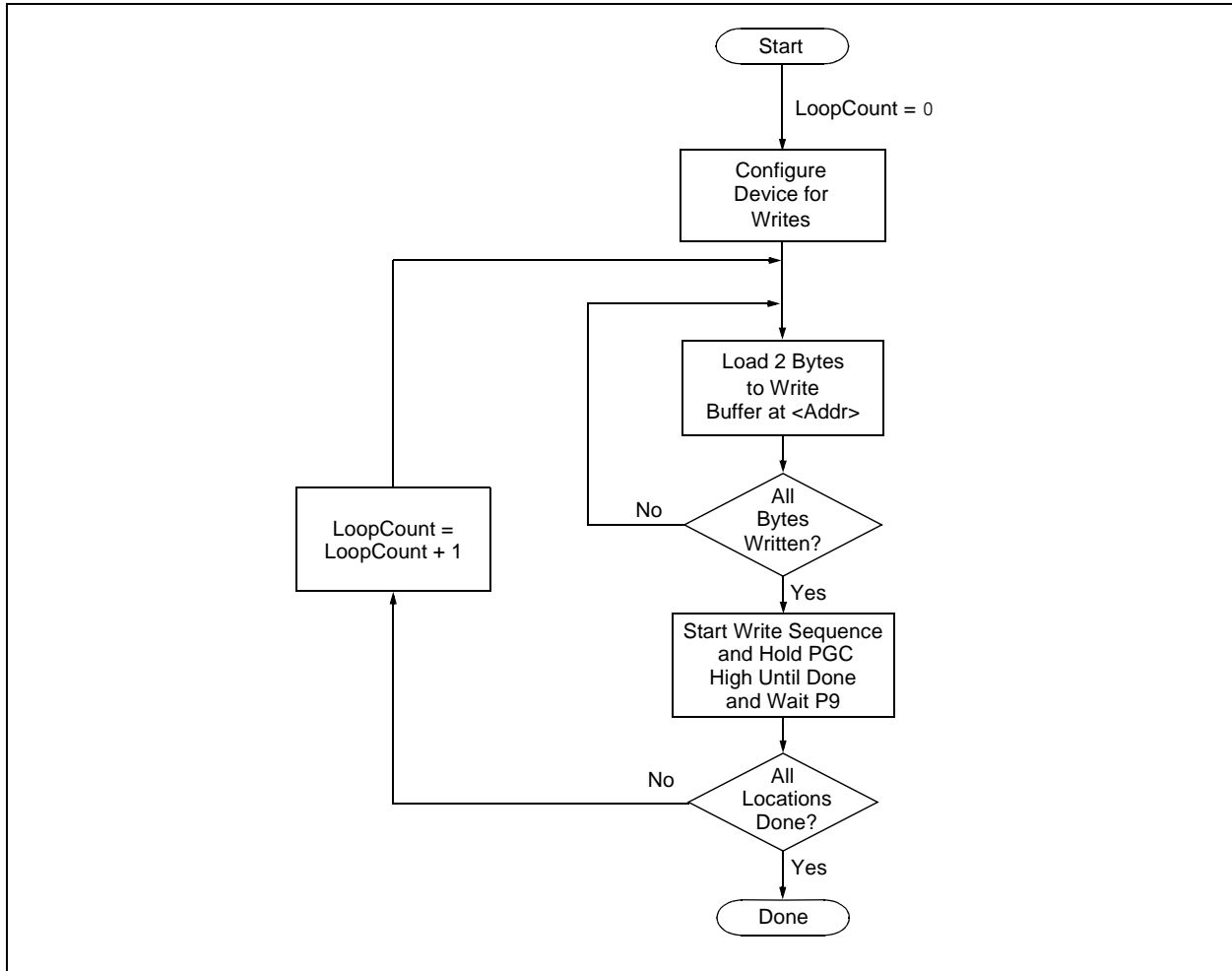
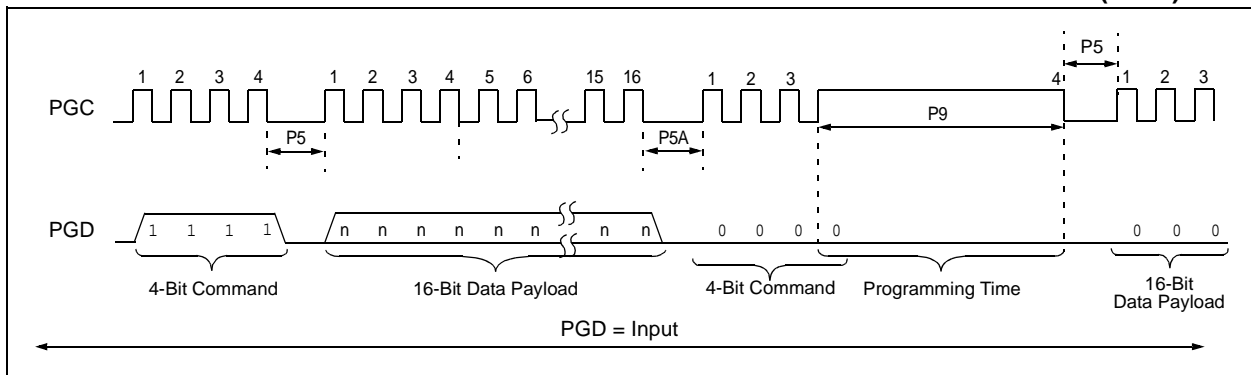


FIGURE 3-6: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



3.3 Endurance and Retention

To maintain the endurance specification of the Flash program memory cells, each byte should never be programmed more than once between erase operations. Before attempting to modify the contents of a specific byte of Flash memory a second time, an erase operation (either a Bulk Erase or a Row Erase which includes that byte) should be performed.

PIC18F2XJXX/4XJXX FAMILY

4.0 READING THE DEVICE

4.1 Read Code Memory

Code memory is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

The 4-bit command is shifted in LSb first. The read is executed during the next eight clocks, then shifted out on PGD during the last eight clocks, LSb to MSb. A

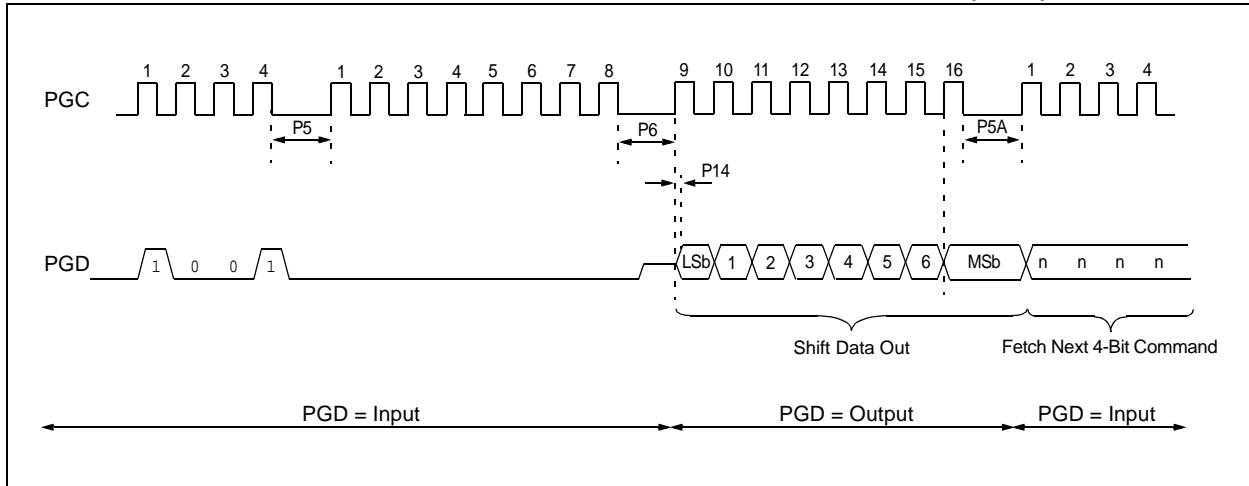
delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFFh address space, so it also applies to reading the Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ, POST-INCREMENT INSTRUCTION TIMING (1001)



PIC18F2XJXX/4XJXX FAMILY

TABLE 5-3: PIC18F45J10 FAMILY DEVICES: BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
DEBUG	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)
CP0	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
IESO	CONFIG2L	Internal/External Oscillator Switchover bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
FOSC2	CONFIG2L	Default Oscillator Select bit 1 = Clock designated by FOSC<1:0> is enabled as system clock when OSCCON<1:0> = 00 0 = INTRC is enabled as system clock when OSCCON<1:0> = 00
FOSC<1:0>	CONFIG2L	Primary Oscillator Select bits 11 = EC oscillator, PLL enabled and under software control, CLKO function on OSC2 10 = EC oscillator, CLKO function on OSC2 01 = HS oscillator, PLL enabled and under software control 00 = HS oscillator
WDTPS<3:0>	CONFIG2H	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
CCP2MX	CONFIG3H	CCP2 MUX bit 1 = CCP2 is multiplexed with RC1 0 = CCP2 is multiplexed with RB3

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-4: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDS

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value ⁽¹⁾
300000h CONFIG1L	DEBUG	XINST	STVREN	—	PLLDIV2 ⁽³⁾	PLLDIV1 ⁽³⁾	PLLDIV0 ⁽³⁾	WDTEN	111- 1111
300001h CONFIG1H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽⁴⁾	CP0	CPDIV1 ⁽³⁾	CPDIV0 ⁽³⁾	---- 0111
300002h CONFIG2L	IESO	FCMEN	—	LPT1OSC	T1DIG	FOSC2	FOSC1	FOSC0	11-1 1111
300003h CONFIG2H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300004h CONFIG3L	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0	DSWDTEN	DSBOREN	RTCOSC	DSWDTOSC	1111 1111
300005h CONFIG3H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	MSSPSMK	—	—	IOL1WAY	---- 1--1
300006h CONFIG4L	WPCFG	WPEND	WPFP5 ⁽⁵⁾	WPFP4 ⁽⁶⁾	WPFP3	WPFP2	WPFP1	WPFP0	1111 1111
300007h CONFIG4H	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	— ⁽²⁾	—	—	—	WPDIS	---- ---1
3FFFFEh DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx
3FFFFFh DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0100 00xx

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

3: These bits are not implemented in PIC18F46J11 family devices.

4: This bit should always be maintained at '0'.

5: This bit is not available on 32K and 16K memory devices (X4J11, X4J50, X5J11, and X5J50 devices) and should always be maintained at '0' on those devices.

6: This bit is not available on 16K memory devices (X4J11 and X4J50 devices) and should always be maintained at '0' on those devices.

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
DEBUG	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Enhanced Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
PLLDIV<2:0> ⁽³⁾	CONFIG1L	PLL Input Divider bits Divider must be selected to provide a 4 MHz input into the 96 MHz PLL. 111 = No divide – oscillator used directly (4 MHz input) 110 = Oscillator divided by 2 (8 MHz input) 101 = Oscillator divided by 3 (12 MHz input) 100 = Oscillator divided by 4 (16 MHz input) 011 = Oscillator divided by 5 (20 MHz input) 010 = Oscillator divided by 6 (24 MHz input) 001 = Oscillator divided by 10 (40 MHz input) 000 = Oscillator divided by 12 (48 MHz input)
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F46J11 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
CP0 ⁽⁴⁾	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
CPDIV<1:0> ⁽³⁾	CONFIG1H	CPU System Clock Selection bits 11 = No CPU system clock divide 10 = CPU system clock divided by 2 01 = CPU system clock divided by 3 00 = CPU system clock divided by 6
IESO	CONFIG2L ^(1,2)	Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L ^(1,2)	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
LPT1OSC	CONFIG2L ^(1,2)	Low-Power Timer1 Oscillator Enable bit 1 = Timer1 oscillator configured for low-power operation 0 = Timer1 oscillator configured for higher-power operation
T1DIG	CONFIG2L ^(1,2)	Secondary Clock Source T1OSCEN Enforcement bit ⁽¹⁾ 1 = Secondary oscillator clock source may be selected (OSCCON <1:0> = 01) regardless of T1OSCEN state 0 = Secondary oscillator clock source may not be selected unless T1CON <3> = 1
FOSC<2:0>	CONFIG2L ^(1,2)	Oscillator Selection bits 111 = EC+PLL (S/W controlled by PLEN bit), CLKO on RA6 110 = EC oscillator (PLL always disabled) with CLKO on RA6 101 = HS+PLL (S/W controlled by PLEN bit) 100 = HS oscillator (PLL always disabled) 011 = INTOSCPLLO, internal oscillator with PLL (S/W controlled by PLEN bit), CLKO on RA6, port function on RA7 010 = INTOSCPLL, internal oscillator with PLL (S/W controlled by PLEN bit), port function on RA6 and RA7 001 = INTOSCO, internal oscillator, INTOSC or INTRC (PLL always disabled), CLKO on RA6, port function on RA7 000 = INTOSC, internal oscillator INTOSC or INTRC (PLL always disabled), port function on RA6 and RA7
WDTPS<3:0>	CONFIG2H ^(1,2)	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F46J11 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
DSWTPS<3:0>	CONFIG3L	Deep Sleep Watchdog Timer Postscale Select bits The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms. 1111 = 1:2,147,483,648 (25.7 days) 1110 = 1:536,870,912 (6.4 days) 1101 = 1:134,217,728 (38.5 hours) 1100 = 1:33,554,432 (9.6 hours) 1011 = 1:8,388,608 (2.4 hours) 1010 = 1:2,097,152 (36 minutes) 1001 = 1:524,288 (9 minutes) 1000 = 1:131,072 (135 seconds) 0111 = 1:32,768 (34 seconds) 0110 = 1:8,192 (8.5 seconds) 0101 = 1:2,048 (2.1 seconds) 0100 = 1:512 (528 ms) 0011 = 1:128 (132 ms) 0010 = 1:32 (33 ms) 0001 = 1:8 (8.3 ms) 0000 = 1:2 (2.1 ms)
DSWDTEN	CONFIG3L	Deep Sleep Watchdog Timer Enable bit 1 = DSWDT enabled 0 = DSWDT disabled
DSBOREN	CONFIG3L	Deep Sleep BOR Enable bit 1 = BOR enabled in Deep Sleep 0 = BOR disabled in Deep Sleep (does not affect operation in non Deep Sleep modes)
RTCOSC	CONFIG3L	RTCC Reference Clock Select bit 1 = RTCC uses T1OSC/T1CKI as reference clock 0 = RTCC uses INTRC as reference clock
DSWDTOSC	CONFIG3L	DSWDT Reference Clock Select bit 1 = DSWDT uses INTRC as reference clock 0 = DSWDT uses T1OSC/T1CKI as reference clock
MSSPMSK ^(1,2)	CONFIG3H	MSSP 7-Bit Address Masking Mode Enable bit 1 = 7-Bit Address Masking mode enable 0 = 5-Bit Address Masking mode enable
IOL1WAY	CONFIG3H	IOLOCK Bit One-Way Set Enable bit 1 = The IOLOCK bit (PPSCON<0>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time. 0 = The IOLOCK bit (PPSCON<0>) can be set and cleared as needed, provided the unlock sequence has been completed.
WPCFG ⁽⁴⁾	CONFIG4L	Write/Erase Protect Configuration Words Page bit (valid when WPDIS = 0) 1 = Configuration Words page is not erase/write-protected unless WPEND and WPPF<5:0> settings include the Configuration Words page 0 = Configuration Words page is erase/write-protected, regardless of WPEND and WPPF<5:0> settings
WPEND	CONFIG4L	Write/Erase Protect Region Select bit (valid when WPDIS = 0) 1 = Flash pages, WPPF<5:0> to Configuration Words page, are write/erase-protected 0 = Flash pages, 0 to WPPF<5:0> are write/erase-protected

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F46J11 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WPFP<5:0>	CONFIG4L	Write/Erase Protect Page Start/End Location bits Used with WPEND bit to define which pages in Flash will be write/erase-protected.
WPDIS	CONFIG4H	Write Protect Disable bit 1 = WPFP<5:0>, WPEND and WPCFG bits ignored; all Flash memory may be erased or written 0 = WPFP<5:0>, WPEND and WPCFG bits enabled; write/erase-protect active for the selected region(s)
DEV<2:0>	DEVID1	Device ID bits Used with the DEV<10:3> bits in the Device ID Register 2 to identify the part number.
REV<4:0>	DEVID1	Revision ID bits Indicate the device revision.
DEV<10:3>	DEVID2	Device ID bits Used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number.

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F46J11 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

TABLE 5-6: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value ⁽¹⁾
300000h	CONFIG1L	DEBUG	XINST	STVREN	CFGPLEN	PLLDIV2	PLLDIV1	PLLDIV0	WDTEN	111- 1111
300001h	CONFIG1H	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	__ ⁽⁴⁾	CP0	CPDIV1 ⁽³⁾	CPDIV0 ⁽³⁾	---- 0111
300002h	CONFIG2L	IESO	FCMEN	CLKOEC	SOSCSEL1	SOSCSEL0	FOSC2	FOSC1	FOSC0	1111 1111
300003h	CONFIG2H	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300004h	CONFIG3L	DSWDTPS3	DSWDTPS2	DSWDTPS1	DSWDTPS0	DSWDTEN	DSBOREN	RTCOSC	DSWDTOSC	1111 1111
300005h	CONFIG3H	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	MSSPMSK	PLLSEL	ADCSEL	IOL1WAY	---- 1111
300006h	CONFIG4L	WPCFG	WPFP6	WPFP5	WPFP4	WPFP3	WPFP2	WPFP1	WPFP0	1111 1111
300007h	CONFIG4H	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	__ ⁽²⁾	LS48MHZ ⁽³⁾	—	WPEND	WPDIS	---- 1-11
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0101 10xx

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

- Note 1:** Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.
Note 2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.
Note 3: These bits are not implemented in PIC18F47J13 family devices.
Note 4: This bit should always be maintained at '0'.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-7: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
DEBUG	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Enhanced Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
CFGPLLEN	CONFIG1L	Enable PLL on Start-up bit 1 = PLL enabled on start-up. Not recommended for low-voltage designs. 0 = PLL disabled on start-up. Firmware may later enable PLL through OSCTUNE<6>.
PLLDIV<2:0>	CONFIG1L	96 MHz PLL Input Divider bits Divider must be selected to provide a 4 MHz input into the 96 MHz PLL. 111 = No divide – oscillator used directly (4 MHz input) 110 = Oscillator divided by 2 (8 MHz input) 101 = Oscillator divided by 3 (12 MHz input) 100 = Oscillator divided by 4 (16 MHz input) 011 = Oscillator divided by 5 (20 MHz input) 010 = Oscillator divided by 6 (24 MHz input) 001 = Oscillator divided by 10 (40 MHz input) 000 = Oscillator divided by 12 (48 MHz input)
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on the SWDTEN bit)
CP0 ⁽⁴⁾	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
CPDIV<1:0> ⁽³⁾	CONFIG1H	CPU System Clock Selection bits 11 = No CPU system clock divide 10 = CPU system clock divided by 2 01 = CPU system clock divided by 3 00 = CPU system clock divided by 6
IESO	CONFIG2L ^(1,2)	Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L ^(1,2)	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
CLKOEC	CONFIG2L	EC Mode Clock Output Enable bit 1 = CLKO output signal active on the RA6 pin (EC mode only) 0 = CLKO output disabled
SOSCSEL<1:0>	CONFIG2L	Secondary Oscillator Circuit Selection bits 11 = High-power SOSC circuit selected 10 = Digital Input mode (SCLKI) 01 = Low-power SOSC circuit selected 00 = Reserved

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F47J13 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

5: Not implemented on PIC18F47J53 family devices.

PIC18F2XJXX/4XJXX FAMILY

5.1 Device ID Word

The Device ID Word for the PIC18F2XJXX/4XJXX Family devices is located at 3FFFFEh:3FFFFFh. These read-only bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code protection has been enabled. The process for reading the Device IDs is shown in Figure 5-1. A complete list of Device ID values for the PIC18F2XJXX/4XJXX Family is presented in Table 5-8.

FIGURE 5-1: READ DEVICE ID WORD FLOW

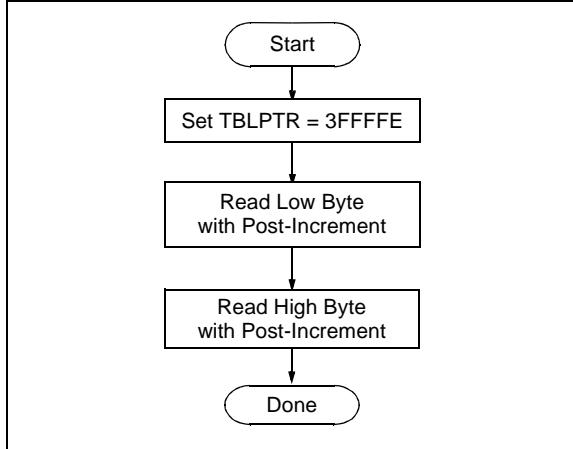


TABLE 5-8: DEVICE ID VALUE

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F24J10	1Dh	000x xxxx
PIC18F25J10	1Ch	000x xxxx
PIC18F44J10	1Dh	001x xxxx
PIC18F45J10	1Ch	001x xxxx
PIC18LF24J10	1Dh	010x xxxx
PIC18LF25J10	1Ch	010x xxxx
PIC18LF44J10	1Dh	011x xxxx
PIC18LF45J10	1Ch	011x xxxx
PIC18F25J11	4Dh	101x xxxx
PIC18F24J11	4Dh	100x xxxx
PIC18F26J11	4Dh	110x xxxx
PIC18F45J11	4Eh	000x xxxx
PIC18F44J11	4Dh	111x xxxx
PIC18F46J11	4Eh	001x xxxx
PIC18F24J50	4Ch	000x xxxx
PIC18F25J50	4Ch	001x xxxx
PIC18F26J50	4Ch	010x xxxx
PIC18F44J50	4Ch	011x xxxx
PIC18F45J50	4Ch	100x xxxx

TABLE 5-8: DEVICE ID VALUE (CONTINUED)

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F46J50	4Ch	101x xxxx
PIC18LF2450	4Ch	110x xxxx
PIC18LF25J50	4Ch	111x xxxx
PIC18LF26J50	4Dh	000x xxxx
PIC18LF44J50	4Dh	001x xxxx
PIC18LF45J50	4Dh	010x xxxx
PIC18LF46J50	4Dh	011x xxxx
PIC18LF24J11	4Eh	010x xxxx
PIC18LF25J11	4Eh	011x xxxx
PIC18LF26J11	4Eh	100x xxxx
PIC18LF44J11	4Eh	101x xxxx
PIC18LF45J11	4Eh	110x xxxx
PIC18LF46J11	4Eh	111x xxxx
PIC18F26J13	59h	001x xxxx
PIC18F27J13	59h	011x xxxx
PIC18F46J13	59h	101x xxxx
PIC18F47J13	59h	111x xxxx
PIC18LF26J13	5Bh	001x xxxx
PIC18LF27J13	5Bh	011x xxxx
PIC18LF46J13	5Bh	101x xxxx
PIC18LF47J13	5Bh	111x xxxx
PIC18F26J53	58h	001x xxxx
PIC18F27J53	58h	011x xxxx
PIC18F46J53	58h	101x xxxx
PIC18F47J53	58h	111x xxxx
PIC18LF26J53	5Ah	001x xxxx
PIC18LF27J53	5Ah	011x xxxx
PIC18LF46J53	5Ah	101x xxxx
PIC18LF47J53	5Ah	111x xxxx

5.2 Checksum Computation

The checksum is calculated by summing the contents of all code memory locations and the device Configuration Words, appropriately masked. The Least Significant 16 bits of this sum are the checksum.

The checksum calculation differs depending on whether or not code protection is enabled. Since the code memory locations read out differently depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Words can always be read.

PIC18F2XJXX/4XJXX FAMILY

Table 5-9 describes how to calculate the checksum for each device.

TABLE 5-9: CHECKSUM COMPUTATION

Device	Code Protection	Checksum
PIC18F24J10 PIC18F44J10	Off	SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & 04h) + ([003FFA] & C7h) + ([003FFB] & 0Fh) + ([003FFD] & 01h)
	On	0000h
PIC18F24J11 PIC18F44J11	Off	SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & FCh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h)
	On	0000h
PIC18F24J50 PIC18F44J50	Off	SUM[000000:003FF7] + ([003FF8] & EFh) + ([003FF9] & FFh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h)
	On	0000h
PIC18F25J10 PIC18F45J10	Off	SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & 04h) + ([007FFA] & C7h) + ([007FFB] & 0Fh) + ([007FFD] & 01h)
	On	0000h
PIC18F25J11 PIC18F45J11	Off	SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & FCh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h)
	On	0000h
PIC18F25J50 PIC18F45J50	Off	SUM[000000:007FF7] + ([007FF8] & EFh) + ([007FF9] & FFh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h)
	On	0000h
PIC18F26J11 PIC18F46J11	Off	SUM[000000:00FFF7] + ([00FFF8] & E1h) + ([00FFF9] & FCh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h)
	On	0000h
PIC18F26J50 PIC18F46J50	Off	SUM[000000:00FFF7] + ([00FFF8] & EFh) + ([00FFF9] & FFh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h)
	On	0000h
PIC18F26J13 PIC18F46J13	Off	SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FCh) + ([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FFh) + ([00FFFE] & BFh) + ([00FFFF] & F3h)
	On	0000h
PIC18F26J53 PIC18F46J53	Off	SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FFh) + ([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FBh) + ([00FFFE] & BFh) + ([00FFFF] & FBh)
	On	0000h
PIC18F27J13 PIC18F47J13	Off	SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FCh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FFh) + ([01FFFE] & FFh) + ([01FFFF] & F3h)
	On	0000h
PIC18F27J53 PIC18F47J53	Off	SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FFh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FBh) + ([01FFFE] & FFh) + ([01FFFF] & FBh)
	On	0000h

Legend: [a] = Value at address a; SUM[a:b] = Sum of locations a to b inclusive; + = Addition; & = Bitwise AND.
All addresses are hexadecimal.

PIC18F2XJXX/4XJXX FAMILY

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions							
Operating Temperature: 25°C is recommended							
Param No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
	VDDCORE	External Supply Voltage for Microcontroller Core During Programming Operations (PIC18LF devices)		2.25	2.75	V	(Note 1)
D111	VDD	Supply Voltage During Programming	PIC18LFXXJXX	VDDCORE	3.60	V	Normal programming (Note 2)
			PIC18FXXJ10	2.70	3.60	V	
			PIC18FXXJ50	2.35	3.60	V	
			PIC18FXXJ11				
			PIC18FXXJ53				
PIC18FXXJ13							
D112	IPP	Programming Current on MCLR		—	5	μA	
D113	IDDP	Supply Current During Programming		—	10	mA	
D031	VIL	Input Low Voltage		VSS	0.2 VDD	V	
D041	VIH	Input High Voltage		0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage		—	0.4	V	IO L = 3.4 mA @ 3.3V
D090	VOH	Output High Voltage		2.4	—	V	IO H = -2.0 mA @ 3.3V
D012	CIO	Capacitive Loading on I/O pin (PGD)		—	50	pF	To meet AC specifications
	CF	Filter Capacitor Value on VCAP	PIC18LFXXJXX	0.1	—	μF	(Note 1)
			PIC18FXXJ10	4.7	18	μF	
			PIC18FXXJ13	5.4	18	μF	
			PIC18FXXJ11				
			PIC18FXXJ5X				

- Note 1:** External power must be supplied to the VDDCORE/V_{CAP} pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 “PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX Devices and the On-Chip Voltage Regulator”** for more information.
- 2:** VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

PIC18F2XJXX/4XJXX FAMILY

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions Operating Temperature: 25°C is recommended						
Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
P1	Tr	MCLR Rise Time to Enter Program/Verify mode	—	1.0	μs	
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	
P2A	TPGCL	Serial Clock (PGC) Low Time	50	—	ns	
P2B	TPGCH	Serial Clock (PGC) High Time	50	—	ns	
P3	TSET1	Input Data Setup Time to Serial Clock ↓	20	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	20	—	ns	
P5	TDLY1	Delay Between 4-Bit Command and Command Operand	50	—	ns	
P5A	TDLY1A	Delay Between 4-Bit Command Operand and Next 4-Bit Command	50	—	ns	
P6	TDLY2	Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	Delay to allow Block Programming to occur	3.4	—	ms	PIC18F2XJ10/PIC18F4XJ10
			1.2	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ5X/PIC18F4XJ5X
P10	TDLY6	Delay to allow Row Erase to occur	49	—	ms	PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53
			54	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50
P11	TDLY7	Delay to allow Bulk Erase to occur	475	—	ms	PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53
			524	—	ms	PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50
P12	THLD2	Input Data Hold Time from MCLR ↑	400	—	μs	
P13	TSET2	VDD ↑ Setup Time to MCLR ↑	100	—	ns	
P14	TVALID	Data Out Valid from PGC ↑	25	—	ns	
P16	TDLY8	Delay between Last PGC ↓ and MCLR ↓	20	—	ns	
P17	THLD3	MCLR ↓ to VDD ↓	3	—	μs	
P19	TKEY1	Delay from First MCLR ↓ to First PGC ↑ for Key Sequence on PGD	4	—	ms	
P20	TKEY2	Delay from Last PGC ↓ for Key Sequence on PGD to Second MCLR ↑	50	—	ns	

- Note 1:** External power must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 “PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX Devices and the On-Chip Voltage Regulator”** for more information.
- 2:** VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC³² logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2008-2015, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63277-874-1

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

07/14/15