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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K × 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064h-i-mr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

TABLE 3-3: MIPS32[®] M4K[®] PROCESSOR CORE EXCEPTION TYPES

3.3 Power Management

The MIPS[®] M4K[®] processor core offers a number of power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 27.0 "Power-Saving Features".

3.3.2 LOCAL CLOCK GATING

The majority of the power consumed by the PIC32MX330/350/370/430/450/470 family core is in the clock tree and clocking registers. The PIC32MX family uses extensive use of local gated-clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The MIPS[®] M4K[®] processor core provides for an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K[®] core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R	R	R	R	R	R	R	R		
31:24		BMXDRMSZ<31:24>								
22:16	R	R	R	R	R	R	R	R		
23.10	BMXDRMSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXDRMSZ<15:8>									
7.0	R	R	R	R	R	R	R	R		
7:0				BMXDR	MSZ<7:0>					

BMXDRMSZ: DATA RAM SIZE REGISTER **REGISTER 4-5:**

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXDRMSZ<31:0>: Data RAM Memory (DRM) Size bits

Static value that indicates the size of the Data RAM in bytes: 0x00004000 = Device has 16 KB RAM 0x00008000 = Device has 32 KB RAM 0x00010000 = Device has 64 KB RAM 0x00020000 = Device has 128 KB RAM

REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	_	—	_	—	BMXPUPBA<19:16>				
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	
15:8	BMXPUPBA<15:8>								
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				BMXPU	PBA<7:0>				

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-20 Unimplemented: Read as '0'

bit 19-11 BMXPUPBA<19:11>: Program Flash (PFM) User Program Base Address bits

bit 10-0 BMXPUPBA<10:0>: Read-Only bits Value is always '0', which forces 2 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernel mode data usage.

2: The value in this register must be less than or equal to BMXPFMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	-	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	LVDSTAT ⁽¹⁾	—	—	—
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	-	—	—	NVMOP<3:0>			

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	nd as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	WR: Write Control bit
	This bit is writable when WREN = 1 and the unlock sequence is followed.
	1 = Initiate a Flash operation. Hardware clears this bit when the operation completes
	0 = Flash operation complete or inactive
bit 14	WREN: Write Enable bit
	1 = Enable writes to WR bit and enables LVD circuit
	0 = Disable writes to WR bit and disables LVD circuit
	This is the only bit in this register reset by a device Reset.
bit 13	WRERR: Write Error bit ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 Program or erase sequence did not complete successfully
	0 = Program or erase sequence completed normally
bit 12	LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	1 = Low-voltage detected (possible data corruption, if WRERR is set)
	0 = Voltage level is acceptable for programming
bit 11	LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set, and cleared, by hardware.
	1 = Low-voltage event active
	0 = Low-voltage event NOT active
bit 10-4	Unimplemented: Read as '0'
bit 3-0	NVMOP<3:0>: NVM Operation bits
	These bits are writable when WREN = 0.
	1111 = Reserved
	0111 = Reserved
	0110 = No operation
	0101 = Program Flash (PFM) erase operation: erases PFM, if all pages are not write-protected
	0100 = Page erase operation: erases page selected by NVMADDR, if it is not write protected
	0011 = No operation
	0001 = Word program operation: programs word selected by NVMADDR, if it is not write-protected
	0000 = No operation

Note 1: This bit is cleared by setting NVMOP = 0000, and initiating a Flash operation (i.e., WR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Legend:

R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 IFS31-IFS0: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 IEC31-IEC0: Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	—	—	—		IP3<2:0>		IS3<	:1:0>
23.16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	—	—	—		IP2<2:0>		IS2<	:1:0>
15.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	—	—	—		IP1<2:0>		IS1<	:1:0>
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	_	_	_		IP0<2:0>		IS0<	:1:0>

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown



Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22:16	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	_	—	—	—	—	_	—	—
7.0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_			TUN<	5:0>(1)		

REGISTER 8-2: OSCTUN: FRC TUNING REGISTER

Legend:	y = Value set from Configuration bits on POR							
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 31-6 Unimplemented: Read as '0'

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation, and is neither characterized nor tested.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

12.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the peripheral pin select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 12-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 12-2 and Figure 12-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 12-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



12.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

12.3.6.1 Control Register Lock

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the IOLOCK Configuration bit (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

12.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The IOL1WAY Configuration bit (DEVCFG3<29>) blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

15.1 Watchdog Timer Control Registers

DS6000	
)1185F-p	
bage 1	
78	

TABLE 15-1: WATCHDOG TIMER CONTROL REGISTER MAP

ess	Register Name ⁽¹⁾ Bit Range	Bits													<i>(</i> 0				
Virtual Addr (BF80_#)		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0000		31:16	_	_	_	_	-	—	—	—	_	_	_	-	-	-	—	_	0000
0000	WDICON	15:0	ON	_	_	_	_	_	_	_	_		SV	VDTPS<4:()>		WDTWINEN	WDTCLR	0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

REGIS	TER 18-1:	SPIxCON: S	SPI CONTROL REGISTER (CONTINUED)									
bit 17	SPIFE: F	rame Sync Puls	e Edge Select bit (Framed SPI mode only)									
	1 = Fran	ne synchronizati	on pulse coincides with the first bit clock									
1.11.40		ne synchronizati	on pulse precedes the first bit clock									
bit 16		-: Enhanced Buf	ter Enable bit ⁽²⁾									
	1 - Enna	anced Buffer mo	de is disabled									
bit 15		ON: SPI Peripheral On bit ⁽¹⁾										
bit io	1 = SPI	Peripheral is ena	abled									
	0 = SPI	Peripheral is dis	abled									
bit 14	Unimple	mented: Read a	as '0'									
bit 13	SIDL: St	op in Idle Mode I	bit									
	1 = Disc	ontinue operatio	n when CPU enters in Idle mode									
	0 = Con	tinue operation i	n Idle mode									
bit 12	DISSDO	Disable SDOx	pin bit									
	1 = SDC	Dx pin is not used	d by the module. Pin is controlled by associated PORT register									
bit 11		22 16 - 22/16 Pi	t Communication Select hite									
DIL 11-	When Al	JDFN = 1:										
	MODE32	2 MODE16	Communication									
	1	1	24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame									
	1	0	32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame									
	0	1	16-bit Data, 16-bit FIFO, 32-bit Channel/64-bit Frame									
	0	0	16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame									
		$\frac{\text{JDEN} = 0}{\text{NODE10}}$	O manufaction									
	MODE32	MODE16	Communication 32-bit									
	1 0	1	16-bit									
	0	0	8-bit									
bit 9	SMP: SF	PI Data Input Sar	nple Phase bit									
	Master m	node (MSTEN =	<u>1):</u>									
	1 = Inpu	t data sampled a	at end of data output time									
	0 = Inpu Slave mo	t data sampled a $de (MSTEN = 0$	at mode of data output time									
	SMP value	ue is ignored wh	en SPI is used in Slave mode. The module always uses SMP = 0.									
bit 8	CKE: SF	PI Clock Edge Se	elect bit ⁽³⁾									
	1 = Seria	al output data ch	anges on transition from active clock state to Idle clock state (see CKP bit)									
	0 = Seri	al output data ch	anges on transition from Idle clock state to active clock state (see CKP bit)									
bit 7	SSEN: S	lave Select Ena	ble (Slave mode) bit									
	$1 = \frac{SSX}{SSX}$	pin used for Sla	ve mode									
hit 6	0 - 33X	pin not used for	slave mode, pin controlled by port function.									
DILO	1 = Idle	state for clock is	a high level: active state is a low level									
	0 = Idle	state for clock is	a low level; active state is a high level									
bit 5	MSTEN:	Master Mode E	nable bit									
	1 = Mas	ter mode										
	0 = Slav	e mode										
	4 \A/											
Note		sing the 1:1 PBC	LK divisor, the user software should not read or write the peripheral's SFRs in the roly following the instruction that clears the medule's ON bit									
	0100LM 2. This hit		en when the ON hit = 0									
4	2. 1115 UIL (2. This bit i		En when the ON Dit = 0. a Framed SDI mode. The user should program this bit to '0' for the Framed SDI									
•	mode (F	RMEN = 1).	e ramed or rindue. The user should program this bit to 0 for the riamed SPI									
	4: When A	UDEN = 1. the S	PI module functions as if the CKP bit is equal to '1'. regardless of the actual value									
	of CKP.	_,										

22.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32 RTCC module is intended for applications in which accurate time must be maintained for extended periods of time with minimal or no CPU intervention. Low-power optimization provides extended battery lifetime while keeping track of time. The following are key features of this module:

- · Time: hours, minutes and seconds
- 24-hour format (military time)
- · Visibility of one-half second period
- Provides calendar: Weekday, date, month and year
- Alarm intervals are configurable for half of a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week, one month and one year
- · Alarm repeat with decrementing counter
- · Alarm with indefinite repeat: Chime
- Year range: 2000 to 2099
- · Leap year correction
- · BCD format for smaller firmware overhead
- Optimized for long-term battery operation
- · Fractional second synchronization
- User calibration of the clock crystal frequency with auto-adjust
- Calibration range: ±0.66 seconds error per month
- · Calibrates up to 260 ppm of crystal error
- Requirements: External 32.768 kHz clock crystal
- Alarm pulse or seconds clock output on RTCC pin



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22.1 Control Registers

TABLE 22-1: RTCC REGISTER MAP

ess											Bits								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0200	PTCCON	31:16	—	—	—	—	_	— — CAL<9:0>						0000					
0200	RICCON	15:0	ON	_	SIDL	—	_	—	-		RTSECSEL	RTCCLKON	—	_	RTCWREN	RTCSYNC	HALFSEC	RTCOE	0000
0210		31:16		_	_	—		_			—	_	_	_	_	_	_	—	0000
0210	RICALNI	15:0	ALRMEN	CHIME	PIV	ALRMSYNC		AMASI	< <3:0>					ARPT	<7:0>				0000
0220	DTOTIME	31:16		HR1	0<3:0>			HR01<3:0>		MIN10<3:0>				MIN01<3:0>			xxxx		
0220	RICHWL	15:0		SEC	10<3:0>		SEC01<3:0>						_					xx00	
0230	DTODATE	31:16		YEAR	10<3:0>			YEAR0	1<3:0>			MONTH10)<3:0>			MONTH	01<3:0>		xxxx
0230	RICDAIL	15:0		DAY1	0<3:0>			DAY01	1<3:0>		_	_	_	_		WDAY0	1<3:0>		xx00
0240		31:16		HR1	0<3:0>			HR01	<3:0>			MIN10<	3:0>			MIN01	<3:0>		xxxx
0240		15:0		SEC	10<3:0>			SEC0 ²	1<3:0>		_	_	_	_	_	_	_	—	xx00
0250		31:16		_	_	—		_				MONTH10)<3:0>			MONTH	01<3:0>		00xx
0230	250 ALRMDATE	15:0		DAY1	0<3:0>			DAY01	1<3:0>		_	_	—	_		WDAY0	1<3:0>		xx0x

PIC32MX330/350/370/430/450/470

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
51.24	_	_	_	—	—	_	—	—				
00:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23.10	—	—	—	—	—	—	—	—				
45.0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0				
15.8	ALRMEN ^(1,2)	CHIME ⁽²⁾	PIV ⁽²⁾	ALRMSYNC ⁽³⁾		AMASK	<3:0> ⁽³⁾					
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
7:0	ARPT<7:0> ⁽³⁾											

REGISTER 22-2: RTCALRM: RTC ALARM CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ALRMEN: Alarm Enable bit^(1,2)
 - 1 = Alarm is enabled
 - 0 = Alarm is disabled

bit 14 CHIME: Chime Enable bit⁽²⁾

- 1 = Chime is enabled ARPT<7:0> is allowed to rollover from 0x00 to 0xFF
- 0 = Chime is disabled ARPT<7:0> stops once it reaches 0x00

bit 13 **PIV:** Alarm Pulse Initial Value bit⁽²⁾

When ALRMEN = 0, PIV is writable and determines the initial value of the Alarm Pulse. When ALRMEN = 1, PIV is read-only and returns the state of the Alarm Pulse.

bit 12 ALRMSYNC: Alarm Sync bit⁽³⁾

- 1 = ARPT<7:0> and ALRMEN may change as a result of a half second rollover during a read. The ARPT must be read repeatedly until the same value is read twice. This must be done since multiple bits may be changing, which are then synchronized to the PB clock domain
- 0 = ARPT<7:0> and ALRMEN can be read without concerns of rollover because the prescaler is > 32 RTC clocks away from a half-second rollover

bit 11-8 AMASK<3:0>: Alarm Mask Configuration bits⁽³⁾

- 0000 = Every half-second
- 0001 = Every second
- 0010 = Every 10 seconds
- 0011 = Every minute
- 0100 = Every 10 minutes
- 0101 = Every hour
- 0110 = Once a day
- 0111 = Once a week
- 1000 = Once a month
- 1001 = Once a year (except when configured for February 29, once every four years)
- 1010 = Reserved; do not use
- 1011 = Reserved; do not use
- 11xx = Reserved; do not use
- **Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
 - 2: This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
 - 3: This assumes a CPU read will execute in less than 32 PBCLKs.

Note: This register is reset only on a Power-on Reset (POR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
10.0	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
7:0	_	_	_	_	_	_	C2OUT	C10UT

REGISTER 24-2: CMSTAT: COMPARATOR STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

bit 13 SIDL: Stop in IDLE Control bit

1 = All Comparator modules are disabled in IDLE mode

0 = All Comparator modules continue to operate in the IDLE mode

- bit 12-2 Unimplemented: Read as '0'
- bit 1 **C2OUT:** Comparator Output bit
 - 1 = Output of Comparator 2 is a '1'
 - 0 = Output of Comparator 2 is a '0'

bit 0 C1OUT: Comparator Output bit

- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid. To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TARI E 27-1·	PERIPHERAL MODULE DISABLE BITS AND LOCATIONS
IADLE ZI-I.	FERIFIERAL MODULE DISABLE DITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
СТМИ	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
UART3	U3MD	PMD5<2>
UART4	U4MD	PMD5<3>
UART5	U5MD	PMD5<4>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
12C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See TABLE 1: "PIC32MX330/350/ 370/430/450/470 Controller Family Features" for the lists of available peripherals.

2: Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

TABLE 28-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

ess										Bits									s
Virtual Addr (BFC0_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
2550		31:16	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	_	—	_	-	_	_	_	_	—	FS	SRSSEL<2:	0>	xxxx
2660	DEVCEGS	15:0								USERID<1	5:0>								xxxx
2554		31:16			_	—	—	—					—		_	FP	LLODIV<2:	0>	xxxx
2664	DEVCFGZ	15:0	UPLLEN ⁽¹⁾		—	—	—	UPI	LIDIV<2:0>	(1)	-	FF	PLLMUL<2:	0>	—	FF	PLLIDIV<2:()>	xxxx
2550		31:16			_	_	—	_	FWDTWI	NSZ<1:0>	FWDTEN	WINDIS	—		١	WDTPS<4:()>		xxxx
2660	DEVCEGI	15:0	FCKSM	<1:0>	FPBD	IV<1:0>	—	OSCIOFNC	POSCM	OD<1:0>	IESO	-	FSOSCEN		—	F	NOSC<2:0	>	xxxx
2550		31:16	_	—	_	CP	_	—	—	BWP	—	—	—	—		PWP	<7:4>		xxxx
ZFFC	DEVCEGU	15:0		PWP<	<3:0>		_	_				-	_	ICESE	L<1:0>	JTAGEN	DEBU	G<1:0>	xxxx

Legend: x = unknown value on Reset; - = reserved, write as '1'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on devices with a USB module.

TABLE 28-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

ess		6		Bits															
Virtual Addr (BF80 #)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5000		31:16						0000											
FZUU	CFGCON	15:0	—	—	IOLOCK	PMDLOCK	DCK — — — — — — — — JTAGEN TROEN — 1						TDOEN	000B					
E00(31:16	VER<3:0> DEVID<27:16> xx:					xxxx ⁽¹⁾											
FZZU) DEVID	15:0	DEVID<15:0> xxxx						xxxx ⁽¹⁾										
EDD	SVSKEV	31:16							0000										
FZOU) STOKET	15:0								STORE	1~51.0~								0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: Reset values are dependent on the device variant.

$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				-								
R R	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24 VER<3:0>(1) DEVID<27:24>(1) 23:16 R R R R R R DEVID<23:16>(1) 15:8	04.04	R	R	R	R	R	R	R	R			
R R	31:24		VER•	<3:0> (1)		DEVID<27:24> ⁽¹⁾						
Z3:10 DEVID<23:16>(1) 15:8 R	00.40	R	R	R	R	R	R	R	R			
15:8 R R R R R R R R	23:10	DEVID<23:16>(1)										
15.8	45.0	R	R	R	R	R	R	R	R			
DEVID<15:8>(1)	15:8	DEVID<15:8> ⁽¹⁾										
R R R R R R R R R	7.0	R	R	R	R	R	R	R	R			
7:0 DEVID<7:0>(1)	7:0				DEVID<	:7:0>(1)						

REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER

Legend:

zogonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 VER<3:0>: Revision Identifier bits⁽¹⁾

bit 27-0 **DEVID<27:0>:** Device ID⁽¹⁾

Note 1: See the "PIC32 Flash Programming Specification" (DS60001145) for a list of Revision and Device ID values.

DC CHA	RACTER	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ for Commercial} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions	
D130	Eр	Cell Endurance	20,000	—	_	E/W	—	
D131	Vpr	VDD for Read	2.3	—	3.6	V	—	
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	_	
D134	TRETD	Characteristic Retention	20	_		Year	Provided no other specifications are violated	
D135	IDDP	Supply Current during Programming	—	10	_	mA	_	
D138	Tww	Word Write Cycle Time ⁽⁴⁾	44	—	59	μs	—	
D136	Trw	Row Write Cycle Time ^(2,4)	2.8	3.3	3.8	ms	_	
D137	TPE	Page Erase Cycle Time ⁽⁴⁾	22	_	29	ms		
D139	TCE	Chip Erase Cycle Time ⁽⁴⁾	86	_	116	ms	_	

TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY⁽³⁾

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

- **3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.
- 4: This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

TABLE 31-13:	DC CHARACTERISTICS:	PROGRAM FLASH MEMOR	Y WAIT STATE
--------------	---------------------	----------------------------	--------------

	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)							
DC CHARACTERISTICS	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Required Flash Wait States	SYSCLK	Units	Conditions					
0 Wait State	0-40	MHz	-40°C to +85°C					
	0-30	MHz	-40°C to +105°C					
1 Wait State	41-80	MHz	-40°C to +85°C					
i Wait State	31-60	MHz	-40°C to +105°C					
2 Wait States	81-100	MHz	-40°C to +85°C					
	61-80	MHz	-40°C to +105°C					
3 Wait States	101-120	MHz	0°C to +70°C					





APPENDIX A: REVISION HISTORY

Revision A (July 2012)

This is the initial released version of the document.

Revision B (April 2013)

Note:	The status of this data sheet was updated
	to Preliminary; however, any electrical
	specifications listed for PIC32MX370/470
	devices is to be considered Advance
	Information and is marked accordingly.

This revision includes the following updates, as shown in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section	Update Description			
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/Graphics/Touch (HMI). USB.	SRAM was changed from 32 KB to 64 KB. Data Memory (KB) was changed from 32 to 64 for the following devices (see			
and Advanced Analog"	 PIC32MX350F256H PIC32MX350F256L PIC32MX450F256H PIC32MX450F256L The following devices were added: PIC32MX370F512H PIC32MX370F512L PIC32MX470F512H 			
	 PIC32MX470F512H PIC32MX470F512L 			
4.0 "Memory Organization"	The Memory Map for Devices with 256 KB of Program Memory was update (see Figure 4-3).			
	The Memory Map for Devices with 512 KB of Program Memory was added (see Figure 4-4).			
7.0 "Interrupt Controller"	Updated the Interrupt IRQ, Vector and Bit Locations (see Table 7-1).			
20.0 "Parallel Master Port (PMP)"	Added the CS2 bit and updated the ADDR bits in the Parallel Port Address register (see Register 20-3).			
27.0 "Special Features"	Updated the PWP bit in the Device Configuration Word 3 register (see Register 27-4).			
30.0 "Electrical Characteristics"	Note 2 in the DC Characteristics: Operating Current (IDD) were updated (see Table 30-5).			
	Note 1 in the DC Characteristics: Idle Current (IIDLE) were updated (see Table 30-6).			
	Note 1 in the DC Characteristics: Power-down Current (IPD) were updated (see Table 30-7).			
	Updated Program Memory values for parameters D135 (Tww), D136 (Trw), and D137 (TPE and TCE) (see Table 30-12).			
31.0 "DC and AC Device Characteristics Graphs"	New IDD, IIDLE, and IPD current graphs were added for PIC32MX330/430 devices and PIC32MX350/450 devices.			

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