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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064h-v-rg">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064h-v-rg</a>

# PIC32MX330/350/370/430/450/470

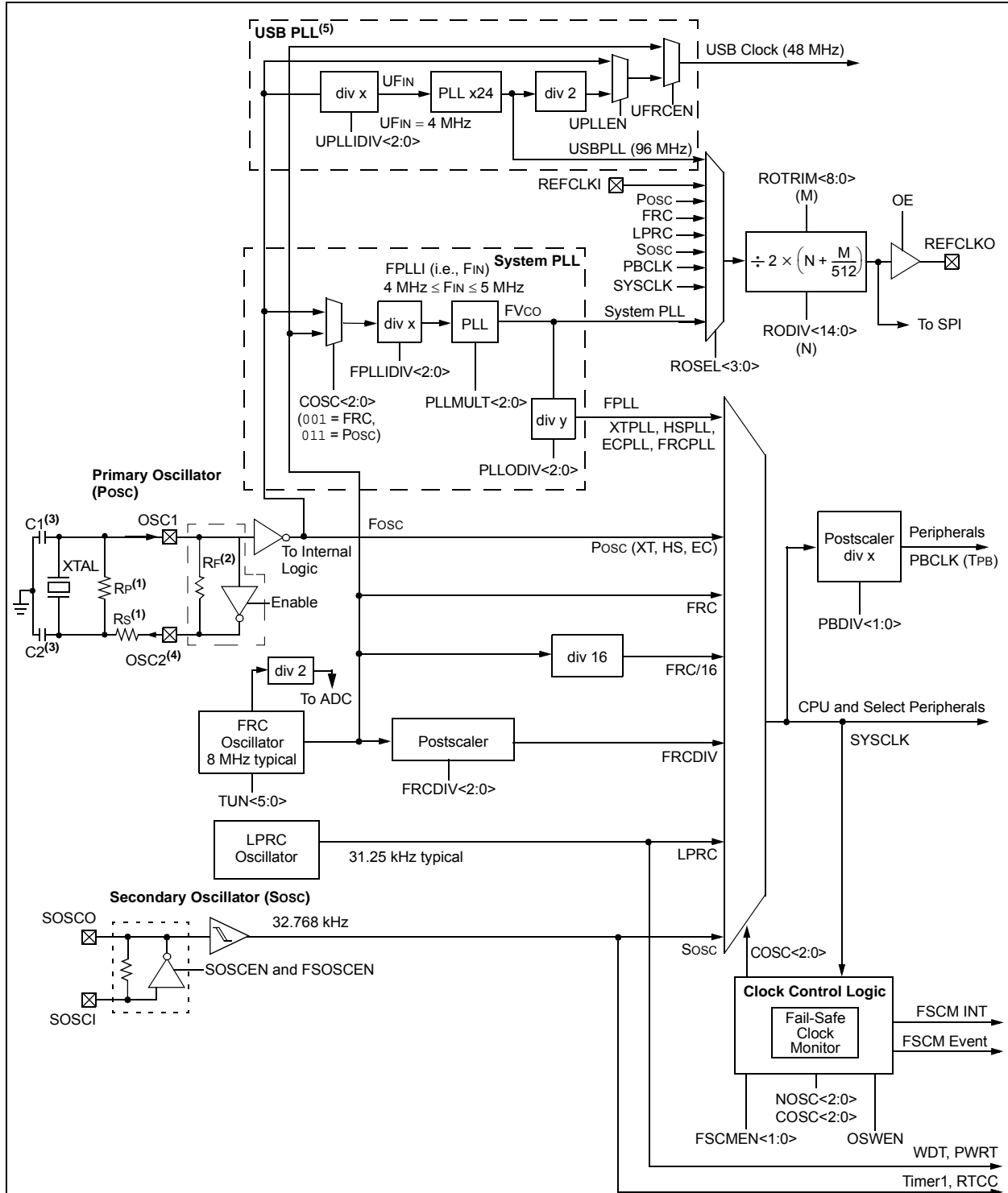
**TABLE 6: PIN NAMES FOR 124-PIN DEVICES**

<b>124-PIN VTLA (BOTTOM VIEW)<sup>(1,2,3,4,5)</sup></b> <div> <div>A17</div> <div>B13B29</div> <div>A34</div> <div>Conductive Thermal Pad</div> <div>B1B56B41</div> <div>A51</div> <div>A1</div> <div>A68</div> <div>Polarity Indicator</div> </div> <b>PIC32MX330F064L</b> <b>PIC32MX350F128L</b> <b>PIC32MX350F256L</b> <b>PIC32MX370F512L</b>			
Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
A1	No Connect	A38	SDA1/RG3
A2	RG15	A39	SCL2/RA2
A3	Vss	A40	TDI/CTED9/RA4
A4	AN23/PMD6/RE6	A41	VDD
A5	RPC1/RC1	A42	OSC2/CLKO/RC15
A6	RPC3/RC3	A43	Vss
A7	AN16/C1IND/RPG6/SCK2/PMA5/RG6	A44	RPA15/RA15
A8	AN18/C2IND/RPG8/PMA3/RG8	A45	RPD9/RD9
A9	AN19/C2INC/RPG9/PMA2/RG9	A46	RPD11/PMCS1/RD11
A10	VDD	A47	SOSCI/IPC13/RC13
A11	RPE8/RE8	A48	VDD
A12	AN5/C1INA/RPB5/RB5	A49	No Connect
A13	PGED3/AN3/C2INA/RPB3/RB3	A50	No Connect
A14	VDD	A51	No Connect
A15	PGEC1/AN1/RPB1/CTED12/RB1	A52	AN24/RPD1/RD1
A16	No Connect	A53	AN26/RPD3/RD3
A17	No Connect	A54	PMD13/RD13
A18	No Connect	A55	RPD5/PMRD/RD5
A19	No Connect	A56	PMD15/RD7
A20	PGEC2/AN6/RPB6/RB6	A57	No Connect
A21	VREF-/CVREF-/PMA7/RA9	A58	No Connect
A22	AVDD	A59	VDD
A23	AN8/RPB8/CTED10/RB8	A60	RPF1/PMD10/RF1
A24	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	A61	RPG0/PMD8/RG0
A25	Vss	A62	TRD3/CTED8/RA7
A26	TCK/CTED2/RA1	A63	Vss
A27	RPF12/RF12	A64	PMD1/RE1
A28	AN13/PMA10/RB13	A65	TRD1/RG12
A29	AN15/RPB15/OCFB/CTED6/PMA0/RB15	A66	AN20/PMD2/RE2
A30	VDD	A67	AN21/PMD4/RE4
A31	RPD15/RD15	A68	No Connect
A32	RPF5/PMA8/RF5	B1	VDD
A33	No Connect	B2	AN22/RPE5/PMD5/RE5
A34	No Connect	B3	AN27/PMD7/RE7
A35	RPF3/RF3	B4	RPC2/RC2
A36	RPF2/RF2	B5	RPC4/CTED7/RC4
A37	RPF7/RF7	B6	AN17/C1INC/RPG7/PMA4/RG7

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RAX-RGX), with the exception of RF6, can be used as a change notification pin (CNAX-CNGX). See **Section 12.0 “I/O Ports”** for more information.
  - 3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.
  - 4: Shaded package bumps are 5V tolerant.
  - 5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

# PIC32MX330/350/370/430/450/470

FIGURE 8-1: PIC32MX330/350/370/430/450/470 FAMILY CLOCK DIAGRAM



- Notes:**
1. A series resistor, R<sub>s</sub>, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, R<sub>p</sub>, with a value of 1 MΩ.
  2. The internal feedback resistor, R<sub>f</sub>, is typically in the range of 2 MΩ to 10 MΩ.
  3. Refer to **Section 6, "Oscillator Configuration"** (DS60001112) in the "PIC32 Family Reference Manual" for help in determining the best oscillator components.
  4. PBCLK out is available on the OSC2 pin in certain clock modes.
  5. USB PLL is available on PIC32MX4XX devices only.

# PIC32MX330/350/370/430/450/470

## REGISTER 9-1: CHECON: CACHE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CHECOH
15:8	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	DCSZ<1:0>	
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
	—	—	PREFEN<1:0>		—	PFMWS<2:0>		

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-17 **Unimplemented:** Write '0'; ignore read

bit 16 **CHECOH:** Cache Coherency Setting on a PFM Program Cycle bit

1 = Invalidate all data and instruction lines

0 = Invalidate all data lines and instruction lines that are not locked

bit 15-10 **Unimplemented:** Write '0'; ignore read

bit 9-8 **DCSZ<1:0>:** Data Cache Size in Lines bits

11 = Enable data caching with a size of 4 Lines

10 = Enable data caching with a size of 2 Lines

01 = Enable data caching with a size of 1 Line

00 = Disable data caching

Changing these bits induce all lines to be reinitialized to the "invalid" state.

bit 7-6 **Unimplemented:** Write '0'; ignore read

bit 5-4 **PREFEN<1:0>:** Predictive Prefetch Enable bits

11 = Enable predictive prefetch for both cacheable and non-cacheable regions

10 = Enable predictive prefetch for non-cacheable regions only

01 = Enable predictive prefetch for cacheable regions only

00 = Disable predictive prefetch

bit 3 **Unimplemented:** Write '0'; ignore read

bit 2-0 **PFMWS<2:0>:** PFM Access Time Defined in Terms of SYSLK Wait States bits

111 = Seven Wait states

110 = Six Wait states

101 = Five Wait states

100 = Four Wait states

011 = Three Wait states

010 = Two Wait states

001 = One Wait state

000 = Zero Wait state

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## REGISTER 9-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEPFABT<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEPFABT<31:0>**: Prefab Abort Count bits

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

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**REGISTER 10-5: DCRCDATA: DMA CRC DATA REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCDATA<7:0>								

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DCRCDATA<31:0>**: CRC Data Register bits

Writing to this register will seed the CRC generator. Reading from this register will return the current value of the CRC. Bits greater than PLEN will return '0' on any read.

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

Only the lower 16 bits contain IP header checksum information. The upper 16 bits are always '0'. Data written to this register is converted and read back in 1's complement form (i.e., current IP header checksum value).

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

Bits greater than PLEN will return '0' on any read.

**REGISTER 10-6: DCRCXOR: DMA CRCXOR ENABLE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<31:24>								
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<23:16>								
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<15:8>								
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DCRCXOR<7:0>								

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **DCRCXOR<31:0>**: CRC XOR Register bits

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):

This register is unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):

1 = Enable the XOR input to the Shift register

0 = Disable the XOR input to the Shift register; data is shifted in directly from the previous stage in the register

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**REGISTER 10-16: DCHxCSIZ: DMA CHANNEL 'x' CELL-SIZE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHCSIZ<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCSIZ<15:0>:** Channel Cell-Size bits

1111111111111111 = 65,535 bytes transferred on an event

.

.

.

0000000000000010 = 2 bytes transferred on an event

0000000000000001 = 1 byte transferred on an event

0000000000000000 = 65,536 bytes transferred on an event

**REGISTER 10-17: DCHxCPTR: DMA CHANNEL 'x' CELL POINTER REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<15:8>							
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	CHCPTR<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHCPTR<7:0>:** Channel Cell Progress Pointer bits

1111111111111111 = 65,535 bytes have been transferred since the last event

.

.

.

0000000000000001 = 1 byte has been transferred since the last event

0000000000000000 = 0 bytes have been transferred since the last event

**Note:** When in Pattern Detect mode, this register is reset on a pattern detect.

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**REGISTER 11-9: U1IE: USB ERROR INTERRUPT ENABLE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
7:0	R/W-0 BTSEE	R/W-0 BMXEE	R/W-0 DMAEE	R/W-0 BTOEE	R/W-0 DFN8EE	R/W-0 CRC16EE	R/W-0 CRC5EE <sup>(1)</sup> EOFEE <sup>(2)</sup>	R/W-0 PIDEE

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **BTSEE:** Bit Stuff Error Interrupt Enable bit

- 1 = BTSEF interrupt is enabled
- 0 = BTSEF interrupt is disabled

bit 6 **BMXEE:** Bus Matrix Error Interrupt Enable bit

- 1 = BMXEF interrupt is enabled
- 0 = BMXEF interrupt is disabled

bit 5 **DMAEE:** DMA Error Interrupt Enable bit

- 1 = DMAEF interrupt is enabled
- 0 = DMAEF interrupt is disabled

bit 4 **BTOEE:** Bus Turnaround Time-out Error Interrupt Enable bit

- 1 = BTOEF interrupt is enabled
- 0 = BTOEF interrupt is disabled

bit 3 **DFN8EE:** Data Field Size Error Interrupt Enable bit

- 1 = DFN8EF interrupt is enabled
- 0 = DFN8EF interrupt is disabled

bit 2 **CRC16EE:** CRC16 Failure Interrupt Enable bit

- 1 = CRC16EF interrupt is enabled
- 0 = CRC16EF interrupt is disabled

bit 1 **CRC5EE:** CRC5 Host Error Interrupt Enable bit<sup>(1)</sup>

- 1 = CRC5EF interrupt is enabled
- 0 = CRC5EF interrupt is disabled

**EOFEE:** EOF Error Interrupt Enable bit<sup>(2)</sup>

- 1 = EOF interrupt is enabled
- 0 = EOF interrupt is disabled

bit 0 **PIDEE:** PID Check Failure Interrupt Enable bit

- 1 = PIDEF interrupt is enabled
- 0 = PIDEF interrupt is disabled

**Note 1:** Device mode.

**2:** Host mode.

**Note:** For an interrupt to propagate USBIF, the UERRIE bit (U1IE<1>) must be set.



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## REGISTER 11-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPDEN:** Low Speed Enable Indicator bit

1 = Next token command to be executed at Low Speed

0 = Next token command to be executed at Full Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

## REGISTER 11-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

## 16.0 INPUT CAPTURE

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 15. “Input Capture”** (DS60001122), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- Simple capture event modes:
  - Capture timer value on every falling edge of input at ICx pin
  - Capture timer value on every rising edge of input at ICx pin
  - Capture timer value on every edge (rising and falling)
  - Capture timer value on every edge (rising and falling), specified edge first.

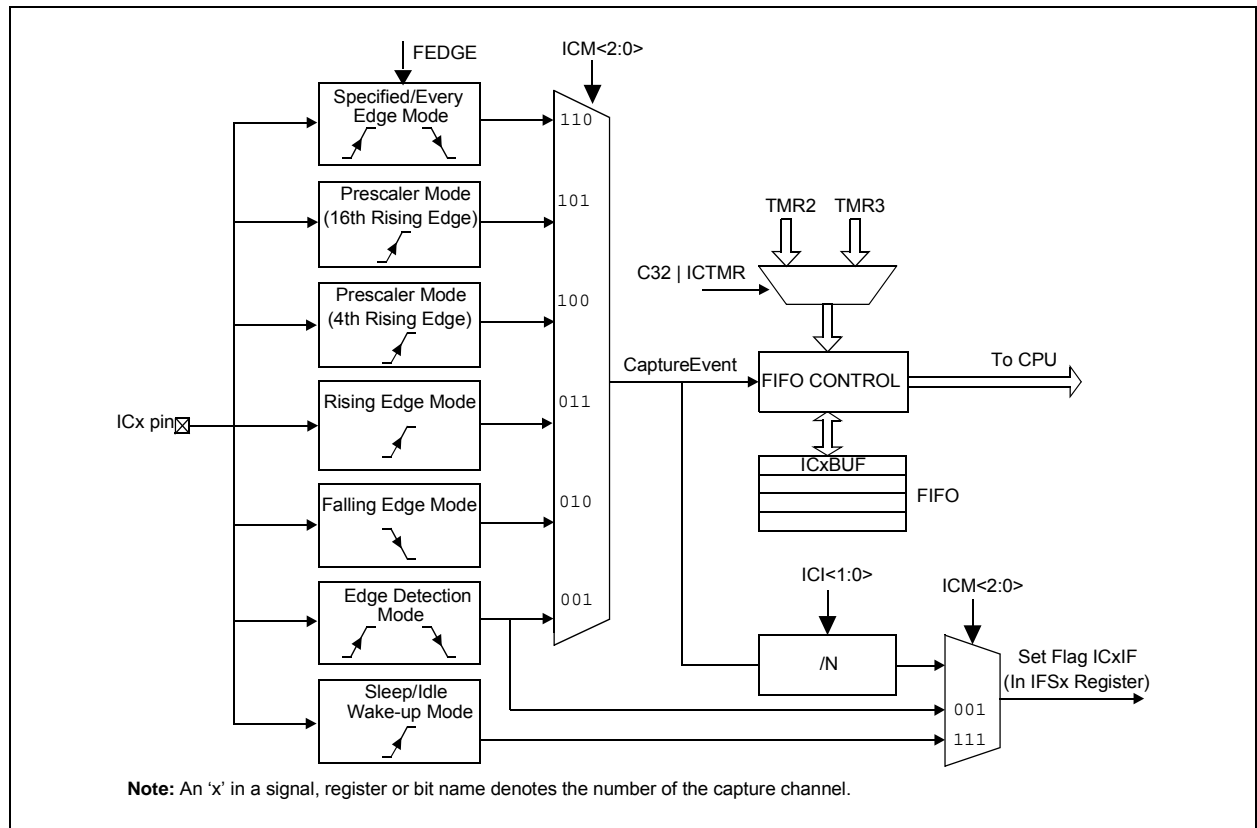
- Prescaler capture event modes:
  - Capture timer value on every 4th rising edge of input at ICx pin
  - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- Device wake-up from capture pin during CPU Sleep and Idle modes
- Interrupt on input capture event
- 4-word FIFO buffer for capture values  
Interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled
- Input capture can also be used to provide additional sources of external interrupts

**FIGURE 16-1: INPUT CAPTURE BLOCK DIAGRAM**



## 19.1 Control Registers

**TABLE 19-1: I2C1 AND I2C2 REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5000	I2C1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5010	I2C1STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
5020	I2C1ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
5030	I2C1MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
5040	I2C1BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5050	I2C1TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Transmit Register									
5060	I2C1RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Receive Register									
5100	I2C2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	BFFF
5110	I2C2STAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
5120	I2C2ADD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Register										0000
5130	I2C2MSK	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	Address Mask Register										0000
5140	I2C2BRG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	Baud Rate Generator Register												0000
5150	I2C2TRN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Transmit Register									
5160	I2C2RCV	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	Receive Register									

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

## REGISTER 19-1: I2CxCON: I<sup>2</sup>C CONTROL REGISTER (CONTINUED)

- bit 7     **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave)  
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)  
0 = General call address disabled
- bit 6     **STREN:** SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave)  
Used in conjunction with SCLREL bit.  
1 = Enable software or receive clock stretching  
0 = Disable software or receive clock stretching
- bit 5     **ACKDT:** Acknowledge Data bit (when operating as I<sup>2</sup>C master, applicable during master receive)  
Value that is transmitted when the software initiates an Acknowledge sequence.  
1 = Send NACK during Acknowledge  
0 = Send ACK during Acknowledge
- bit 4     **ACKEN:** Acknowledge Sequence Enable bit  
(when operating as I<sup>2</sup>C master, applicable during master receive)  
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit.  
Hardware clear at end of master Acknowledge sequence.  
0 = Acknowledge sequence not in progress
- bit 3     **RCEN:** Receive Enable bit (when operating as I<sup>2</sup>C master)  
1 = Enables Receive mode for I<sup>2</sup>C. Hardware clear at end of eighth bit of master receive data byte.  
0 = Receive sequence not in progress
- bit 2     **PEN:** Stop Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.  
0 = Stop condition not in progress
- bit 1     **RSEN:** Repeated Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.  
0 = Repeated Start condition not in progress
- bit 0     **SEN:** Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.  
0 = Start condition not in progress

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## REGISTER 19-2: I2CxSTAT: I<sup>2</sup>C STATUS REGISTER (CONTINUED)

- bit 4     **P:** Stop bit  
1 = Indicates that a Stop bit has been detected last  
0 = Stop bit was not detected last  
Hardware set or clear when Start, Repeated Start or Stop detected.
- bit 3     **S:** Start bit  
1 = Indicates that a Start (or Repeated Start) bit has been detected last  
0 = Start bit was not detected last  
Hardware set or clear when Start, Repeated Start or Stop detected.
- bit 2     **R\_W:** Read/Write Information bit (when operating as I<sup>2</sup>C slave)  
1 = Read – indicates data transfer is output from slave  
0 = Write – indicates data transfer is input to slave  
Hardware set or clear after reception of I<sup>2</sup>C device address byte.
- bit 1     **RBF:** Receive Buffer Full Status bit  
1 = Receive complete, I2CxRCV is full  
0 = Receive not complete, I2CxRCV is empty  
Hardware set when I2CxRCV is written with received byte. Hardware clear when software reads I2CxRCV.
- bit 0     **TBF:** Transmit Buffer Full Status bit  
1 = Transmit in progress, I2CxTRN is full  
0 = Transmit complete, I2CxTRN is empty  
Hardware set when software writes I2CxTRN. Hardware clear at completion of data transmission.

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NOTES:

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**REGISTER 24-1: CMxCON: COMPARATOR CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
	ON <sup>(1)</sup>	COE	CPOL <sup>(2)</sup>	—	—	—	—	COUT
7:0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Comparator ON bit<sup>(1)</sup>

1 = Module is enabled. Setting this bit does not affect the other bits in this register

0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register

bit 14 **COE:** Comparator Output Enable bit

1 = Comparator output is driven on the output CxOUT pin

0 = Comparator output is not driven on the output CxOUT pin

bit 13 **CPOL:** Comparator Output Inversion bit<sup>(2)</sup>

1 = Output is inverted

0 = Output is not inverted

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **COUT:** Comparator Output bit

1 = Output of the Comparator is a '1'

0 = Output of the Comparator is a '0'

bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits

11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output

10 = Comparator interrupt is generated on a high-to-low transition of the comparator output

01 = Comparator interrupt is generated on a low-to-high transition of the comparator output

00 = Comparator interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Positive Input Configure bit

1 = Comparator non-inverting input is connected to the internal CVREF

0 = Comparator non-inverting input is connected to the CxINA pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator Negative Input Select bits for Comparator

11 = Comparator inverting input is connected to the IVREF

10 = Comparator inverting input is connected to the CxIND pin

01 = Comparator inverting input is connected to the CxINC pin

00 = Comparator inverting input is connected to the CxINB pin

**Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

## 25.0 COMPARATOR VOLTAGE REFERENCE (CVREF)

**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

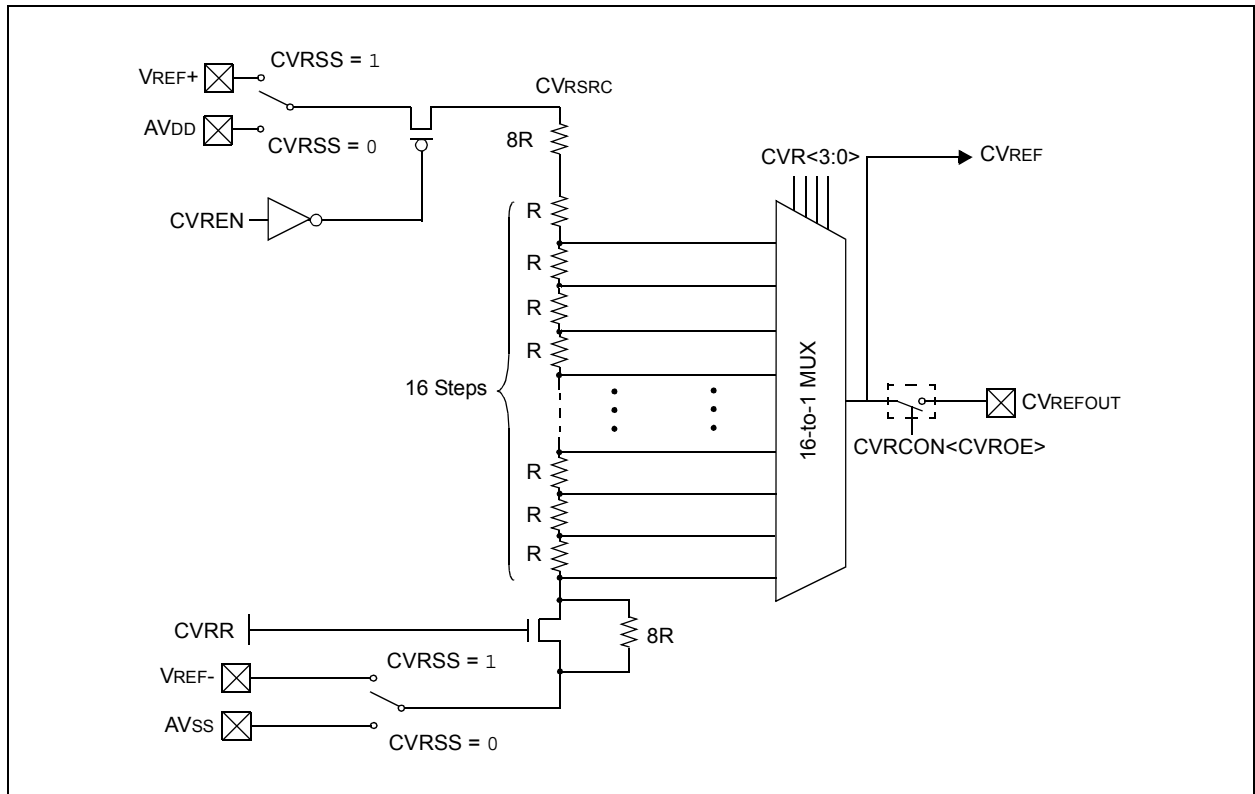
The CVREF module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 25-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not being used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The CVREF output is available for the comparators and typically available for pin output.

The CVREF module has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

**FIGURE 25-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**





# PIC32MX330/350/370/430/450/470

**TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)		
			Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp		
Param. No.	Typ. <sup>(2)</sup>	Max.	Units	Conditions	
PIC32MX370 Devices Only					
Power-Down Current (IPD) (Note 1)					
DC40k	55	95	$\mu\text{A}$	-40°C	Base Power-Down Current
DC40l	81	95	$\mu\text{A}$	+25°C	
DC40n	281	450	$\mu\text{A}$	+85°C	
DC40m	559	895	$\mu\text{A}$	+105°C	
PIC32MX470 Devices Only					
Power-Down Current (IPD) (Note 1)					
DC40k	33	78	$\mu\text{A}$	-40°C	Base Power-Down Current
DC40o	33	78	$\mu\text{A}$	0°C <sup>(5)</sup>	
DC40l	49	78	$\mu\text{A}$	+25°C	
DC40p	281	450	$\mu\text{A}$	+70°C <sup>(5)</sup>	
DC40n	281	450	$\mu\text{A}$	+85°C	
DC40m	559	895	$\mu\text{A}$	+105°C	
PIC32MX330/350/370/430/450/470 Devices					
Module Differential Current					
DC41e	6.7	20	$\mu\text{A}$	3V	Watchdog Timer Current: $\Delta I_{\text{WDT}}$ (Note 3)
DC42e	29.1	50	$\mu\text{A}$	3V	RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{\text{RTCC}}$ (Note 3)
DC43d	1000	1200	$\mu\text{A}$	3V	ADC: $\Delta I_{\text{ADC}}$ (Notes 3,4)

**Note 1:** The test conditions for IPD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
  - OSC2/CLKO is configured as an I/O input pin
  - USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
  - CPU is in Sleep mode, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
  - No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
  - WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
  - All I/O pins are configured as inputs and pulled to Vss
  - MCLR = VDD
  - RTCC and JTAG are disabled
  - Voltage regulator is off during Sleep mode (VREGS bit in the RCON register = 0)
- 2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.
- 4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.
- 5:** 120 MHz commercial devices only (0°C to +70°C).

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**TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp				
Param. No.	Symb.	Characteristics	Min.	Typ. <sup>(1)</sup>	Max.	Units	Conditions
DI60b	I <sub>ICH</sub>	Input High Injection Current	0	—	+5 <sup>(8,9,10)</sup>	mA	Pins with Analog functions. Exceptions: [SOSCI, SOSCO, OSC1, D+, D-] = 0 mA max.
							Digital 5V tolerant designated pins ( $V_{IH} < 5.5\text{V}$ ) <sup>(9)</sup> . Exceptions: [All] = 0 mA max.
							Digital non-5V tolerant designated pins. Exceptions: [N/A] = 0 mA max.
DI60c	$\Sigma I_{ICT}$	Total Input Injection Current (sum of all I/O and control pins)	-20 <sup>(11)</sup>	—	+20 <sup>(11)</sup>	mA	Absolute instantaneous sum of all $\pm$ input injection currents from all I/O pins ( $ I_{ICL}  +  I_{ICH} $ ) $\leq \Sigma I_{ICT}$

- Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** This parameter is characterized, but not tested in manufacturing.
- 5:** See the “**Device Pin Tables**” section for the 5V tolerant pins.
- 6:** The  $V_{IH}$  specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic “high” internally to the PIC32 device, provided that the external load does not exceed the minimum value of  $I_{CNPV}$ . For External “input” logic inputs that require a pull-up source, to guarantee the minimum  $V_{IH}$  of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.
- 7:**  $V_{IL}$  source  $< (V_{SS} - 0.3)$ . Characterized but not tested.
- 8:**  $V_{IH}$  source  $> (V_{DD} + 0.3)$  for non-5V tolerant pins only.
- 9:** Digital 5V tolerant pins do not have an internal high side diode to  $V_{DD}$ , and therefore, cannot tolerate any “positive” input injection current.
- 10:** Injection currents  $> |0|$  can affect the ADC results by approximately 4 to 6 counts (i.e.,  $V_{IH}$  Source  $> (V_{DD} + 0.3)$  or  $V_{IL}$  source  $< (V_{SS} - 0.3)$ ).
- 11:** Any number and/or combination of I/O pins not excluded under  $I_{ICL}$  or  $I_{ICH}$  conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**,  $I_{ICL} = ((V_{SS} - 0.3) - V_{IL} \text{ source}) / R_S$ . If **Note 8**,  $I_{ICH} = (I_{ICH} \text{ source} - (V_{DD} + 0.3)) / R_S$ .  $R_S$  = Resistance between input source voltage and device pin. If  $(V_{SS} - 0.3) \leq V_{SOURCE} \leq (V_{DD} + 0.3)$ , injection current = 0.

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**TABLE 31-32: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Typical <sup>(2)</sup>	Max.	Units	Conditions
SP50	TssL2sch, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—
SP51	TssH2boZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance (Note 4)	5	—	25	ns	—
SP52	Tsch2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2boV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

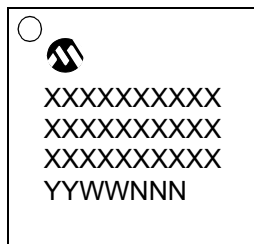
**3:** The minimum clock period for SCKx is 40 ns.

**4:** Assumes 50 pF load on all SPIx pins.

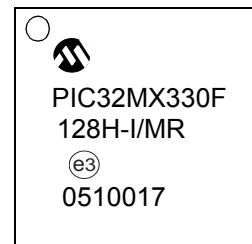
# PIC32MX330/350/370/430/450/470

## 33.1 Package Marking Information (Continued)

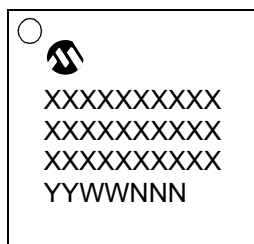
64-Lead QFN (9x9x0.9 mm) with 5.40x5.40 Exposed Pad



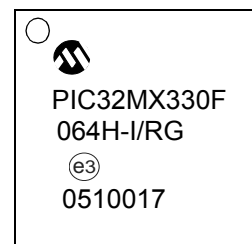
Example



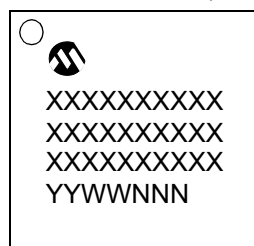
64-Lead QFN (9x9x0.9 mm) with 4.7x4.7 Exposed Pad



Example



124-Lead VTLA (9x9x0.9 mm)



Example



<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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NOTES: