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Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064ht-v-rg

PIC32MX330/350/370/430/450/470

2.11 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-6, Figure 2-7, and Figure 2-8.

FIGURE 2-6: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

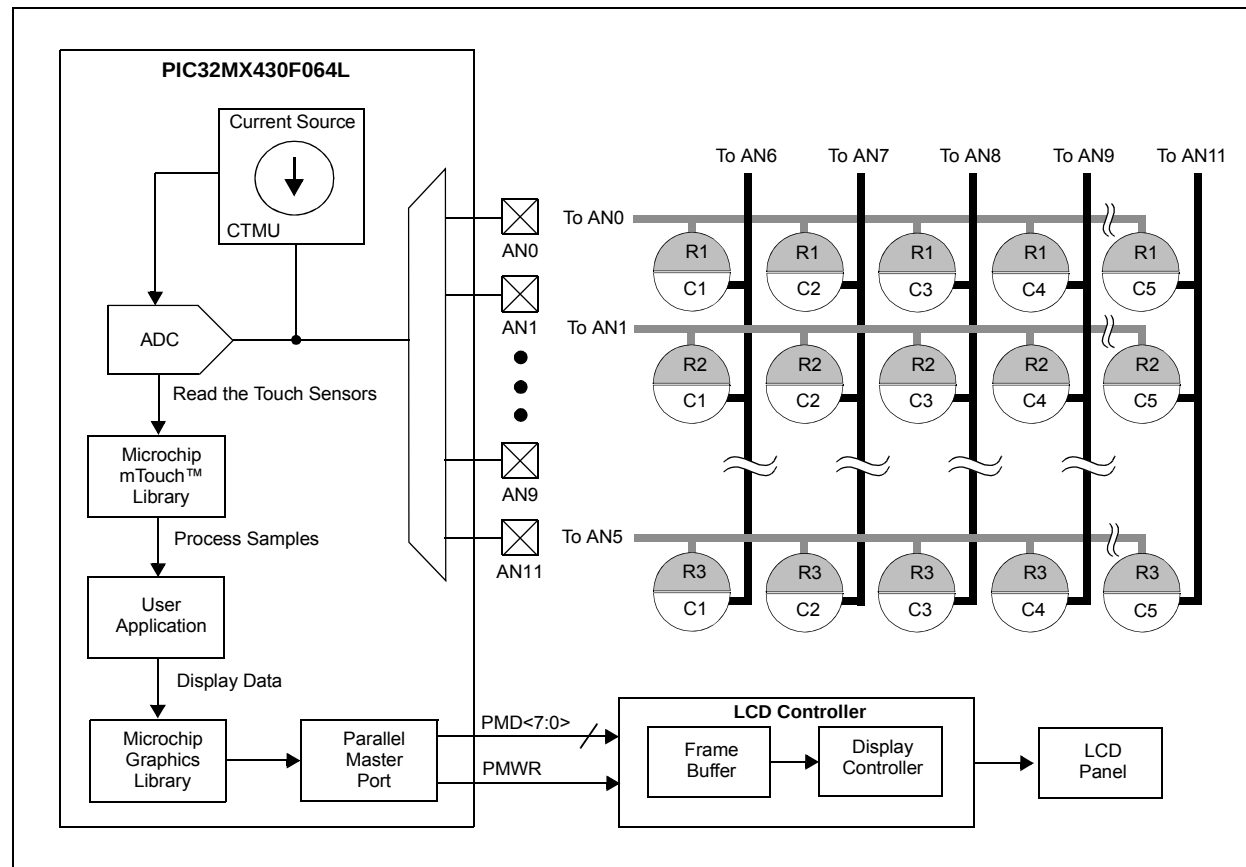
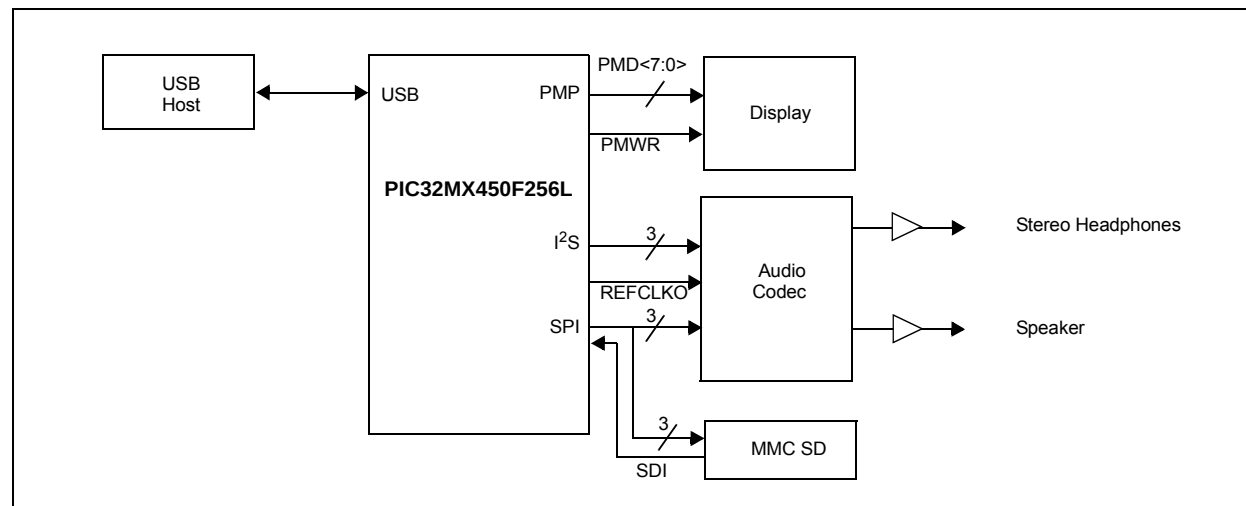


FIGURE 2-7: AUDIO PLAYBACK APPLICATION



PIC32MX330/350/370/430/450/470

REGISTER 9-4: CHEMSK: CACHE TAG MASK REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LMASK<10:3>							
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	LMASK<2:0>			—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Write '0'; ignore read

bit 15-5 **LMASK<10:0>:** Line Mask bits

1 = Enables mask logic to force a match on the corresponding bit position in the LTAG<19:0> bits (CHETAG<23:4>) and the physical address.

0 = Only writeable for values of CHEIDX<3:0> bits (CHEACC<3:0>) equal to 0x0A and 0x0B. Disables mask logic.

bit 4-0 **Unimplemented:** Write '0'; ignore read

REGISTER 9-5: CHEW0: CACHE WORD 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW0<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEW0<31:0>:** Word 0 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>)

Readable only if the device is not code-protected.

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REGISTER 9-6: CHEW1: CACHE WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW1<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEW1<31:0>**: Word 1 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>)
 Readable only if the device is not code-protected.

REGISTER 9-7: CHEW2: CACHE WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<31:24>							
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<23:16>							
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<15:8>							
7:0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	CHEW2<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-0 **CHEW2<31:0>**: Word 2 of the cache line selected by the CHEIDX<3:0> bits (CHEACC<3:0>)
 Readable only if the device is not code-protected.

10.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

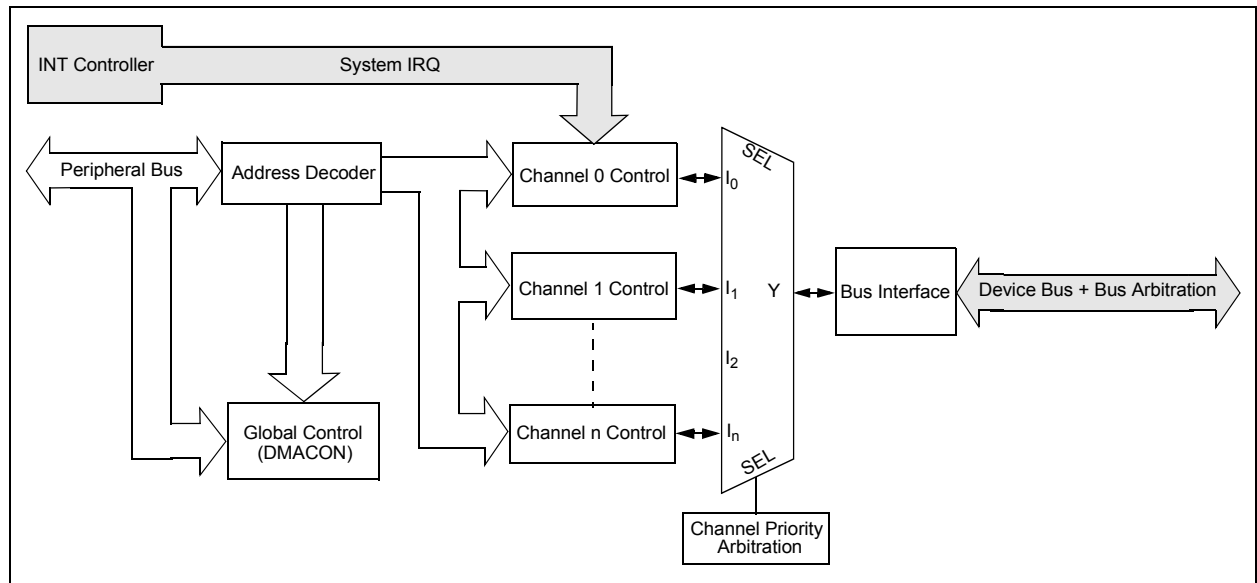
The PIC32 Direct Memory Access (DMA) controller is a bus master module useful for data transfers between different devices without CPU intervention. The source and destination of a DMA transfer can be any of the memory mapped modules existent in the PIC32 (such as Peripheral Bus (PBUS) devices: SPI, UART, PMP, etc.) or memory itself.

Following are some of the key features of the DMA controller module:

- Four identical channels, each featuring:
 - Auto-increment source and destination address registers
 - Source and destination pointers
 - Memory to memory and memory to peripheral transfers
- Automatic word-size detection:
 - Transfer granularity, down to byte level
 - Bytes need not be word-aligned at source and destination

- Fixed priority channel arbitration
- Flexible DMA channel operating modes:
 - Manual (software) or automatic (interrupt) DMA requests
 - One-Shot or Auto-Repeat Block Transfer modes
 - Channel-to-channel chaining
- Flexible DMA requests:
 - A DMA request can be selected from any of the peripheral interrupt sources
 - Each channel can select any (appropriate) observable interrupt as its DMA request source
 - A DMA transfer abort can be selected from any of the peripheral interrupt sources
 - Pattern (data) match transfer termination
- Multiple DMA channel status interrupts:
 - DMA channel block transfer complete
 - Source empty or half empty
 - Destination full or half full
 - DMA transfer aborted due to an external event
 - Invalid DMA address generated
- DMA debug support features:
 - Most recent address accessed by a DMA channel
 - Most recent DMA channel to transfer data
- CRC Generation module:
 - CRC module can be assigned to any of the available channels
 - CRC module is highly configurable

FIGURE 10-1: DMA BLOCK DIAGRAM



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REGISTER 10-8: DCHxECON: DMA CHANNEL 'x' EVENT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHAIRQ<7:0> ⁽¹⁾							
15:8	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	CHSIRQ<7:0> ⁽¹⁾							
7:0	S-0 CFORCE	S-0 CABORT	R/W-0 PATEN	R/W-0 SIRQEN	R/W-0 AIRQEN	U-0 —	U-0 —	U-0 —

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	U = Unimplemented bit, read as '0'
	'0' = Bit is cleared
	x = Bit is unknown

bit 31-24 **Unimplemented:** Read as '0'

bit 23-16 **CHAIRQ<7:0>:** Channel Transfer Abort IRQ bits⁽¹⁾

11111111 = Interrupt 255 will abort any transfers in progress and set CHAIF flag

•
•
•

00000001 = Interrupt 1 will abort any transfers in progress and set CHAIF flag

00000000 = Interrupt 0 will abort any transfers in progress and set CHAIF flag

bit 15-8 **CHSIRQ<7:0>:** Channel Transfer Start IRQ bits⁽¹⁾

11111111 = Interrupt 255 will initiate a DMA transfer

•
•
•

00000001 = Interrupt 1 will initiate a DMA transfer

00000000 = Interrupt 0 will initiate a DMA transfer

bit 7 **CFORCE:** DMA Forced Transfer bit

1 = A DMA transfer is forced to begin when this bit is written to a '1'

0 = This bit always reads '0'

bit 6 **CABORT:** DMA Abort Transfer bit

1 = A DMA transfer is aborted when this bit is written to a '1'

0 = This bit always reads '0'

bit 5 **PATEN:** Channel Pattern Match Abort Enable bit

1 = Abort transfer and clear CHEN on pattern match

0 = Pattern match is disabled

bit 4 **SIRQEN:** Channel Start IRQ Enable bit

1 = Start channel cell transfer if an interrupt matching CHSIRQ occurs

0 = Interrupt number CHSIRQ is ignored and does not start a transfer

bit 3 **AIRQEN:** Channel Abort IRQ Enable bit

1 = Channel transfer is aborted if an interrupt matching CHAIRQ occurs

0 = Interrupt number CHAIRQ is ignored and does not terminate a transfer

bit 2-0 **Unimplemented:** Read as '0'

Note 1: See Table 7-1: "Interrupt IRQ, Vector and Bit Location" for the list of available interrupt IRQ sources.

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REGISTER 11-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVIE	SESENDIE	—	VBUSVDIE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit

1 = ID interrupt is enabled

0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit

1 = 1 millisecond timer interrupt is enabled

0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit

1 = Line state interrupt is enabled

0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit

1 = ACTIVITY interrupt is enabled

0 = ACTIVITY interrupt is disabled

bit 3 **SESVIE:** Session Valid Interrupt Enable bit

1 = Session valid interrupt is enabled

0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit

1 = B-session end interrupt is enabled

0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit

1 = A-VBUS valid interrupt is enabled

0 = A-VBUS valid interrupt is disabled

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REGISTER 21-2: PMMODE: PARALLEL PORT MODE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R-0 BUSY	R/W-0 IRQM<1:0>	R/W-0 IRQM<1:0>	R/W-0 INCM<1:0>	R/W-0 INCM<1:0>	R/W-0 MODE16	R/W-0 MODE<1:0>	R/W-0 MODE<1:0>
7:0	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITB<1:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITM<3:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾	R/W-0 WAITE<1:0> ⁽¹⁾

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **BUSY:** Busy bit (Master mode only)

1 = Port is busy

0 = Port is not busy

bit 14-13 **IRQM<1:0>:** Interrupt Request Mode bits

11 = Reserved, do not use

10 = Interrupt generated when Read Buffer 3 is read or Write Buffer 3 is written (Buffered PSP mode) or on a read or write operation when PMA<1:0> = 11 (Addressable Slave mode only)

01 = Interrupt generated at the end of the read/write cycle

00 = No Interrupt generated

bit 12-11 **INCM<1:0>:** Increment Mode bits

11 = Slave mode read and write buffers auto-increment (MODE<1:0> = 00 only)

10 = Decrement ADDR<15:0> by 1 every read/write cycle⁽²⁾

01 = Increment ADDR<15:0> by 1 every read/write cycle⁽²⁾

00 = No increment or decrement of address

bit 10 **MODE16:** 8/16-bit Mode bit

1 = 16-bit mode: a read or write to the data register invokes a single 16-bit transfer

0 = 8-bit mode: a read or write to the data register invokes a single 8-bit transfer

bit 9-8 **MODE<1:0>:** Parallel Port Mode Select bits

11 = Master mode 1 (PMCSx, PMRD/PMWR, PMENB, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)

10 = Master mode 2 (PMCSx, PMRD, PMWR, PMA<x:0>, PMD<7:0> and PMD<8:15>⁽³⁾)

01 = Enhanced Slave mode, control signals (PMRD, PMWR, PMCS, PMD<7:0> and PMA<1:0>)

00 = Legacy Parallel Slave Port, control signals (PMRD, PMWR, PMCS and PMD<7:0>)

bit 7-6 **WAITB<1:0>:** Data Setup to Read/Write Strobe Wait States bits⁽¹⁾

11 = Data wait of 4 TPB; multiplexed address phase of 4 TPB

10 = Data wait of 3 TPB; multiplexed address phase of 3 TPB

01 = Data wait of 2 TPB; multiplexed address phase of 2 TPB

00 = Data wait of 1 TPB; multiplexed address phase of 1 TPB (default)

Note 1: Whenever WAITM<3:0> = 0000, WAITB and WAITE bits are ignored and forced to 1 TPB cycle for a write operation; WAITB = 1 TPB cycle, WAITE = 0 TPB cycles for a read operation.

2: Address bits, A15 and A14, are not subject to automatic increment/decrement if configured as Chip Select CS2 and CS1.

3: These pins are active when MODE16 = 1 (16-bit mode).

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REGISTER 22-3: RTCTIME: RTC TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	HR10<3:0>				HR01<3:0>			
23:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	MIN10<3:0>				MIN01<3:0>			
15:8	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	SEC10<3:0>				SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **HR10<3:0>**: Binary-Coded Decimal Value of Hours bits, 10s place digits; contains a value from 0 to 2

bit 27-24 **HR01<3:0>**: Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9

bit 23-20 **MIN10<3:0>**: Binary-Coded Decimal Value of Minutes bits, 10s place digits; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>**: Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **SEC10<3:0>**: Binary-Coded Decimal Value of Seconds bits, 10s place digits; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>**: Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented**: Read as '0'

Note: This register is only writable when RTCWREN = 1 (RTCCON<3>).

23.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

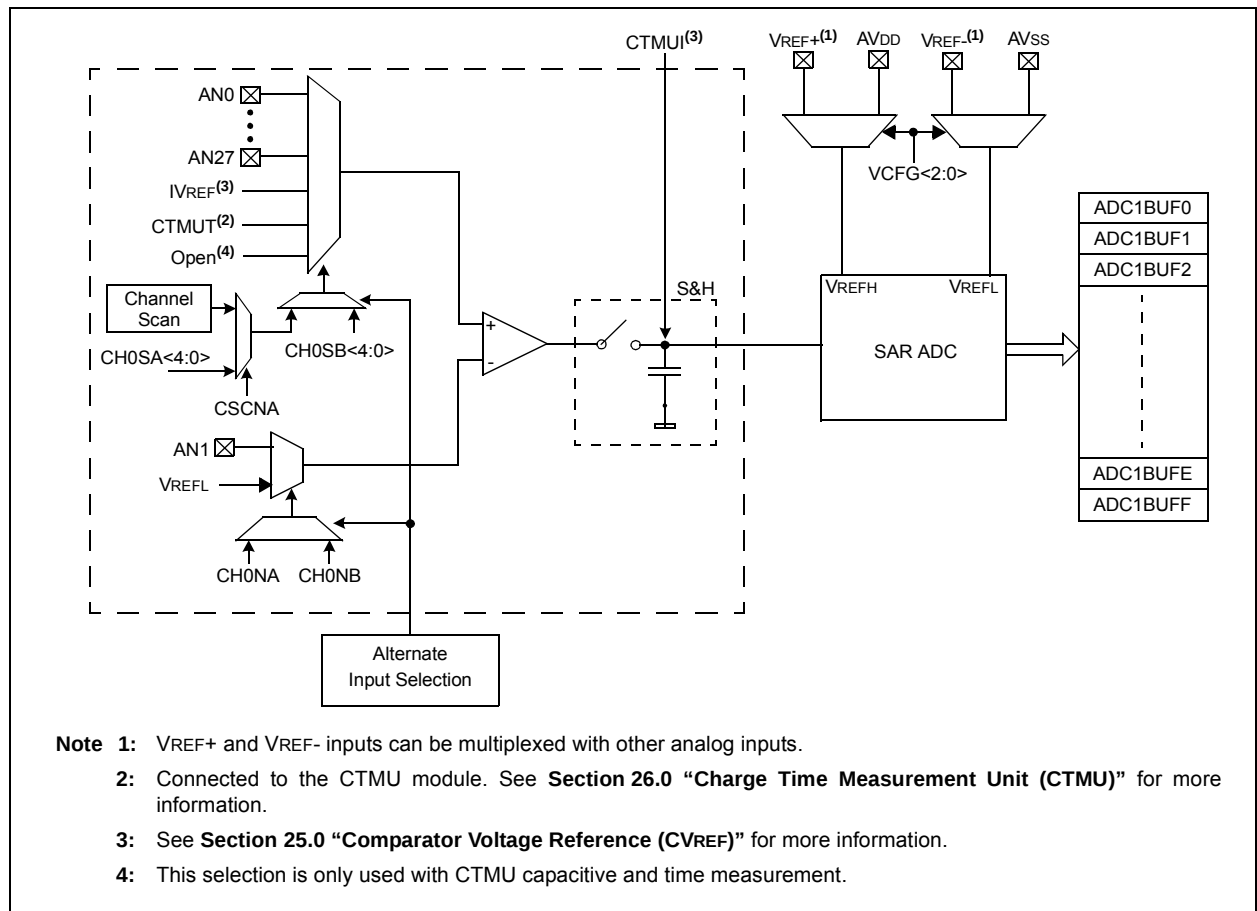
Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 28 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 23-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

FIGURE 23-1: ADC1 MODULE BLOCK DIAGRAM



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REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
	VCFG<2:0>			OFFCAL	—	CSCNA	—	—
7:0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	BUFS	—	SMPI<3:0>				BUFM	ALTS

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

	VREFH	VREFL
000	AVDD	AVss
001	External VREF+ pin	AVss
010	AVDD	External VREF- pin
011	External VREF+ pin	External VREF- pin
1XX	AVDD	AVss

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scan inputs

0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence

.

.

.

0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence

0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADC1BUF8

0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples

0 = Always use Sample A input multiplexer settings

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REGISTER 28-2: DEVCFG1: DEVICE CONFIGURATION WORD 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	r-1	r-1	r-1	r-1	r-1	R/P	R/P
	—	—	—	—	—	—	FWDTWINSZ<1:0>	
23:16	R/P	R/P	r-1	R/P	R/P	R/P	R/P	R/P
	FWDTEN	WINDIS	—	WDTPS<4:0>				
15:8	R/P	R/P	R/P	R/P	r-1	R/P	R/P	R/P
	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>	
7:0	R/P	r-1	R/P	r-1	r-1	R/P	R/P	R/P
	IESO	—	FSOSCEN	—	—	FNOSC<2:0>		

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-26 **Reserved:** Write '1'

bit 25-24 **FWDTWINSZ<1:0>**: Watchdog Timer Window Size bits

11 = Window size is 25%
 10 = Window size is 37.5%
 01 = Window size is 50%
 00 = Window size is 75%

bit 23 **FWDTEN**: Watchdog Timer Enable bit

1 = Watchdog Timer is enabled and cannot be disabled by software
 0 = Watchdog Timer is not enabled; it can be enabled in software

bit 22 **WINDIS**: Watchdog Timer Window Enable bit

1 = Watchdog Timer is in non-Window mode
 0 = Watchdog Timer is in Window mode

bit 21 **Reserved:** Write '1'

bit 20-16 **WDTPS<4:0>**: Watchdog Timer Postscale Select bits

10100 = 1:1048576
 10011 = 1:524288
 10010 = 1:262144
 10001 = 1:131072
 10000 = 1:65536
 01111 = 1:32768
 01110 = 1:16384
 01101 = 1:8192
 01100 = 1:4096
 01011 = 1:2048
 01010 = 1:1024
 01001 = 1:512
 01000 = 1:256
 00111 = 1:128
 00110 = 1:64
 00101 = 1:32
 00100 = 1:16
 00011 = 1:8
 00010 = 1:4
 00001 = 1:2
 00000 = 1:1

All other combinations not shown result in operation = 10100

Note 1: Do not disable the Posc (POSCMOD = 11) when using this oscillator source.

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REGISTER 28-3: DEVCFG2: DEVICE CONFIGURATION WORD 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLIDIV<2:0>	R/P	R/P
15:8	R/P UPLLEN ⁽¹⁾	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLLDIV<2:0> ⁽¹⁾	R/P	R/P
7:0	r-1 —	R/P-1 FPLLMUL<2:0>	R/P	R/P-1	r-1 —	R/P FPLLDIV<2:0>	R/P	R/P

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLIDIV<2:0>:** Default PLL Output Divisor bits

111 = PLL output divided by 256
 110 = PLL output divided by 64
 101 = PLL output divided by 32
 100 = PLL output divided by 16
 011 = PLL output divided by 8
 010 = PLL output divided by 4
 001 = PLL output divided by 2
 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit⁽¹⁾
 1 = Disable and bypass USB PLL
 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** USB PLL Input Divider bits⁽¹⁾

111 = 12x divider
 110 = 10x divider
 101 = 6x divider
 100 = 5x divider
 011 = 4x divider
 010 = 3x divider
 001 = 2x divider
 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

111 = 24x multiplier
 110 = 21x multiplier
 101 = 20x multiplier
 100 = 19x multiplier
 011 = 18x multiplier
 010 = 17x multiplier
 001 = 16x multiplier
 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

Note 1: This bit is available on PIC32MX4XX devices only.

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TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY⁽³⁾

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
D138	TWW	Word Write Cycle Time ⁽⁴⁾	44	—	59	μs	—
D136	TRW	Row Write Cycle Time ^(2,4)	2.8	3.3	3.8	ms	—
D137	TPE	Page Erase Cycle Time ⁽⁴⁾	22	—	29	ms	—
D139	TCE	Chip Erase Cycle Time ⁽⁴⁾	86	—	116	ms	—

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

- 2:** The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).
- 3:** Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.
- 4:** This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

TABLE 31-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATE

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp	
Required Flash Wait States	SYSCLK	Units	Conditions
0 Wait State	0-40	MHz	-40°C to +85°C
	0-30	MHz	-40°C to +105°C
1 Wait State	41-80	MHz	-40°C to +85°C
	31-60	MHz	-40°C to +105°C
2 Wait States	81-100	MHz	-40°C to +85°C
	61-80	MHz	-40°C to +105°C
3 Wait States	101-120	MHz	0°C to +70°C

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FIGURE 31-10: SPIx MODULE MASTER MODE (CKE = 0) TIMING CHARACTERISTICS

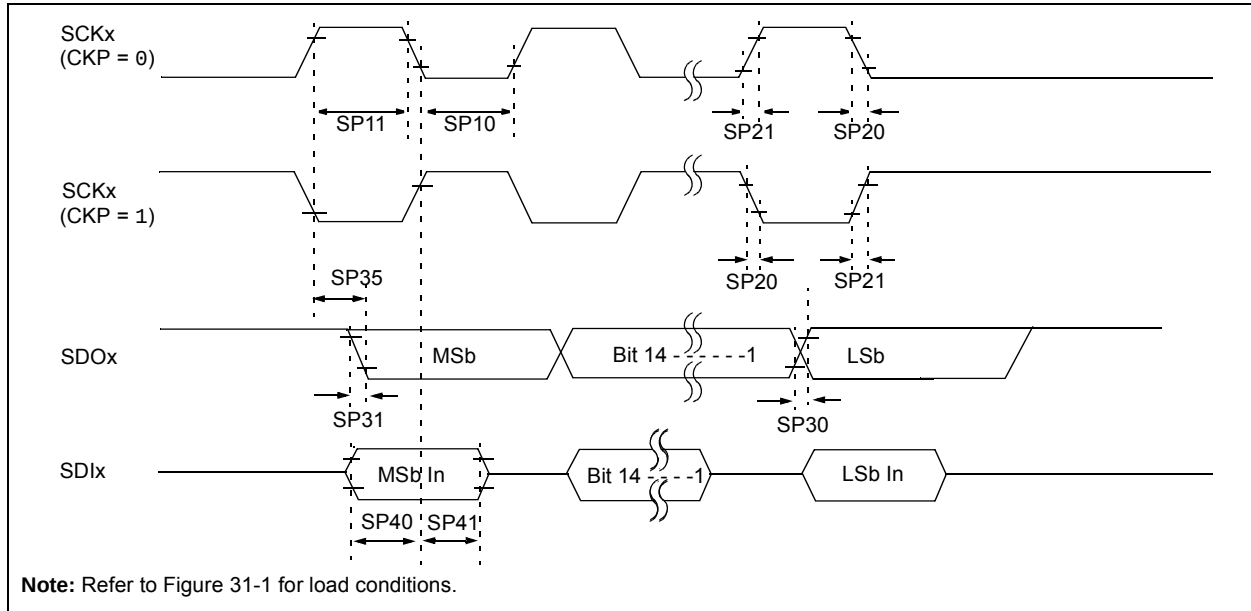


TABLE 31-29: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	T _{SCK} /2	—	—	ns	—
SP11	TscH	SCKx Output High Time (Note 3)	T _{SCK} /2	—	—	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time (Note 4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time (Note 4)	—	—	—	ns	See parameter DO31
SP35	Tsch2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	V _{DD} > 2.7V
			—	—	20	ns	V _{DD} < 2.7V
SP40	TdiV2sch, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—
SP41	Tsch2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	10	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

Note 2: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Note 3: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

Note 4: Assumes 50 pF load on all SPIx pins.

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TABLE 31-35: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS ⁽⁵⁾			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module Vss Supply	Vss	—	Vss + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	(Note 1)
AD05a			2.5	—	3.6	V	VREFH = AVDD (Note 3)
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	(Note 1)
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	(Note 3)
AD08	IREF	Current Drain	—	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15		Leakage Current	—	+/- 0.001	+/-0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	(Note 1)
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	E _{OFF}	Offset Error	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for VBORMIN values.

PIC32MX330/350/370/430/450/470

FIGURE 31-20: PARALLEL SLAVE PORT TIMING

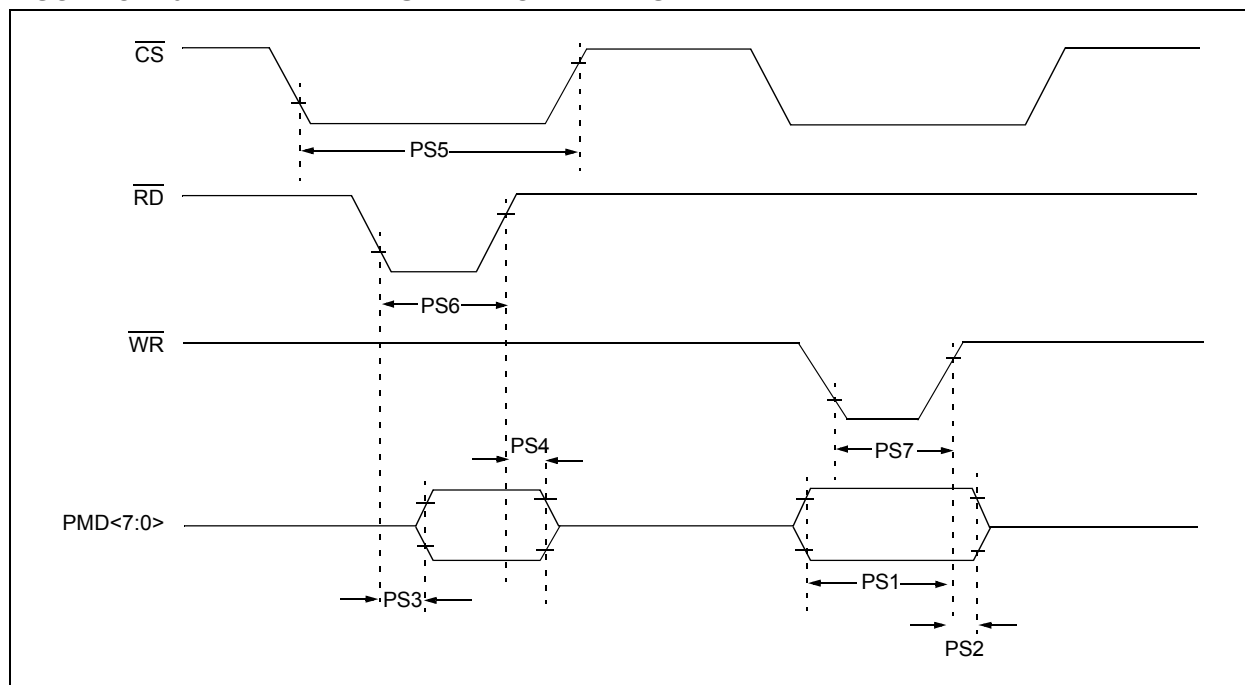


TABLE 31-38: PARALLEL SLAVE PORT REQUIREMENTS

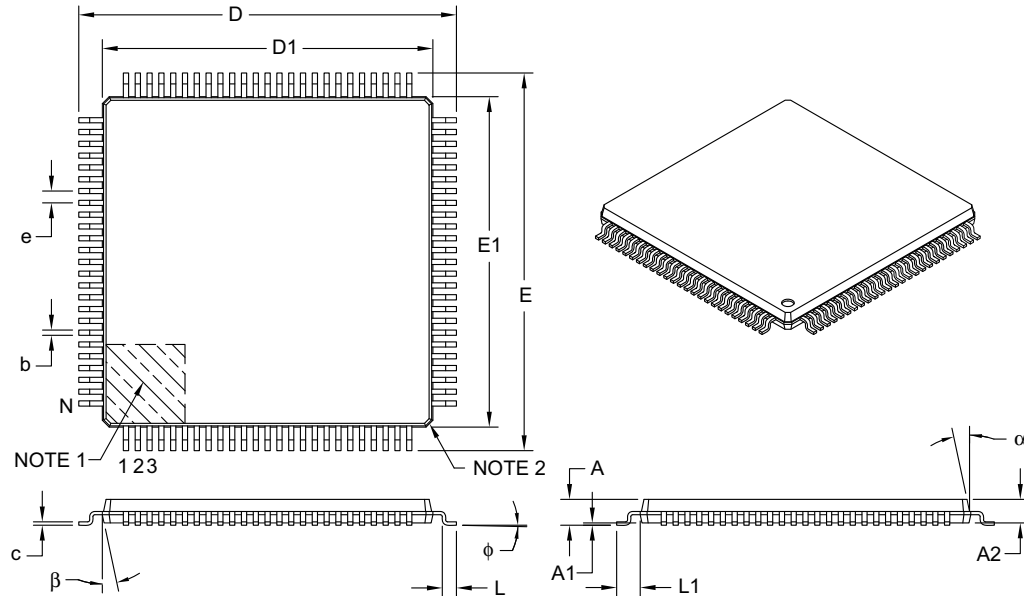
AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)			
				Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Para m.No.	Symbol	Characteristics ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
PS1	TdtV2wr H	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dt I	$\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dt V	$\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX330/350/370/430/450/470

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	100		
Lead Pitch	e	0.50 BSC		
Overall Height	A	—	—	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	—	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	16.00 BSC		
Overall Length	D	16.00 BSC		
Molded Package Width	E1	14.00 BSC		
Molded Package Length	D1	14.00 BSC		
Lead Thickness	c	0.09	—	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

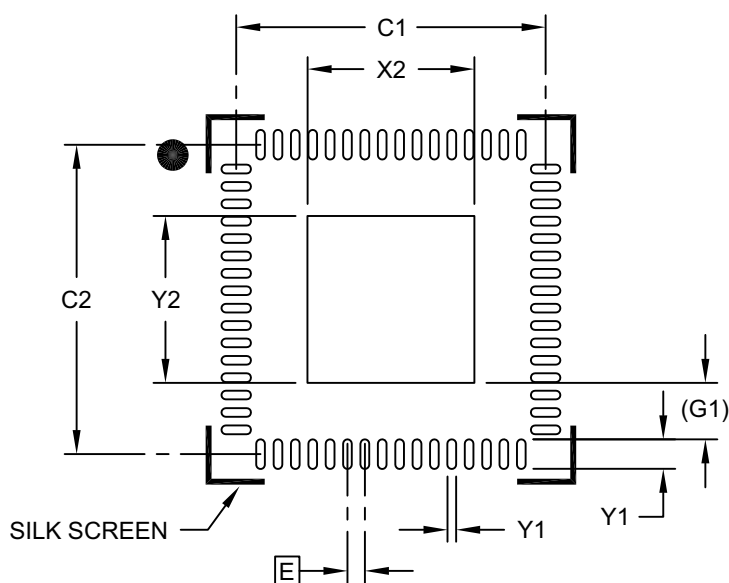
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

PIC32MX330/350/370/430/450/470

64-Lead Very Thin Plastic Quad Flat, No Lead Package (RG) - 9x9x1.0 mm Body [QFN] 4.7x4.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			4.80
Optional Center Pad Length	Y2			4.80
Contact Pad Spacing	C1		8.90	
Contact Pad Spacing	C2		8.90	
Contact Pad Width (X64)	X1			0.25
Contact Pad Length (X64)	Y1			0.85
Contact Pad to Center Pad (X64)	G1	1.625 REF		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2260A

PIC32MX330/350/370/430/450/470

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