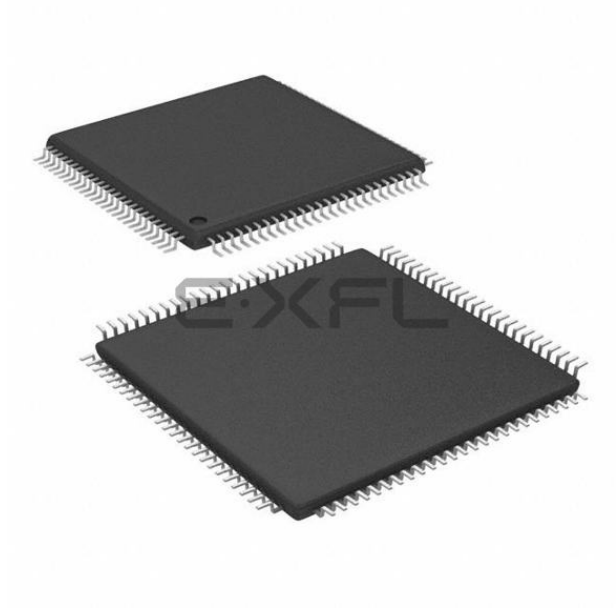

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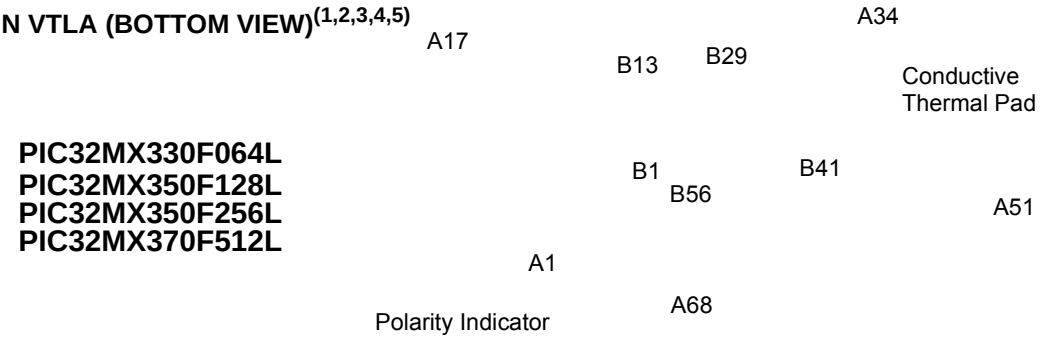
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064l-i-pf

TABLE 6: PIN NAMES FOR 124-PIN DEVICES (CONTINUED)

124-PIN VTLA (BOTTOM VIEW)(1,2,3,4,5)



Package Bump #	Full Pin Name	Package Bump #	Full Pin Name
B7	$\overline{MCLR}$	B32	SDA2/RA3
B8	VSS	B33	TDO/RA5
B9	TMS/CTED1/RA0	B34	OSC1/CLKI/RC12
B10	RPE9/RE9	B35	No Connect
B11	AN4/C1INB/RB4	B36	RPA14/RA14
B12	VSS	B37	RPD8/RTCC/RD8
B13	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	B38	RPD10/PMCS2/RD10
B14	PGED1/AN0/RPB0/RB0	B39	RPD0/RD0
B15	No Connect	B40	SOSCO/RPC14/T1CK/RC14
B16	PGED2/AN7/RPB7/CTED3/RB7	B41	VSS
B17	VREF+/CVREF+/PMA6/RA10	B42	AN25/RPD2/RD2
B18	AVSS	B43	RPD12/PMD12/RD12
B19	AN9/RPB9/CTED4/RB9	B44	RPD4/PMWR/RD4
B20	AN11/PMA12/RB11	B45	PMD14/RD6
B21	VDD	B46	No Connect
B22	RPF13/RF13	B47	No Connect
B23	AN12/PMA11/RB12	B48	VCAP
B24	AN14/RPB14/CTED5/PMA1/RB14	B49	RPF0/PMD11/RF0
B25	VSS	B50	RPG1/PMD9/RG1
B26	RPD14/RD14	B51	TRCLK/RA6
B27	RPF4/PMA9/RF4	B52	PMD0/RE0
B28	No Connect	B53	VDD
B29	RPF8/RF8	B54	TRD2/RG14
B30	RPF6/SCKI/INT0/RF6	B55	TRD0/RG13
B31	SCL1/RG2	B56	RPE3/CTPLS/PMD3/RE3

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RGx), with the exception of RF6, can be used as a change notification pin (CNAx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

3: RPF6 (bump B30) and RPF7 (bump A37) are only remappable for input functions.

4: Shaded package bumps are 5V tolerant.

5: It is recommended that the user connect the printed circuit board (PCB) ground to the conductive thermal pad on the bottom of the package. And to not run non-Vss PCB traces under the conductive thermal pad on the same side of the PCB layout.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA			
U1CTS	PPS	PPS	PPS	I	ST	UART1 Clear to Send
U1RTS	PPS	PPS	PPS	O	—	UART1 Ready to Send
U1RX	PPS	PPS	PPS	I	ST	UART1 Receive
U1TX	PPS	PPS	PPS	O	—	UART1 Transmit
U2CTS	PPS	PPS	PPS	I	ST	UART2 Clear to Send
U2RTS	PPS	PPS	PPS	O	—	UART2 Ready to Send
U2RX	PPS	PPS	PPS	I	ST	UART2 Receive
U2TX	PPS	PPS	PPS	O	—	UART2 Transmit
U3CTS	PPS	PPS	PPS	I	ST	UART3 Clear to Send
U3RTS	PPS	PPS	PPS	O	—	UART3 Ready to Send
U3RX	PPS	PPS	PPS	I	ST	UART3 Receive
U3TX	PPS	PPS	PPS	O	—	UART3 Transmit
U4CTS	PPS	PPS	PPS	I	ST	UART4 Clear to Send
U4RTS	PPS	PPS	PPS	O	—	UART4 Ready to Send
U4RX	PPS	PPS	PPS	I	ST	UART4 Receive
U4TX	PPS	PPS	PPS	O	—	UART4 Transmit
U5CTS(3)	—	PPS	PPS	I	ST	UART5 Clear to Send
U5RTS(3)	—	PPS	PPS	O	—	UART5 Ready to Send
U5RX(3)	—	PPS	PPS	I	ST	UART5 Receive
U5TX(3)	—	PPS	PPS	O	—	UART5 Transmit
SCK1	35(1), 50(2)	55(1), 70(2)	B30(1), B38(2)	I/O	ST	Synchronous Serial Clock Input/Output for SPI1
SDI1	PPS	PPS	PPS	O	—	SPI1 Data In
SDO1	PPS	PPS	PPS	I/O	ST	SPI1 Data Out
SS1	PPS	PPS	PPS	I/O	—	SPI1 Slave Synchronization for Frame Pulse I/O
SCK2	4	10	A7	I/O	ST	Synchronous Serial Clock Input/Output for SPI2
SDI2	PPS	PPS	PPS	O	—	SPI2 Data In
SDO2	PPS	PPS	PPS	I/O	ST	SPI2 Data Out
SS2	PPS	PPS	PPS	I/O	—	SPI2 Slave Synchronization for Frame Pulse I/O
SCL1	37(1), 44(2)	57(1), 66(2)	B31(1), B36(2)	I/O	ST	Synchronous Serial Clock Input/Output for I2C1
SDA1	36(1), 43(2)	56(1), 67(2)	A38(1), A44(2)	I/O	ST	Synchronous Serial Data Input/Output for I2C1
SCL2	32	58	A39	I/O	ST	Synchronous Serial Clock Input/Output for I2C2
SDA2	31	59	B32	I/O	ST	Synchronous Serial Data Input/Output for I2C2
TMS	23	17	B9	I	ST	JTAG Test Mode Select Pin
TCK	27	38	A26	I	ST	JTAG Test Clock Input Pin
TDI	28	60	A40	I	—	JTAG Test Clock Input Pin
TDO	24	61	B33	O	—	JTAG Test Clock Output Pin
RTCC	42	68	B37	O	—	Real-Time Clock Alarm Output

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA			
CVREF-	15	28	A21	I	Analog	Comparator Voltage Reference (Low)
CVREF+	16	29	B17	I	Analog	Comparator Voltage Reference (High)
CVREFOUT	23	34	A24	I	Analog	Comparator Voltage Reference (Output)
C1INA	11	20	A12	I	Analog	Comparator 1 Inputs
C1INB	12	21	B11	I	Analog	
C1INC	5	11	B6	I	Analog	
C1IND	4	10	A7	I	Analog	
C2INA	13	22	A13	I	Analog	Comparator 2 Inputs
C2INB	14	23	B13	I	Analog	
C2INC	8	14	A9	I	Analog	
C2IND	6	12	A8	I	Analog	
C1OUT	PPS	PPS	PPS	O	—	Comparator 1 Output
C2OUT	PPS	PPS	PPS	O	—	Comparator 2 Output
PMALL	30	44	A29	O	TTL/ST	Parallel Master Port Address Latch Enable Low Byte
PMALH	29	43	B24	O	TTL/ST	Parallel Master Port Address Latch Enable High Byte
PMA0	30	44	A29	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA1	29	43	B24	O	TTL/ST	Parallel Master Port Address bit 0 Input (Buffered Slave modes) and Output (Master modes)
PMA2	8	14	A9	O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes)
PMA3	6	12	A8	O	TTL/ST	
PMA4	5	11	B6	O	TTL/ST	
PMA5	4	10	A7	O	TTL/ST	
PMA6	16	29	B17	O	TTL/ST	
PMA7	22	28	A21	O	TTL/ST	
PMA8	32	50	A32	O	TTL/ST	
PMA9	31	49	B27	O	TTL/ST	
PMA10	28	42	A28	O	TTL/ST	
PMA11	27	41	B23	O	TTL/ST	
PMA12	24	35	B20	O	TTL/ST	
PMA13	23	34	A24	O	TTL/ST	
PMA14	45	71	A46	O	TTL/ST	
PMA15	44	70	B38	O	TTL/ST	
PMCS1	45	71	A46	O	TTL/ST	
PMCS2	44	70	B38	O	TTL/ST	
PMD0	60	93	B52	I/O	TTL/ST	
PMD1	61	94	A64	I/O	TTL/ST	
PMD2	62	98	A66	I/O	TTL/ST	

Legend: CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
P = Power
I = Input

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA			
CTED4	22	33	B19	I	ST	CTMU External Edge Input 4
CTED5	29	43	B24	I	ST	CTMU External Edge Input 5
CTED6	30	44	A29	I	ST	CTMU External Edge Input 6
CTED7	—	9	B5	I	ST	CTMU External Edge Input 7
CTED8	—	92	A62	I	ST	CTMU External Edge Input 8
CTED9	—	60	A40	I	ST	CTMU External Edge Input 9
CTED10	21	32	A23	I	ST	CTMU External Edge Input 10
CTED11	23	34	A24	I	ST	CTMU External Edge Input 11
CTED12	15	24	A15	I	ST	CTMU External Edge Input 12
CTED13	14	23	B13	I	ST	CTMU External Edge Input 13
$\overline{MCLR}$	7	13	B7	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	A22	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	B18	P	P	Ground reference for analog modules
VDD	10, 26, 38, 57	2, 16, 37, 46, 62, 86	B1, A10, A14, B21, A30, A41, A48, A59, B53	P	—	Positive supply for peripheral logic and I/O pins
VCAP	56	85	B48	P	—	Capacitor for Internal Voltage Regulator
VSS	9, 25, 41	15, 36, 45, 65, 75	A3, B8, B12, A25, B25, A43, B41, A63	P	—	Ground reference for logic and I/O pins
VREF+	16	29	B17	I	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	A21	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)

bit 9-8 **IS1<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-2 **IP0<2:0>:** Interrupt Priority bits
111 = Interrupt priority is 7
•
•
•
010 = Interrupt priority is 2
001 = Interrupt priority is 1
000 = Interrupt is disabled

bit 1-0 **IS0<1:0>:** Interrupt Subpriority bits
11 = Interrupt subpriority is 3
10 = Interrupt subpriority is 2
01 = Interrupt subpriority is 1
00 = Interrupt subpriority is 0

Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

8.0 OSCILLATOR CONFIGURATION

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 6. "Oscillator Configuration"** (DS60001112), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The PIC32MX330/350/370/430/450/470 oscillator system has the following modules and features:

- A Total of four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

REGISTER 9-2: CHEACC: CACHE ACCESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	CHEWEN	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	CHEIDX<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **CHEWEN:** Cache Access Enable bits for registers CHETAG, CHEMSK, CHEW0, CHEW1, CHEW2, and CHEW3

1 = The cache line selected by CHEIDX<3:0> is writeable

0 = The cache line selected by CHEIDX<3:0> is not writeable

bit 30-4 **Unimplemented:** Write '0'; ignore read

bit 3-0 **CHEIDX<3:0>:** Cache Line Index bits

The value selects the cache line for reading or writing.

REGISTER 10-4: DCRCCON: DMA CRC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0
	—	—	BYTO<1:0>		WBO(1)	—	—	BITO(1)
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	PLEN<4:0>				
7:0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CRCEN	CRCAPP(1)	CRCTYP	—	—	CRCCH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **BYTO<1:0>:** CRC Byte Order Selection bits
- 11 = Endian byte swap on half-word boundaries (i.e., source half-word order with reverse source byte order per half-word)
- 10 = Swap half-words on word boundaries (i.e., reverse source half-word order with source byte order per half-word)
- 01 = Endian byte swap on word boundaries (i.e., reverse source byte order)
- 00 = No swapping (i.e., source byte order)

bit 27 **WBO:** CRC Write Byte Order Selection bit(1)
- 1 = Source data is written to the destination re-ordered as defined by BYTO<1:0>
- 0 = Source data is written to the destination unaltered

bit 26-25 **Unimplemented:** Read as '0'

bit 24 **BITO:** CRC Bit Order Selection bit(1)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
- 1 = The IP header checksum is calculated Least Significant bit (LSb) first (i.e., reflected)
- 0 = The IP header checksum is calculated Most Significant bit (MSb) first (i.e., not reflected)

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
- 1 = The LFSR CRC is calculated Least Significant bit first (i.e., reflected)
- 0 = The LFSR CRC is calculated Most Significant bit first (i.e., not reflected)

bit 23-13 **Unimplemented:** Read as '0'

bit 12-8 **PLEN<4:0>:** Polynomial Length bits(1)

When CRCTYP (DCRCCON<15>) = 1 (CRC module is in IP Header mode):
These bits are unused.

When CRCTYP (DCRCCON<15>) = 0 (CRC module is in LFSR mode):
Denotes the length of the polynomial – 1.

bit 7 **CRCEN:** CRC Enable bit
- 1 = CRC module is enabled and channel transfers are routed through the CRC module
- 0 = CRC module is disabled and channel transfers proceed normally

Note 1: When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 11-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	U-0	R/WC-0, HS
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF	—	VBUSVDIF

Legend:	WC = Write '1' to clear	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = Change in ID state is detected
- 0 = No change in ID state is detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1millisecond, but different from last time
- 0 = USB line state has not been stable for 1 millisecond

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = Change on the session valid input is detected
- 0 = No change on the session valid input is detected

TABLE 12-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection
RPD2	RPD2R	RPD2R<3:0>	0000 = No Connect 0001 = U3TX 0010 = U4RTS 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = OC3 1100 = Reserved 1101 = C2OUT 1110 = Reserved 1111 = Reserved
RPG8	RPG8R	RPG8R<3:0>	
RPF4	RPF4R	RPF4R<3:0>	
RPD10	RPD10R	RPD10R<3:0>	
RPF1	RPF1R	RPF1R<3:0>	
RPB9	RPB9R	RPB9R<3:0>	
RPB10	RPB10R	RPB10R<3:0>	
RPC14	RPC14R	RPC14R<3:0>	
RPB5	RPB5R	RPB5R<3:0>	
RPC1(4)	RPC1R	RPC1R<3:0>	
RPD14(4)	RPD14R	RPD14R<3:0>	
RPG1(4)	RPG1R	RPG1R<3:0>	
RPA14(4)	RPA14R	RPA14R<3:0>	
RPD3	RPD3R	RPD3R<3:0>	0000 = No Connect 0001 = U2TX 0010 = Reserved 0011 = U1TX 0100 = U5RTS(4) 0101 = Reserved 0110 = SDO2 0111 = Reserved 1000 = SDO1 1001 = Reserved 1010 = Reserved 1011 = OC4 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
RPG7	RPG7R	RPG7R<3:0>	
RPF5	RPF5R	RPF5R<3:0>	
RPD11	RPD11R	RPD11R<3:0>	
RPF0	RPF0R	RPF0R<3:0>	
RPB1	RPB1R	RPB1R<3:0>	
RPE5	RPE5R	RPE5R<3:0>	
RPC13	RPC13R	RPC13R<3:0>	
RPB3	RPB3R	RPB3R<3:0>	
RPF3(2)	RPF3R	RPF3R<3:0>	
RPC4(4)	RPC4R	RPC4R<3:0>	
RPD15(4)	RPD15R	RPD15R<3:0>	
RPG0(4)	RPG0R	RPG0R<3:0>	
RPA15(4)	RPA15R	RPA15R<3:0>	

Note 1: This selection is only available on General Purpose devices.

2: This selection is only available on 64-pin General Purpose devices.

3: This selection is only available on 100-pin General Purpose devices.

4: This selection is only available on 100-pin USB and General Purpose devices.

5: This selection is not available on 64-pin USB devices.

24.0 COMPARATOR

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. "Comparator"** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

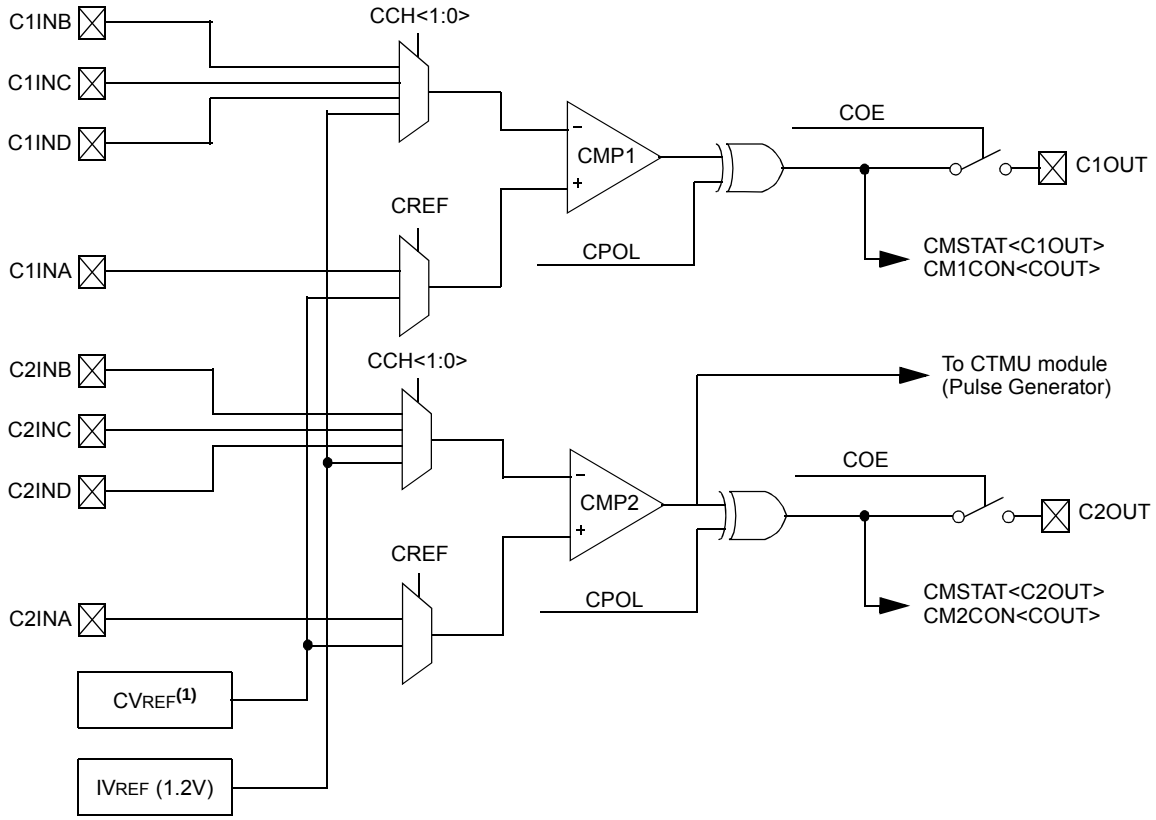
The Analog Comparator module contains two comparators that can be configured in a variety of ways.

The following are key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be Inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 24-1.

FIGURE 24-1: COMPARATOR BLOCK DIAGRAM



Note 1: Internally connected. See **Section 25.0 "Comparator Voltage Reference (CVREF)"** for more information.

REGISTER 28-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	U-0	U-0	U-0	U-0
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
	—	—	—	—	—	FSRSSEL<2:0>		
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **FVBUSONIO:** USB VBUS_ON Selection bit
- 1 = VBUSON pin is controlled by the USB module
- 0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
- 1 = USBID pin is controlled by the USB module
- 0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
- 1 = Allow only one reconfiguration
- 0 = Allow multiple reconfigurations

bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit
- 1 = Allow only one reconfiguration
- 0 = Allow multiple reconfigurations

bit 27-19 **Unimplemented:** Read as '0'

bit 18-16 **FSRSSEL<2:0>:** Shadow Register Set Priority Select bit

These bits assign an interrupt priority to a shadow register.
- 111 = Shadow register set used with interrupt priority 7
- 110 = Shadow register set used with interrupt priority 6
- 101 = Shadow register set used with interrupt priority 5
- 100 = Shadow register set used with interrupt priority 4
- 011 = Shadow register set used with interrupt priority 3
- 010 = Shadow register set used with interrupt priority 2
- 001 = Shadow register set used with interrupt priority 1
- 000 = Shadow register set used with interrupt priority 0

bit 15-0 **USERID<15:0>:** This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

REGISTER 28-6: DEVID: DEVICE AND REVISION ID REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R	R	R	R	R	R	R	R
	VER<3:0>(1)				DEVID<27:24>(1)			
23:16	R	R	R	R	R	R	R	R
	DEVID<23:16>(1)							
15:8	R	R	R	R	R	R	R	R
	DEVID<15:8>(1)							
7:0	R	R	R	R	R	R	R	R
	DEVID<7:0>(1)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID(1)

Note 1: See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

30.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

30.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

30.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

30.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

30.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symb.**	**Characteristics**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
		Input Low Voltage					
DI10	VIL	I/O Pins with PMP	VSS	—	0.15 VDD	V	
		I/O Pins	VSS	—	0.2 VDD	V	
DI18		SDAx, SCLx	VSS	—	0.3 VDD	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	VSS	—	0.8	V	SMBus enabled **(Note 4)**
		Input High Voltage					
DI20	VIH	I/O Pins not 5V-tolerant**(5)**	0.65 VDD	—	VDD	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP**(5)**	0.25 VDD + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant**(5)**	0.65 VDD	—	5.5	V	
DI28		SDAx, SCLx	0.65 VDD	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)**
DI30	ICNPU	**Change Notification Pull-up Current**	—	—	-50	µA	VDD = 3.3V, VPIN = VSS **(Note 3,6)**
DI31	ICNPD	**Change Notification Pull-down Current(4)**	—	50	—	µA	VDD = 3.3V, VPIN = VDD

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Device Pin Tables"** section for the 5V tolerant pins.

6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

7: VIL source < (VSS - 0.3). Characterized but not tested.

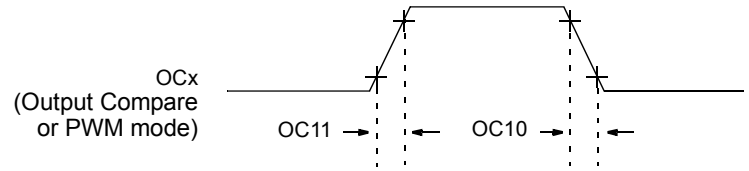
8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

9: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

10: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If **Note 7**, IICL = (((Vss - 0.3) - VIL source) / Rs). If **Note 8**, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

FIGURE 31-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 31-1 for load conditions.

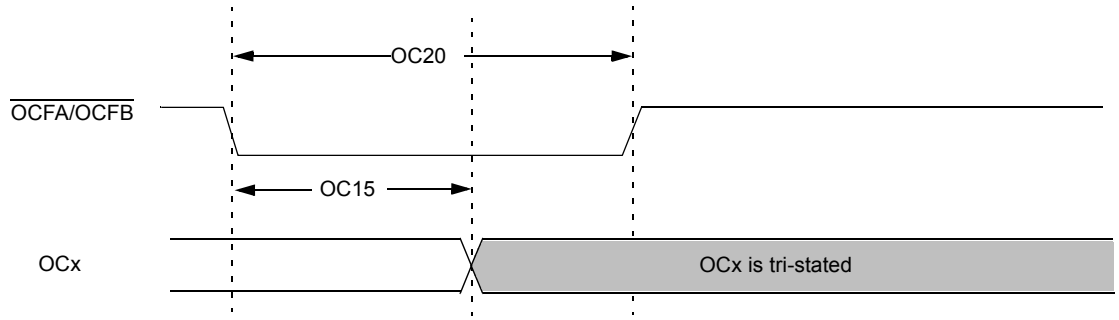
TABLE 31-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-9: OCx/PWM MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 31-1 for load conditions.

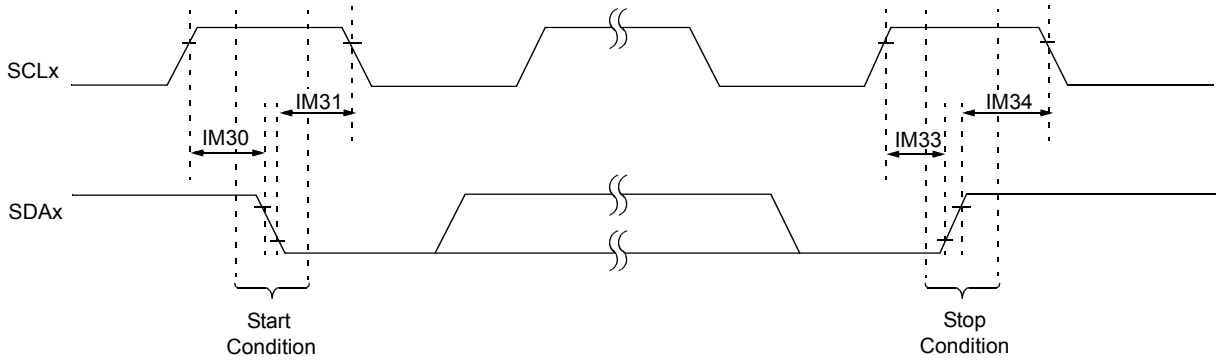
TABLE 31-28: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	**Symbol**	**Characteristics(1)**	**Min**	**Typical(2)**	**Max**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 31-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 31-1 for load conditions.

FIGURE 31-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)

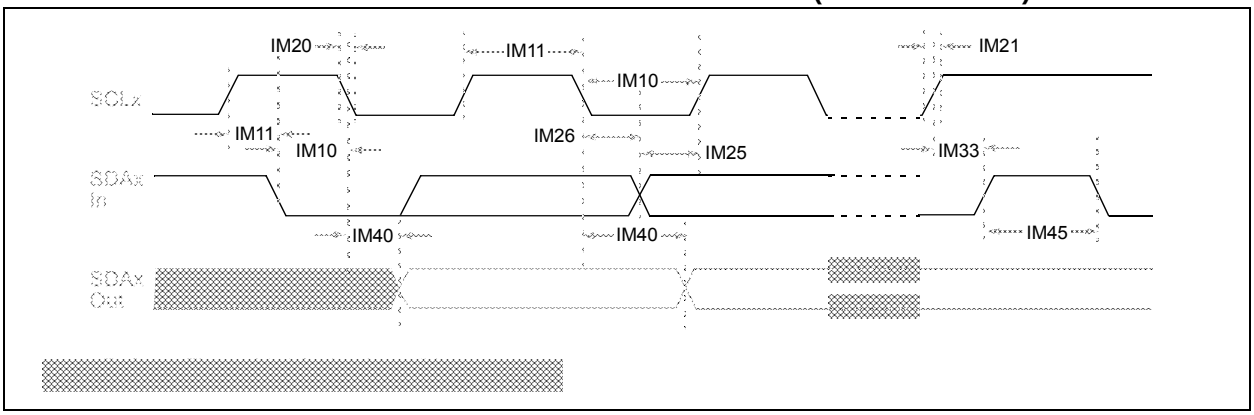


TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	ns	—
			400 kHz mode	TPB * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

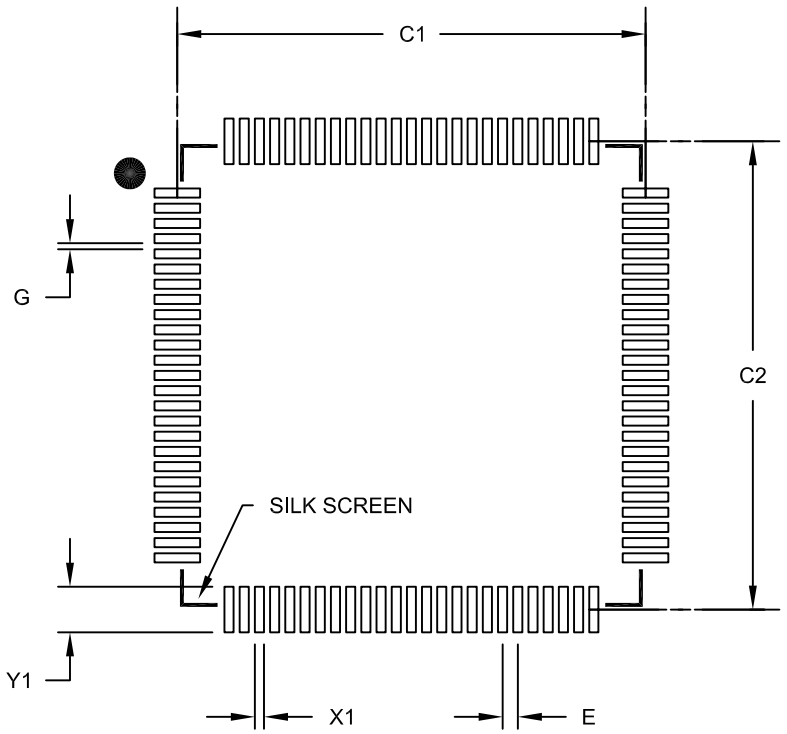
Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

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