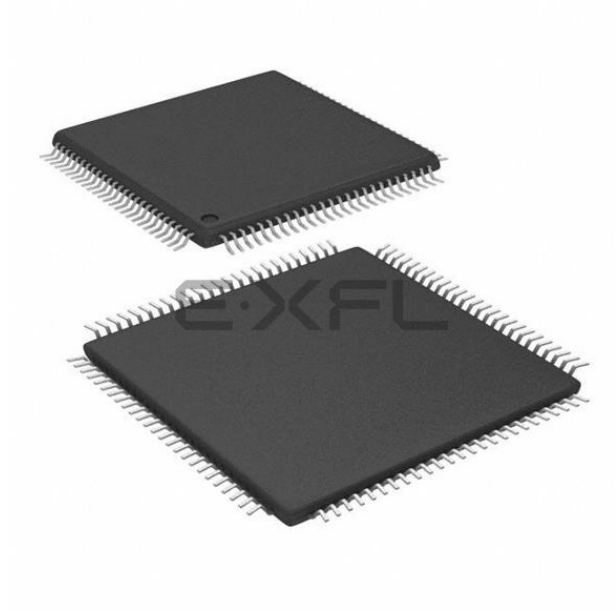
# Microchip Technology - PIC32MX330F064L-V/PT Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 28x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx330f064l-v-pt |

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**TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3060 | DCH0CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3070 | DCH0ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 3080 | DCH0INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3090 | DCH0SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30A0 | DCH0DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 30B0 | DCH0SSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30C0 | DCH0DSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30D0 | DCH0SPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHSPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30E0 | DCH0DPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHDPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 30F0 | DCH0CSIZ | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCSIZ<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3100 | DCH0CPTR | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHCPTR<15:0> | | | | | | | | | | | | | | | | 0000 |
| 3110 | DCH0DAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHPDAT<7:0> | | | | | | | | 0000 |
| 3120 | DCH1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | CHBUSY | — | — | — | — | — | — | CHCHNS | CHEN | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | | 0000 |
| 3130 | DCH1ECON | 31:16 | — | — | — | — | — | — | — | — | CHAIRQ<7:0> | | | | | | | | 00FF |
| | | 15:0 | CHSIRQ<7:0> | | | | | | | | CFORCE | CABORT | PATEN | SIRQEN | AIRQEN | — | — | — | FFF8 |
| 3140 | DCH1INT | 31:16 | — | — | — | — | — | — | — | — | CHSDIE | CHSHIE | CHDDIE | CHDHIE | CHBCIE | CHCCIE | CHTAIE | CHERIE | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | CHSDIF | CHSHIF | CHDDIF | CHDHIF | CHBCIF | CHCCIF | CHTAIF | CHERIF | 0000 |
| 3150 | DCH1SSA | 31:16 | CHSSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3160 | DCH1DSA | 31:16 | CHDSA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

**REGISTER 10-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHSSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size
.
.
.
0000000000000010 = 2 byte source size
0000000000000001 = 1 byte source size
0000000000000000 = 65,536 byte source size

**REGISTER 10-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHDSIZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size
.
.
.
0000000000000010 = 2 byte destination size
0000000000000001 = 1 byte destination size
0000000000000000 = 65,536 byte destination size

**TABLE 12-14: PORTF REGISTER MAP FOR PIC32MX430F064H, PIC32MX450F128H, PIC32MX450F256H, AND PIC32MX470F512H DEVICES ONLY**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 6510 | TRISF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | TRISF5 | TRISF4 | TRISF3 | — | TRISF1 | TRISF0 | xxxx |
| 6520 | PORTF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | RF5 | RF4 | RF3 | — | RF1 | RF0 | xxxx |
| 6530 | LATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | LATF5 | LATF4 | LATF3 | — | LATF1 | LATF0 | xxxx |
| 6540 | ODCF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | ODCF5 | ODCF4 | ODCF3 | — | ODCF1 | ODCF0 | xxxx |
| 6550 | CNPUF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNPUF5 | CNPUF4 | CNPUF3 | — | CNPUF1 | CNPUF0 | xxxx |
| 6560 | CNPDF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNPDF5 | CNPDF4 | CNPDF3 | — | CNPDF1 | CNPDF0 | xxxx |
| 6570 | CNCONF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 6580 | CNENF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CNIEF5 | CNIEF4 | CNIEF3 | — | CNIEF1 | CNIEF0 | xxxx |
| 6590 | CNSTATF | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | CN STATF5 | CN STATF4 | CN STATF3 | — | CN STATF1 | CN STATF0 | xxxx |

**Legend:** x = Unknown value on Reset; — = Unimplemented, read as '0'; Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

## 16.1 Control Register

**REGISTER 16-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | — | — | — | FEDGE | C32 |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 |
| | ICTMR | ICI<1:0> | | ICOV | ICBNE | ICM<2:0> | | |

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit |
| -n = Bit Value at POR: ('0', '1', x = unknown) | P = Programmable bit | r = Reserved bit |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Input Capture Module Enable bit(1)
- 1 = Module is enabled
- 0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = Halt in CPU Idle mode
- 0 = Continue to operate in CPU Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **FEDGE:** First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
- 1 = Capture rising edge first
- 0 = Capture falling edge first

bit 8 **C32:** 32-bit Capture Select bit
- 1 = 32-bit timer resource capture
- 0 = 16-bit timer resource capture

bit 7 **ICTMR:** Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
- 0 = Timer3 is the counter source for capture
- 1 = Timer2 is the counter source for capture

bit 6-5 **ICI<1:0>:** Interrupt Control bits
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture overflow has occurred
- 0 = No input capture overflow has occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty; at least one more capture value can be read
- 0 = Input capture buffer is empty

**Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**REGISTER 17-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1) | — | SIDL | — | — | — | — | — |
| 7:0 | U-0 | U-0 | R/W-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | OC32 | OCFLT(2) | OCTSEL | OCM<2:0> | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit(1)
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue operation when CPU enters Idle mode
- 0 = Continue operation in Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisions to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (cleared in HW only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin is enabled
- 110 = PWM mode on OCx; Fault pin is disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**2:** This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

## 20.2 Timing Diagrams

Figure 20-2 and Figure 20-3 illustrate typical receive and transmit timing for the UART module.

**FIGURE 20-2: UART RECEPTION**

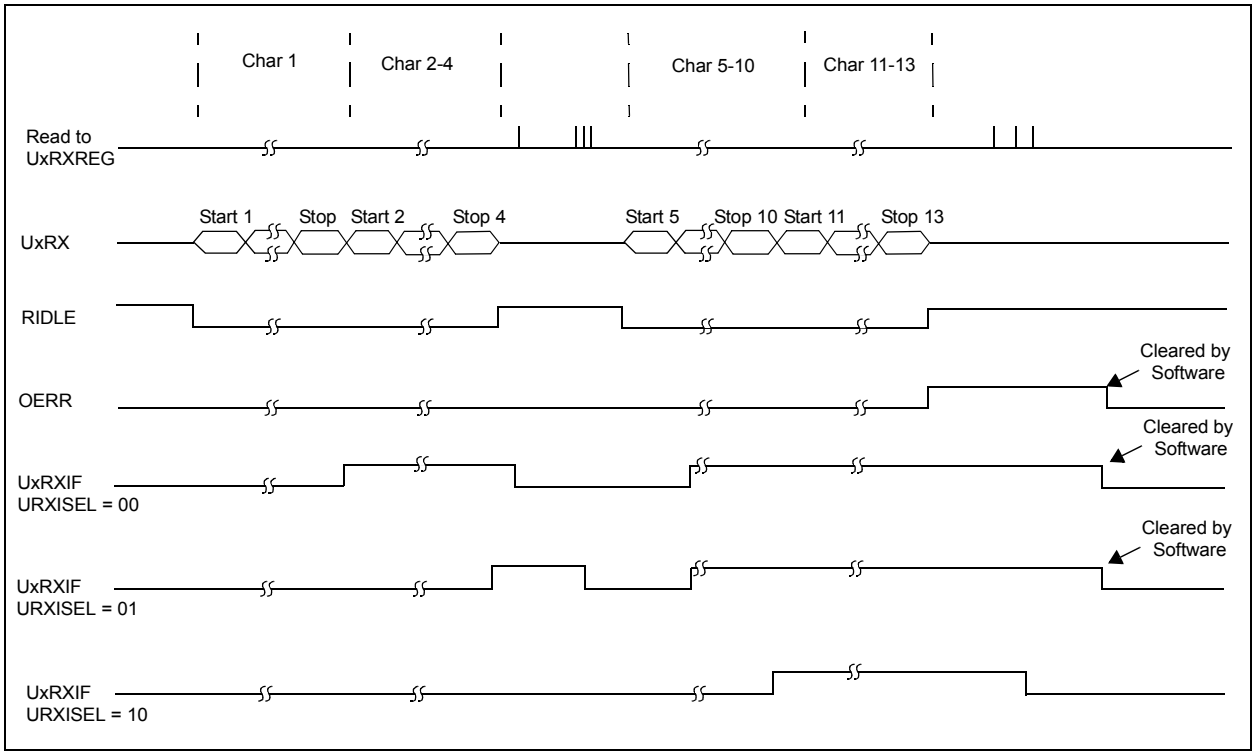
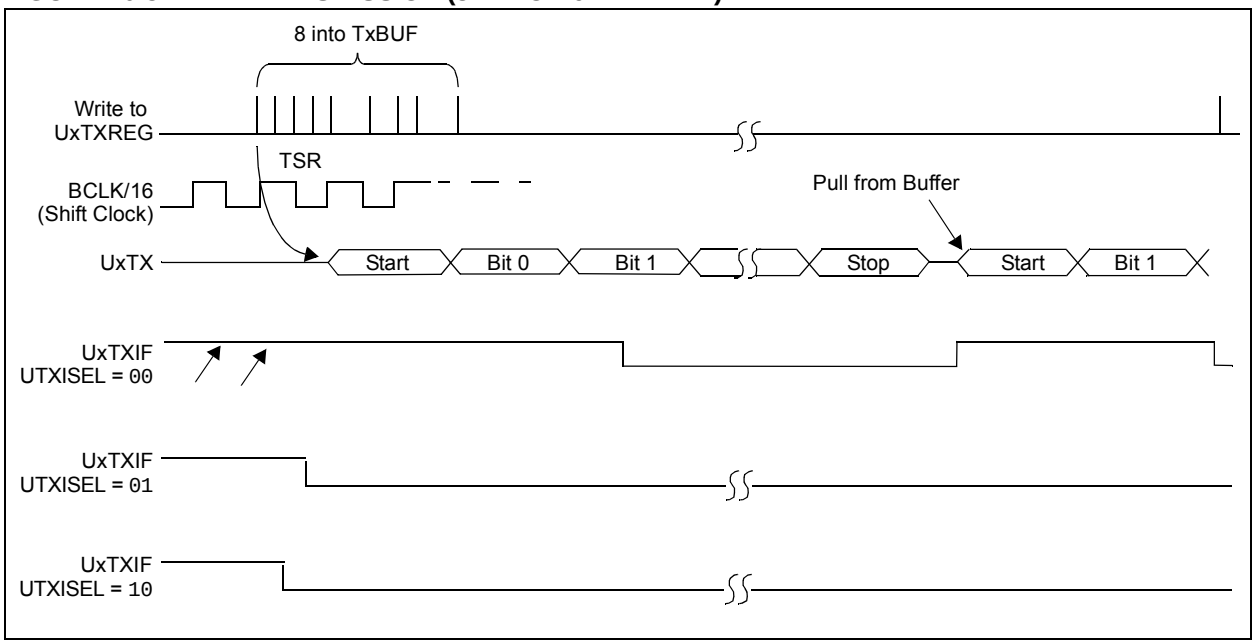



**FIGURE 20-3: TRANSMISSION (8-BIT OR 9-BIT DATA)**



**NOTES:**

**NOTES:**

## 27.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 27-1 for more information.

| **Note:** | Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits. |
|---|---|

**TABLE 27-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS**

| Peripheral(1) | PMDx bit Name(1) | Register Name and Bit Location |
|---|---|---|
| ADC1 | AD1MD | PMD1<0> |
| CTMU | CTMUMD | PMD1<8> |
| Comparator Voltage Reference | CVRMD | PMD1<12> |
| Comparator 1 | CMP1MD | PMD2<0> |
| Comparator 2 | CMP2MD | PMD2<1> |
| Input Capture 1 | IC1MD | PMD3<0> |
| Input Capture 2 | IC2MD | PMD3<1> |
| Input Capture 3 | IC3MD | PMD3<2> |
| Input Capture 4 | IC4MD | PMD3<3> |
| Input Capture 5 | IC5MD | PMD3<4> |
| Output Compare 1 | OC1MD | PMD3<16> |
| Output Compare 2 | OC2MD | PMD3<17> |
| Output Compare 3 | OC3MD | PMD3<18> |
| Output Compare 4 | OC4MD | PMD3<19> |
| Output Compare 5 | OC5MD | PMD3<20> |
| Timer1 | T1MD | PMD4<0> |
| Timer2 | T2MD | PMD4<1> |
| Timer3 | T3MD | PMD4<2> |
| Timer4 | T4MD | PMD4<3> |
| Timer5 | T5MD | PMD4<4> |
| UART1 | U1MD | PMD5<0> |
| UART2 | U2MD | PMD5<1> |
| UART3 | U3MD | PMD5<2> |
| UART4 | U4MD | PMD5<3> |
| UART5 | U5MD | PMD5<4> |
| SPI1 | SPI1MD | PMD5<8> |
| SPI2 | SPI2MD | PMD5<9> |
| I2C1 | I2C1MD | PMD5<16> |
| I2C2 | I2C2MD | PMD5<17> |
| USB(2) | USBMD | PMD5<24> |
| RTCC | RTCCMD | PMD6<0> |
| Reference Clock Output | REFOMD | PMD6<1> |
| PMP | PMPMD | PMD6<16> |

**Note 1:** Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: "PIC32MX330/350/370/430/450/470 Controller Family Features"** for the lists of available peripherals.

**2:** Module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

## 31.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX330/350/370/430/450/470 electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX330/350/370/430/450/470 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

**(See Note 1)**

Ambient temperature under bias ..... -40°C to +105°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$ **(Note 3)** ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 2.3V$ **(Note 3)** ..... -0.3V to +6.0V
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} < 2.3V$ **(Note 3)** ..... -0.3V to +3.6V
Voltage on D+ or D- pin with respect to $V_{USB3V3}$ ..... -0.3V to ($V_{USB3V3}$ + 0.3V)
Voltage on $V_{BUS}$ with respect to $V_{SS}$ ..... -0.3V to +5.5V
Maximum current out of $V_{SS}$ pin(s) ..... 200 mA
Maximum current into $V_{DD}$ pin(s) **(Note 2)** ..... 200 mA
Maximum output current sourced/sunk by any 4x I/O pin ..... 15 mA
Maximum output current sourced/sunk by any 8x I/O pin ..... 25 mA
Maximum current sunk by all ports ..... 150 mA
Maximum current sourced by all ports **(Note 2)** ..... 150 mA

**Note 1:** Stresses above those listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

**3:** See the **"Device Pin Tables"** section for the 5V tolerant pins.

**TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** | |
| **PIC32MX330 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 20 | 55 | μA | -40°C | Base Power-Down Current |
| DC40l | 38 | 55 | μA | +25°C | |
| DC40n | 128 | 167 | μA | +85°C | |
| DC40m | 261 | 419 | μA | +105ºC | |
| **PIC32MX430 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 12 | 28 | μA | -40°C | Base Power-Down Current |
| DC40l | 21 | 28 | μA | +25°C | |
| DC40n | 128 | 167 | μA | +85°C | |
| DC40m | 261 | 419 | μA | +105ºC | |
| **PIC32MX350F128 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 31 | 70 | μA | -40°C | Base Power-Down Current |
| DC40l | 45 | 70 | μA | +25°C | |
| DC40n | 175 | 280 | μA | +85°C | |
| DC40m | 415 | 600 | μA | +105ºC | |
| **PIC32MX450F128 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 19 | 35 | μA | -40°C | Base Power-Down Current |
| DC40l | 28 | 35 | μA | +25°C | |
| DC40n | 175 | 280 | μA | +85°C | |
| DC40m | 415 | 600 | μA | +105ºC | |

**Note 1:** The test conditions for IPD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled
- Voltage regulator is off during Sleep mode (VREGS bit in the RCON register = 0)

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** 120 MHz commercial devices only (0ºC to +70ºC).

**TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** | |
| **PIC32MX370 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 55 | 95 | µA | -40°C | Base Power-Down Current |
| DC40l | 81 | 95 | µA | +25°C | |
| DC40n | 281 | 450 | µA | +85°C | |
| DC40m | 559 | 895 | µA | +105ºC | |
| **PIC32MX470 Devices Only** | | | | | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| DC40k | 33 | 78 | µA | -40°C | Base Power-Down Current |
| DC40o | 33 | 78 | µA | 0°C(5) | |
| DC40l | 49 | 78 | µA | +25°C | |
| DC40p | 281 | 450 | µA | +70°C(5) | |
| DC40n | 281 | 450 | µA | +85°C | |
| DC40m | 559 | 895 | µA | +105ºC | |
| **PIC32MX330/350/370/430/450/470 Devices** | | | | | |
| **Module Differential Current** | | | | | |
| DC41e | 6.7 | 20 | µA | 3V | Watchdog Timer Current: ΔIWDT **(Note 3)** |
| DC42e | 29.1 | 50 | µA | 3V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)** |
| DC43d | 1000 | 1200 | µA | 3V | ADC: ΔIADC **(Notes 3,4)** |

**Note 1:** The test conditions for IPD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled
- Voltage regulator is off during Sleep mode (VREGS bit in the RCON register = 0)

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** 120 MHz commercial devices only (0ºC to +70ºC).

**TABLE 31-12: DC CHARACTERISTICS: PROGRAM MEMORY(3)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| D130 | EP | Cell Endurance | 20,000 | — | — | E/W | — |
| D131 | VPR | VDD for Read | 2.3 | — | 3.6 | V | — |
| D132 | VPEW | VDD for Erase or Write | 2.3 | — | 3.6 | V | — |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated |
| D135 | IDDP | Supply Current during Programming | — | 10 | — | mA | — |
| D138 | TWW | Word Write Cycle Time(4) | 44 | — | 59 | µs | — |
| D136 | TRW | Row Write Cycle Time(2,4) | 2.8 | 3.3 | 3.8 | ms | — |
| D137 | TPE | Page Erase Cycle Time(4) | 22 | — | 29 | ms | — |
| D139 | TCE | Chip Erase Cycle Time(4) | 86 | — | 116 | ms | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 8 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

**4:** This parameter depends on the FRC accuracy (see Table 31-20) and the FRC tuning values (see Register 8-2).

**TABLE 31-13: DC CHARACTERISTICS: PROGRAM FLASH MEMORY WAIT STATE**

| DC CHARACTERISTICS | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|
| **Required Flash Wait States** | **SYSCLK** | **Units** | **Conditions** |
| 0 Wait State | 0-40 | MHz | -40ºC to +85ºC |
| | 0-30 | MHz | -40ºC to +105ºC |
| 1 Wait State | 41-80 | MHz | -40ºC to +85ºC |
| | 31-60 | MHz | -40ºC to +105ºC |
| 2 Wait States | 81-100 | MHz | -40ºC to +85ºC |
| | 61-80 | MHz | -40ºC to +105ºC |
| 3 Wait States | 101-120 | MHz | 0ºC to +70ºC |

**TABLE 31-18: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FOSC | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC<br>4 | —<br>— | 50<br>50 | MHz<br>MHz | EC **(Note 4)**<br>ECPLL **(Note 3)** |
| OS11 | | Oscillator Crystal Frequency | 3 | — | 10 | MHz | XT **(Note 4)** |
| OS12 | | | 4 | — | 10 | MHz | XTPLL **(Notes 3,4)** |
| OS13 | | | 10 | — | 25 | MHz | HS **(Note 4)** |
| OS14 | | | 10 | — | 25 | MHz | HSPLL **(Notes 3,4)** |
| OS15 | | | 32 | 32.768 | 100 | kHz | SOSC **(Note 4)** |
| OS20 | TOSC | TOSC = 1/FOSC = TCY **(Note 2)** | — | — | — | — | See parameter OS10 for FOSC value |
| OS30 | TOSL, TOSH | External Clock In (OSC1) High or Low Time | 0.45 x TOSC | — | — | ns | EC **(Note 4)** |
| OS31 | TOSR, TOSF | External Clock In (OSC1) Rise or Fall Time | — | — | 0.05 x TOSC | ns | EC **(Note 4)** |
| OS40 | TOST | Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and SOSC Clock Oscillator modes) | — | 1024 | — | TOSC | **(Note 4)** |
| OS41 | TFSCM | Primary Clock Fail Safe Time-out Period | — | 2 | — | ms | **(Note 4)** |
| OS42 | GM | External Oscillator Transconductance (Primary Oscillator only) | — | 12 | — | mA/V | VDD = 3.3V, TA = +25°C **(Note 4)** |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

**2:** Instruction cycle period (TCY) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

**3:** PLL input requirements: 4 MHz ≤ FPLLIN ≤ 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

**4:** This parameter is characterized, but not tested in manufacturing.

**FIGURE 32-9: TYPICAL IIDLE CURRENT @ VDD = 3.3V**

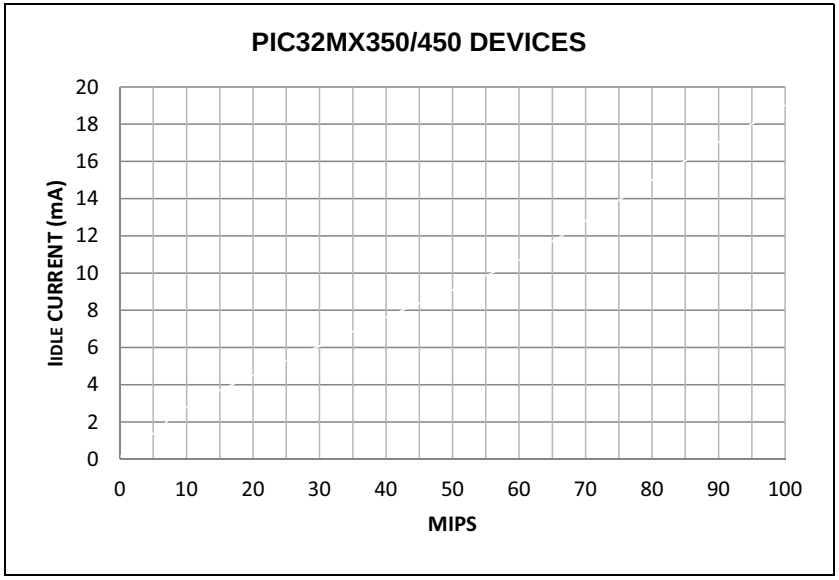



**FIGURE 32-10: TYPICAL IIDLE CURRENT @ VDD = 3.3V**

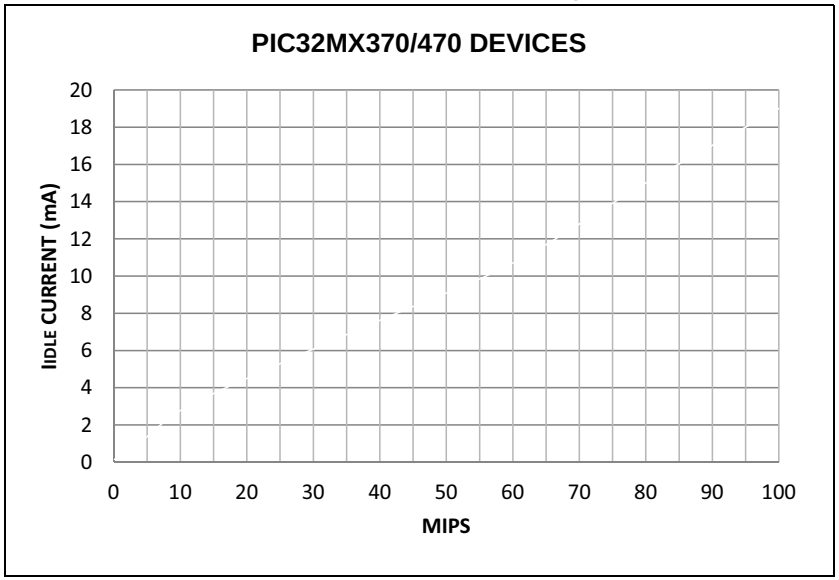



**FIGURE 32-11: TYPICAL IDD CURRENT @ VDD = 3.3V**

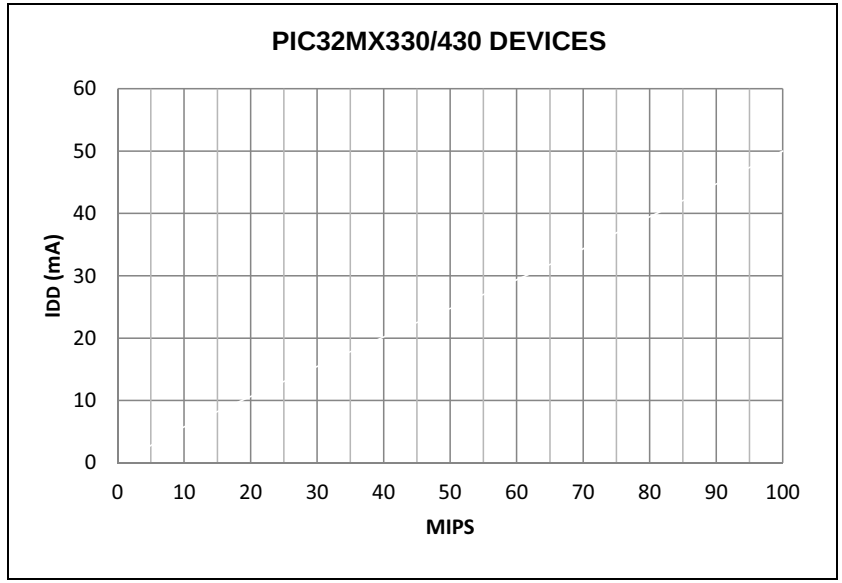
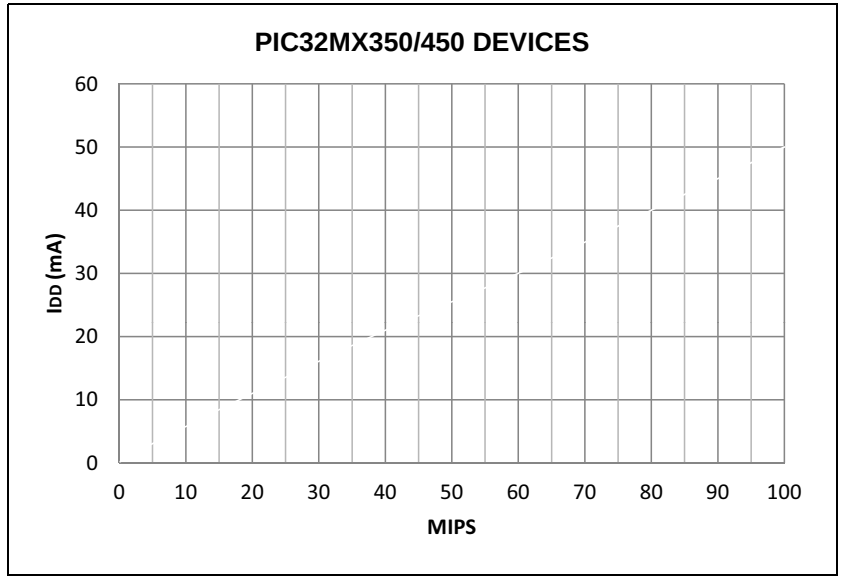
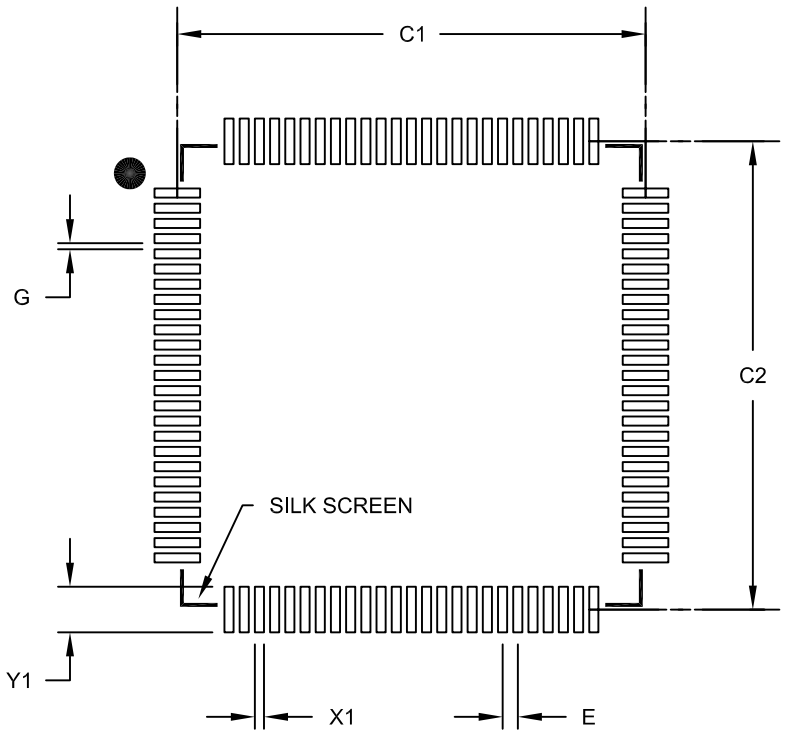



**FIGURE 32-12: TYPICAL IDD CURRENT @ VDD = 3.3V**



100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Contact Pad Spacing | C1 | | 15.40 | |
| Contact Pad Spacing | C2 | | 15.40 | |
| Contact Pad Width (X100) | X1 | | | 0.30 |
| Contact Pad Length (X100) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

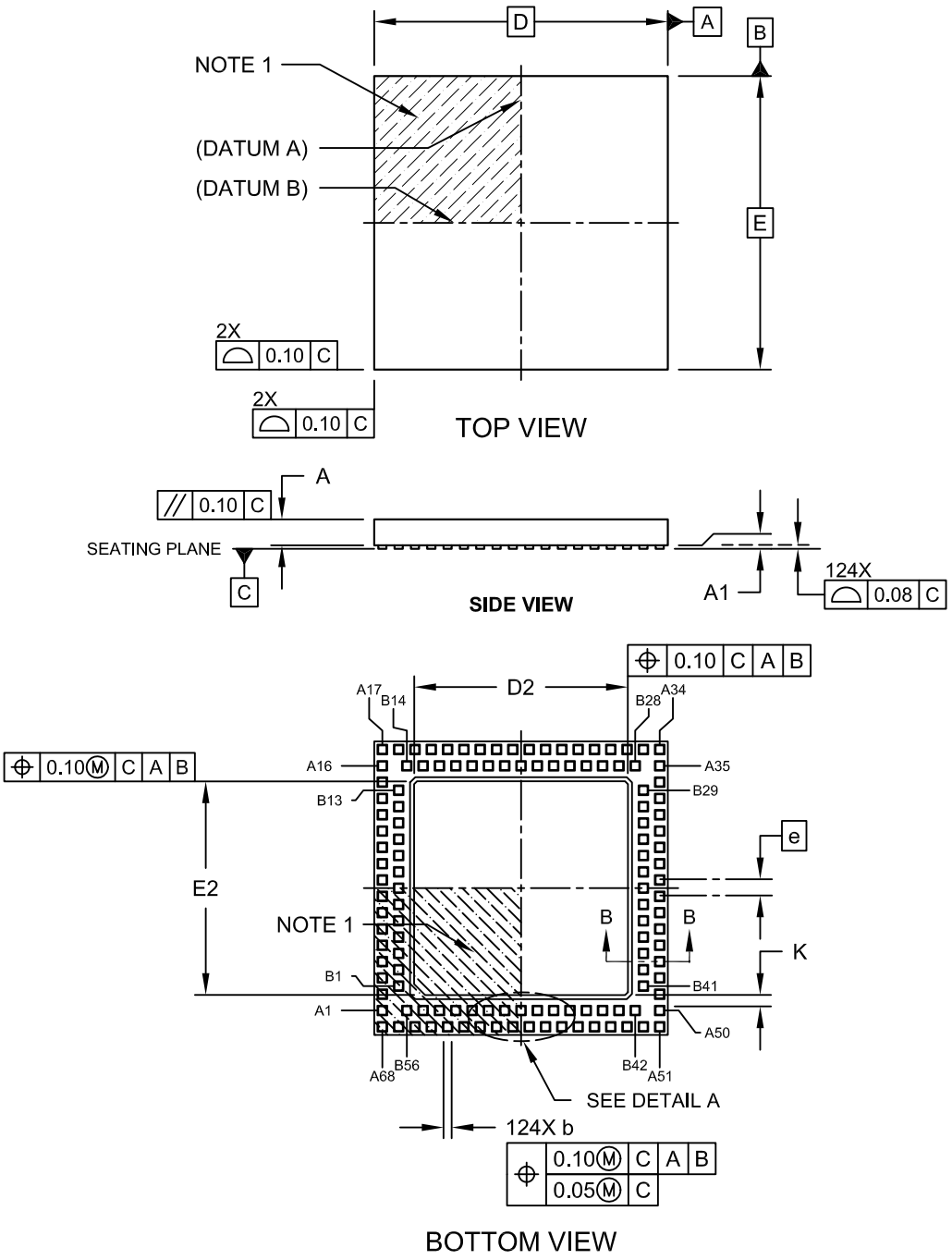
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

### 124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-193A Sheet 1 of 2

# APPENDIX A: REVISION HISTORY

## Revision A (July 2012)

This is the initial released version of the document.

## Revision B (April 2013)

**Note:** The status of this data sheet was updated to Preliminary; however, any electrical specifications listed for PIC32MX370/470 devices is to be considered Advance Information and is marked accordingly.

This revision includes the following updates, as shown in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/Graphics/Touch (HMI), USB, and Advanced Analog"** | SRAM was changed from 32 KB to 64 KB.<br>Data Memory (KB) was changed from 32 to 64 for the following devices (see Table 1):<br>• PIC32MX350F256H<br>• PIC32MX350F256L<br>• PIC32MX450F256H<br>• PIC32MX450F256L<br>The following devices were added:<br>• PIC32MX370F512H<br>• PIC32MX370F512L<br>• PIC32MX470F512H<br>• PIC32MX470F512L |
| **4.0 "Memory Organization"** | The Memory Map for Devices with 256 KB of Program Memory was updated (see Figure 4-3).<br>The Memory Map for Devices with 512 KB of Program Memory was added (see Figure 4-4). |
| **7.0 "Interrupt Controller"** | Updated the Interrupt IRQ, Vector and Bit Locations (see Table 7-1). |
| **20.0 "Parallel Master Port (PMP)"** | Added the CS2 bit and updated the ADDR bits in the Parallel Port Address register (see Register 20-3). |
| **27.0 "Special Features"** | Updated the PWP bit in the Device Configuration Word 3 register (see Register 27-4). |
| **30.0 "Electrical Characteristics"** | Note 2 in the DC Characteristics: Operating Current ($I_{DD}$) were updated (see Table 30-5).<br>Note 1 in the DC Characteristics: Idle Current ($I_{IDLE}$) were updated (see Table 30-6).<br>Note 1 in the DC Characteristics: Power-down Current ($I_{PD}$) were updated (see Table 30-7).<br>Updated Program Memory values for parameters D135 ($T_{WW}$), D136 ($T_{RW}$), and D137 ($T_{PE}$ and $T_{CE}$) (see Table 30-12). |
| **31.0 "DC and AC Device Characteristics Graphs"** | New $I_{DD}$, $I_{IDLE}$, and $I_{PD}$ current graphs were added for PIC32MX330/430 devices and PIC32MX350/450 devices. |

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