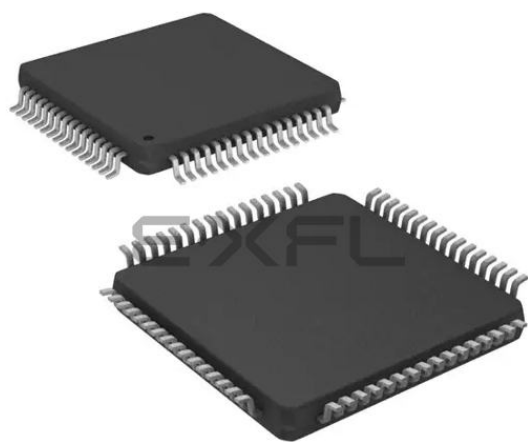




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                               |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                        |
| Core Processor             | MIPS32® M4K™                                                                                                                                                                  |
| Core Size                  | 32-Bit Single-Core                                                                                                                                                            |
| Speed                      | 80MHz                                                                                                                                                                         |
| Connectivity               | I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART                                                                                                                          |
| Peripherals                | Brown-out Detect/Reset, DMA, POR, PWM, WDT                                                                                                                                    |
| Number of I/O              | 53                                                                                                                                                                            |
| Program Memory Size        | 128KB (128K x 8)                                                                                                                                                              |
| Program Memory Type        | FLASH                                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                                             |
| RAM Size                   | 32K x 8                                                                                                                                                                       |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V                                                                                                                                                                   |
| Data Converters            | A/D 28x10b                                                                                                                                                                    |
| Oscillator Type            | Internal                                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                                                                                 |
| Package / Case             | 64-TQFP                                                                                                                                                                       |
| Supplier Device Package    | 64-TQFP (10x10)                                                                                                                                                               |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx350f128ht-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx350f128ht-i-pt</a> |

# PIC32MX330/350/370/430/450/470

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NOTES:

# PIC32MX330/350/370/430/450/470

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NOTES:

# PIC32MX330/350/370/430/450/470

**TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)**

| Interrupt Source <sup>(1)</sup>    | IRQ # | Vector # | Interrupt Bit Location |          |              |              | Persistent Interrupt |
|------------------------------------|-------|----------|------------------------|----------|--------------|--------------|----------------------|
|                                    |       |          | Flag                   | Enable   | Priority     | Sub-priority |                      |
| CNB – PORTB Input Change Interrupt | 45    | 33       | IFS1<13>               | IEC1<13> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| CNC – PORTC Input Change Interrupt | 46    | 33       | IFS1<14>               | IEC1<14> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| CND – PORTD Input Change Interrupt | 47    | 33       | IFS1<15>               | IEC1<15> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| CNE – PORTE Input Change Interrupt | 48    | 33       | IFS1<16>               | IEC1<16> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| CNF – PORTF Input Change Interrupt | 49    | 33       | IFS1<17>               | IEC1<17> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| CNG – PORTG Input Change Interrupt | 50    | 33       | IFS1<18>               | IEC1<18> | IPC8<12:10>  | IPC8<9:8>    | Yes                  |
| PMP – Parallel Master Port         | 51    | 34       | IFS1<19>               | IEC1<19> | IPC8<20:18>  | IPC8<17:16>  | Yes                  |
| PMPE – Parallel Master Port Error  | 52    | 34       | IFS1<20>               | IEC1<20> | IPC8<20:18>  | IPC8<17:16>  | Yes                  |
| SPI2E – SPI2 Fault                 | 53    | 35       | IFS1<21>               | IEC1<21> | IPC8<28:26>  | IPC8<25:24>  | Yes                  |
| SPI2RX – SPI2 Receive Done         | 54    | 35       | IFS1<22>               | IEC1<22> | IPC8<28:26>  | IPC8<25:24>  | Yes                  |
| SPI2TX – SPI2 Transfer Done        | 55    | 35       | IFS1<23>               | IEC1<23> | IPC8<28:26>  | IPC8<25:24>  | Yes                  |
| U2E – UART2 Error                  | 56    | 36       | IFS1<24>               | IEC1<24> | IPC9<4:2>    | IPC9<1:0>    | Yes                  |
| U2RX – UART2 Receiver              | 57    | 36       | IFS1<25>               | IEC1<25> | IPC9<4:2>    | IPC9<1:0>    | Yes                  |
| U2TX – UART2 Transmitter           | 58    | 36       | IFS1<26>               | IEC1<26> | IPC9<4:2>    | IPC9<1:0>    | Yes                  |
| I2C2B – I2C2 Bus Collision Event   | 59    | 37       | IFS1<27>               | IEC1<27> | IPC9<12:10>  | IPC9<9:8>    | Yes                  |
| I2C2S – I2C2 Slave Event           | 60    | 37       | IFS1<28>               | IEC1<28> | IPC9<12:10>  | IPC9<9:8>    | Yes                  |
| I2C2M – I2C2 Master Event          | 61    | 37       | IFS1<29>               | IEC1<29> | IPC9<12:10>  | IPC9<9:8>    | Yes                  |
| U3E – UART3 Error                  | 62    | 38       | IFS1<30>               | IEC1<30> | IPC9<20:18>  | IPC9<17:16>  | Yes                  |
| U3RX – UART3 Receiver              | 63    | 38       | IFS1<31>               | IEC1<31> | IPC9<20:18>  | IPC9<17:16>  | Yes                  |
| U3TX – UART3 Transmitter           | 64    | 38       | IFS2<0>                | IEC2<0>  | IPC9<20:18>  | IPC9<17:16>  | Yes                  |
| U4E – UART4 Error                  | 65    | 39       | IFS2<1>                | IEC2<1>  | IPC9<28:26>  | IPC9<25:24>  | Yes                  |
| U4RX – UART4 Receiver              | 66    | 39       | IFS2<2>                | IEC2<2>  | IPC9<28:26>  | IPC9<25:24>  | Yes                  |
| U4TX – UART4 Transmitter           | 67    | 39       | IFS2<3>                | IEC2<3>  | IPC9<28:26>  | IPC9<25:24>  | Yes                  |
| U5E – UART5 Error                  | 68    | 40       | IFS2<4>                | IEC2<4>  | IPC10<4:2>   | IPC10<1:0>   | Yes                  |
| U5RX – UART5 Receiver              | 69    | 40       | IFS2<5>                | IEC2<5>  | IPC10<4:2>   | IPC10<1:0>   | Yes                  |
| U5TX – UART5 Transmitter           | 70    | 40       | IFS2<6>                | IEC2<6>  | IPC10<4:2>   | IPC10<1:0>   | Yes                  |
| CTMU – CTMU Event                  | 71    | 41       | IFS2<7>                | IEC2<7>  | IPC10<12:10> | IPC10<9:8>   | Yes                  |
| DMA0 – DMA Channel 0               | 72    | 42       | IFS2<8>                | IEC2<8>  | IPC10<20:18> | IPC10<17:16> | No                   |
| DMA1 – DMA Channel 1               | 73    | 43       | IFS2<9>                | IEC2<9>  | IPC10<28:26> | IPC10<25:24> | No                   |
| DMA2 – DMA Channel 2               | 74    | 44       | IFS2<10>               | IEC2<10> | IPC11<4:2>   | IPC11<1:0>   | No                   |
| DMA3 – DMA Channel 3               | 75    | 45       | IFS2<11>               | IEC2<11> | IPC11<12:10> | IPC11<9:8>   | No                   |
| Lowest Natural Order Priority      |       |          |                        |          |              |              |                      |

**Note 1:** Not all interrupt sources are available on all devices. See **TABLE 1: “PIC32MX330/350/370/430/450/470 Controller Family Features”** for the list of available peripherals.

# PIC32MX330/350/370/430/450/470

**REGISTER 11-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | U-0           | R/W-0         |
|           | IDIE           | T1MSECIE       | LSTATEIE       | ACTVIE         | SESVIE         | SESENDIE       | —             | VBUSVDIE      |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIE:** ID Interrupt Enable bit

1 = ID interrupt is enabled

0 = ID interrupt is disabled

bit 6 **T1MSECIE:** 1 Millisecond Timer Interrupt Enable bit

1 = 1 millisecond timer interrupt is enabled

0 = 1 millisecond timer interrupt is disabled

bit 5 **LSTATEIE:** Line State Interrupt Enable bit

1 = Line state interrupt is enabled

0 = Line state interrupt is disabled

bit 4 **ACTVIE:** Bus Activity Interrupt Enable bit

1 = ACTIVITY interrupt is enabled

0 = ACTIVITY interrupt is disabled

bit 3 **SESVIE:** Session Valid Interrupt Enable bit

1 = Session valid interrupt is enabled

0 = Session valid interrupt is disabled

bit 2 **SESENDIE:** B-Session End Interrupt Enable bit

1 = B-session end interrupt is enabled

0 = B-session end interrupt is disabled

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIE:** A-VBUS Valid Interrupt Enable bit

1 = A-VBUS valid interrupt is enabled

0 = A-VBUS valid interrupt is disabled

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## REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | U-0            | U-0            | U-0            | U-0            | U-0            | R-0            | R-0           | R-0           |
|           | —              | —              | —              | —              | —              | FRMH<2:0>      |               |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

## REGISTER 11-15: U1TOK: USB TOKEN REGISTER

| Bit Range | Bit 31/23/15/7          | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|-------------------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0                     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —                       | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0                     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —                       | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0                     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —                       | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0                   | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | PID<3:0> <sup>(1)</sup> |                |                |                | EP<3:0>        |                |               |               |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits<sup>(1)</sup>

0001 = OUT (TX) token type transaction

1001 = IN (RX) token type transaction

1101 = SETUP (TX) token type transaction

**Note:** All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits

The four bit value must specify a valid endpoint.

**Note 1:** All other values are reserved and must not be used.

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**REGISTER 11-20: U1CNFG1: USB CONFIGURATION 1 REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 7:0       | R/W-0          | R/W-0          | U-0            | R/W-0          | U-0            | U-0            | U-0           | R/W-0         |
|           | UTEYE          | UOEMON         | —              | USBSIDL        | —              | —              | —             | UASUSPND      |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **UTEYE:** USB Eye-Pattern Test Enable bit

1 = Eye-Pattern Test is enabled

0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB  $\overline{\text{OE}}$  Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving

0 = OE signal is inactive

bit 5 **Unimplemented:** Read as '0'

bit 4 **USBSIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when device enters Idle mode

0 = Continue module operation in Idle mode

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **UASUSPND:** Automatic Suspend Enable bit

1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 11-5.

0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock

## 14.2 Control Register

**TABLE 14-1: TIMER2 THROUGH TIMER5 REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits       |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | All Resets |
|-----------------------------|---------------------------------|-----------|------------|-------|-------|-------|-------|-------|------|------|-------|------------|------|------|------|------|------|------|------------|
|                             |                                 |           | 31/15      | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7  | 22/6       | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 |            |
| 0800                        | T2CON                           | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON         | —     | SIDL  | —     | —     | —     | —    | —    | TGATE | TCKPS<2:0> |      |      | T32  | —    | TCS  | —    | 0000       |
| 0810                        | TMR2                            | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | TMR2<15:0> |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | 0000       |
| 0820                        | PR2                             | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | PR2<15:0>  |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | FFFF       |
| 0A00                        | T3CON                           | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON         | —     | SIDL  | —     | —     | —     | —    | —    | TGATE | TCKPS<2:0> |      |      | —    | —    | TCS  | —    | 0000       |
| 0A10                        | TMR3                            | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | TMR3<15:0> |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | 0000       |
| 0A20                        | PR3                             | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | PR3<15:0>  |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | FFFF       |
| 0C00                        | T4CON                           | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON         | —     | SIDL  | —     | —     | —     | —    | —    | TGATE | TCKPS<2:0> |      |      | T32  | —    | TCS  | —    | 0000       |
| 0C10                        | TMR4                            | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | TMR4<15:0> |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | 0000       |
| 0C20                        | PR4                             | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | PR4<15:0>  |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | FFFF       |
| 0E00                        | T5CON                           | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | ON         | —     | SIDL  | —     | —     | —     | —    | —    | TGATE | TCKPS<2:0> |      |      | —    | —    | TCS  | —    | 0000       |
| 0E10                        | TMR5                            | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | TMR5<15:0> |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | 0000       |
| 0E20                        | PR5                             | 31:16     | —          | —     | —     | —     | —     | —     | —    | —    | —     | —          | —    | —    | —    | —    | —    | —    | 0000       |
|                             |                                 | 15:0      | PR5<15:0>  |       |       |       |       |       |      |      |       |            |      |      |      |      |      |      | FFFF       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for more information.

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NOTES:

## REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

- bit 5     **ABAUD**: Auto-Baud Enable bit  
          1 = Enable baud rate measurement on the next character – requires reception of Sync character (0x55);  
              cleared by hardware upon completion  
          0 = Baud rate measurement disabled or completed
- bit 4     **RXINV**: Receive Polarity Inversion bit  
          1 = UxRX Idle state is '0'  
          0 = UxRX Idle state is '1'
- bit 3     **BRGH**: High Baud Rate Enable bit  
          1 = High-Speed mode – 4x baud clock enabled  
          0 = Standard Speed mode – 16x baud clock enabled
- bit 2-1   **PDSEL<1:0>**: Parity and Data Selection bits  
          11 = 9-bit data, no parity  
          10 = 8-bit data, odd parity  
          01 = 8-bit data, even parity  
          00 = 8-bit data, no parity
- bit 0     **STSEL**: Stop Selection bit  
          1 = 2 Stop bits  
          0 = 1 Stop bit

**Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.

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**REGISTER 22-4: RTCDATE: RTC DATE VALUE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | YEAR10<3:0>    |                |                |                | YEAR01<3:0>    |                |               |               |
| 23:16     | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | MONTH10<3:0>   |                |                |                | MONTH01<3:0>   |                |               |               |
| 15:8      | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | DAY10<3:0>     |                |                |                | DAY01<3:0>     |                |               |               |
| 7:0       | U-0            | U-0            | U-0            | U-0            | R/W-x          | R/W-x          | R/W-x         | R/W-x         |
|           | —              | —              | —              | —              | WDAY01<3:0>    |                |               |               |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-28 **YEAR10<3:0>**: Binary-Coded Decimal Value of Years bits, 10s place digits

bit 27-24 **YEAR01<3:0>**: Binary-Coded Decimal Value of Years bits, 1s place digit

bit 23-20 **MONTH10<3:0>**: Binary-Coded Decimal Value of Months bits, 10s place digits; contains a value of 0 or 1

bit 19-16 **MONTH01<3:0>**: Binary-Coded Decimal Value of Months bits, 1s place digit; contains a value from 0 to 9

bit 15-12 **DAY10<3:0>**: Binary-Coded Decimal Value of Days bits, 10s place digits; contains a value from 0 to 3

bit 11-8 **DAY01<3:0>**: Binary-Coded Decimal Value of Days bits, 1s place digit; contains a value from 0 to 9

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **WDAY01<3:0>**: Binary-Coded Decimal Value of Weekdays bits, 1s place digit; contains a value from 0 to 6

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

## 23.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

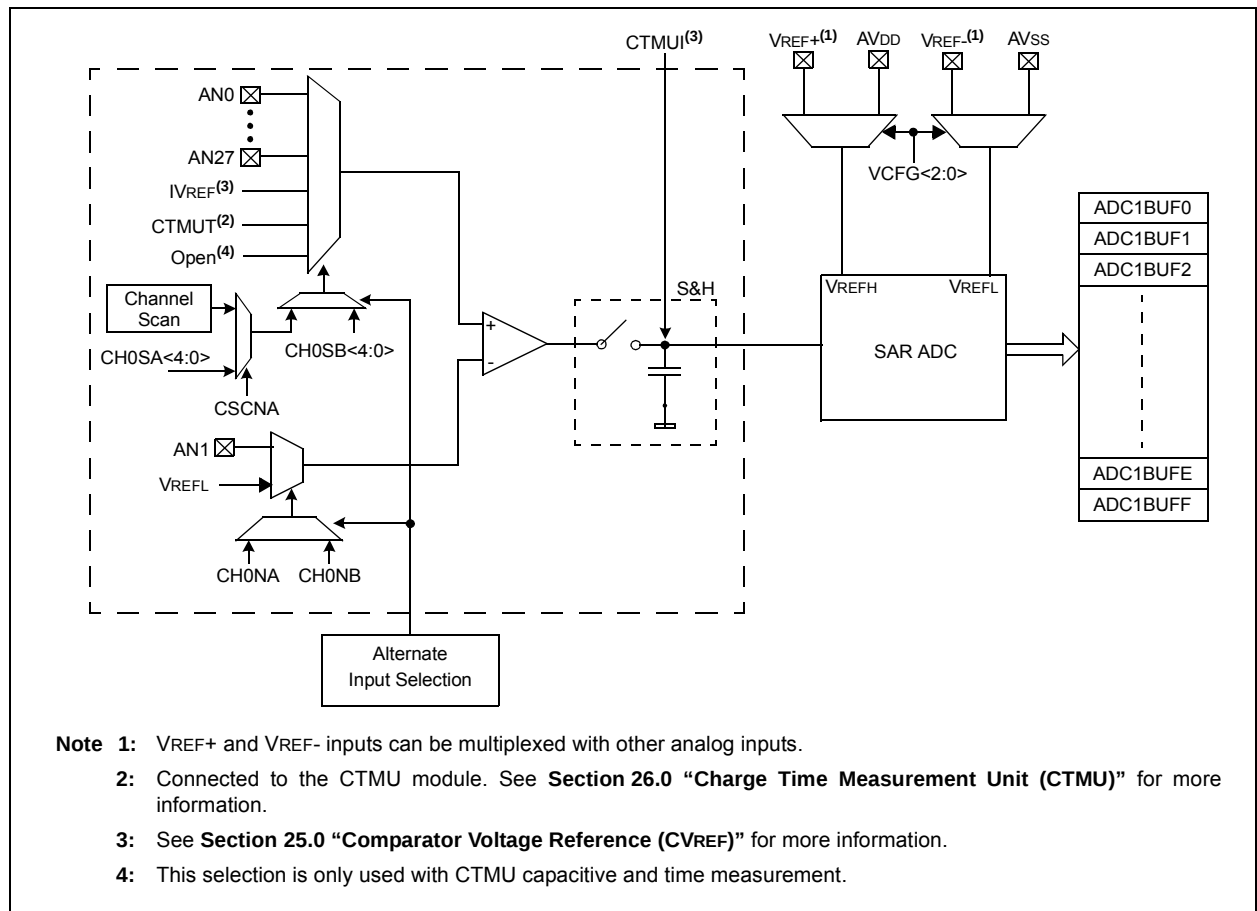
**Note:** This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed
- Up to 28 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during CPU Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 23-1. The 10-bit ADC has up to 28 analog input pins, designated AN0-AN27. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 23-1: ADC1 MODULE BLOCK DIAGRAM**



## 23.1 Control Registers

**TABLE 23-1: ADC REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register Name          | Bit Range | Bits                               |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | All Resets |
|-----------------------------|------------------------|-----------|------------------------------------|--------|--------|------------|--------|-----------|--------|--------|-----------|--------|-----------|------------|--------|--------|--------|--------|------------|
|                             |                        |           | 31/15                              | 30/14  | 29/13  | 28/12      | 27/11  | 26/10     | 25/9   | 24/8   | 23/7      | 22/6   | 21/5      | 20/4       | 19/3   | 18/2   | 17/1   | 16/0   |            |
| 9000                        | AD1CON1 <sup>(1)</sup> | 31:16     | —                                  | —      | —      | —          | —      | —         | —      | —      | —         | —      | —         | —          | —      | —      | —      | —      | 0000       |
|                             |                        | 15:0      | ON                                 | —      | SIDL   | —          | —      | FORM<2:0> |        |        | SSRC<2:0> |        |           | CLRASAM    | —      | ASAM   | SAMP   | DONE   | 0000       |
| 9010                        | AD1CON2 <sup>(1)</sup> | 31:16     | —                                  | —      | —      | —          | —      | —         | —      | —      | —         | —      | —         | —          | —      | —      | —      | —      | 0000       |
|                             |                        | 15:0      | VCFG<2:0>                          |        |        | OFFCAL     | —      | CSCNA     | —      | —      | BUFS      | —      | SMPI<3:0> |            |        |        | BUFM   | ALTS   | 0000       |
| 9020                        | AD1CON3 <sup>(1)</sup> | 31:16     | —                                  | —      | —      | —          | —      | —         | —      | —      | —         | —      | —         | —          | —      | —      | —      | —      | 0000       |
|                             |                        | 15:0      | ADRC                               | —      | —      | SAMC<4:0>  |        |           |        |        | ADCS<7:0> |        |           |            |        |        |        |        | 0000       |
| 9040                        | AD1CHS <sup>(1)</sup>  | 31:16     | CH0NB                              | —      | —      | CH0SB<4:0> |        |           |        |        | CH0NA     | —      | —         | CH0SA<4:0> |        |        |        |        | 0000       |
|                             |                        | 15:0      | —                                  | —      | —      | —          | —      | —         | —      | —      | —         | —      | —         | —          | —      | —      | —      | —      | 0000       |
| 9050                        | AD1CSSL <sup>(1)</sup> | 31:16     | —                                  | CSSL30 | CSSL29 | CSSL28     | CSSL27 | CSSL26    | CSSL25 | CSSL24 | CSSL23    | CSSL22 | CSSL21    | CSSL20     | CSSL19 | CSSL18 | CSSL17 | CSSL16 | 0000       |
|                             |                        | 15:0      | CSSL15                             | CSSL14 | CSSL13 | CSSL12     | CSSL11 | CSSL10    | CSSL9  | CSSL8  | CSSL7     | CSSL6  | CSSL5     | CSSL4      | CSSL3  | CSSL2  | CSSL1  | CSSL0  | 0000       |
| 9070                        | ADC1BUF0               | 31:16     | ADC Result Word 0 (ADC1BUF0<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 9080                        | ADC1BUF1               | 31:16     | ADC Result Word 1 (ADC1BUF1<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 9090                        | ADC1BUF2               | 31:16     | ADC Result Word 2 (ADC1BUF2<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90A0                        | ADC1BUF3               | 31:16     | ADC Result Word 3 (ADC1BUF3<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90B0                        | ADC1BUF4               | 31:16     | ADC Result Word 4 (ADC1BUF4<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90C0                        | ADC1BUF5               | 31:16     | ADC Result Word 5 (ADC1BUF5<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90D0                        | ADC1BUF6               | 31:16     | ADC Result Word 6 (ADC1BUF6<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90E0                        | ADC1BUF7               | 31:16     | ADC Result Word 7 (ADC1BUF7<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 90F0                        | ADC1BUF8               | 31:16     | ADC Result Word 8 (ADC1BUF8<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
| 9100                        | ADC1BUF9               | 31:16     | ADC Result Word 9 (ADC1BUF9<31:0>) |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |
|                             |                        | 15:0      |                                    |        |        |            |        |           |        |        |           |        |           |            |        |        |        |        | 0000       |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 “CLR, SET, and INV Registers” for details.

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## REGISTER 23-2: AD1CON2: ADC CONTROL REGISTER 2

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|-----------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|---------------|
| 31:24     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 23:16     | U-0            | U-0            | U-0            | U-0            | U-0            | U-0            | U-0           | U-0           |
|           | —              | —              | —              | —              | —              | —              | —             | —             |
| 15:8      | R/W-0          | R/W-0          | R/W-0          | R/W-0          | U-0            | R/W-0          | U-0           | U-0           |
|           | VCFG<2:0>      |                |                | OFFCAL         | —              | CSCNA          | —             | —             |
| 7:0       | R-0            | U-0            | R/W-0          | R/W-0          | R/W-0          | R/W-0          | R/W-0         | R/W-0         |
|           | BUFS           | —              | SMPI<3:0>      |                |                |                | BUFM          | ALTS          |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

|     | VREFH              | VREFL              |
|-----|--------------------|--------------------|
| 000 | AVDD               | AVss               |
| 001 | External VREF+ pin | AVss               |
| 010 | AVDD               | External VREF- pin |
| 011 | External VREF+ pin | External VREF- pin |
| 1XX | AVDD               | AVss               |

bit 12 **OFFCAL:** Input Offset Calibration Mode Select bit

1 = Enable Offset Calibration mode

Positive and negative inputs of the sample and hold amplifier are connected to VREFL

0 = Disable Offset Calibration mode

The inputs to the sample and hold amplifier are controlled by AD1CHS or AD1CSSL

bit 11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scan inputs

0 = Do not scan inputs

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **BUFS:** Buffer Fill Status bit

Only valid when BUFM = 1.

1 = ADC is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7

0 = ADC is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF

bit 6 **Unimplemented:** Read as '0'

bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits

1111 = Interrupts at the completion of conversion for each 16<sup>th</sup> sample/convert sequence

1110 = Interrupts at the completion of conversion for each 15<sup>th</sup> sample/convert sequence

.

.

.

0001 = Interrupts at the completion of conversion for each 2<sup>nd</sup> sample/convert sequence

0000 = Interrupts at the completion of conversion for each sample/convert sequence

bit 1 **BUFM:** ADC Result Buffer Mode Select bit

1 = Buffer configured as two 8-word buffers, ADC1BUF7-ADC1BUF0, ADC1BUFF-ADC1BUF8

0 = Buffer configured as one 16-word buffer ADC1BUFF-ADC1BUF0

bit 0 **ALTS:** Alternate Input Sample Mode Select bit

1 = Uses Sample A input multiplexer settings for first sample, then alternates between Sample B and Sample A input multiplexer settings for all subsequent samples

0 = Always use Sample A input multiplexer settings

## 26.1 Control Register

**TABLE 26-1: CTMU REGISTER MAP**

| Virtual Address<br>(BF80_#) | Register<br>Name <sup>(1)</sup> | Bit Range | Bits    |         |              |       |       |          |          |          |            |         |              |      |      |      |           | All Resets |      |
|-----------------------------|---------------------------------|-----------|---------|---------|--------------|-------|-------|----------|----------|----------|------------|---------|--------------|------|------|------|-----------|------------|------|
|                             |                                 |           | 31/15   | 30/14   | 29/13        | 28/12 | 27/11 | 26/10    | 25/9     | 24/8     | 23/7       | 22/6    | 21/5         | 20/4 | 19/3 | 18/2 | 17/1      |            | 16/0 |
| A200                        | CTMUCON                         | 31:16     | EDG1MOD | EDG1POL | EDG1SEL<3:0> |       |       |          | EDG2STAT | EDG1STAT | EDG2MOD    | EDG2POL | EDG2SEL<3:0> |      |      |      | —         | —          | 0000 |
|                             |                                 | 15:0      | ON      | —       | CTMUSIDL     | TGEN  | EDGEN | EDGSEQEN | IDISSEN  | CTTRIG   | ITRIM<5:0> |         |              |      |      |      | IRNG<1:0> |            | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 “CLR, SET, and INV Registers”** for more information.

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**TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS                             |                        |         | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |                                           |
|------------------------------------------------|------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| Parameter No.                                  | Typical <sup>(3)</sup> | Maximum | Units                                                                                                                                                                                                    | Conditions                                |
| <b>Operating Current (IDD)<sup>(1,2)</sup></b> |                        |         |                                                                                                                                                                                                          |                                           |
| DC20                                           | 2.5                    | 4       | mA                                                                                                                                                                                                       | 4 MHz                                     |
| DC21                                           | 6                      | 9       | mA                                                                                                                                                                                                       | 10 MHz <b>(Note 4)</b>                    |
| DC22                                           | 11                     | 17      | mA                                                                                                                                                                                                       | 20 MHz <b>(Note 4)</b>                    |
| DC23                                           | 21                     | 32      | mA                                                                                                                                                                                                       | 40 MHz <b>(Note 4)</b>                    |
| DC24                                           | 30                     | 45      | mA                                                                                                                                                                                                       | 60 MHz <b>(Note 4)</b>                    |
| DC25                                           | 40                     | 60      | mA                                                                                                                                                                                                       | 80 MHz                                    |
| DC25a                                          | 50                     | 75      | mA                                                                                                                                                                                                       | 100 MHz, -40°C ≤ TA ≤ +85°C               |
| DC25c                                          | 72                     | 84      | mA                                                                                                                                                                                                       | 120 MHz, 0°C ≤ TA ≤ +70°C                 |
| DC26                                           | 100                    | —       | μA                                                                                                                                                                                                       | +25°C, 3.3V LPRC (31 kHz) <b>(Note 4)</b> |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 7, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating (ON bit = 0), but the associated PMD bit is clear
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to Vss
- $\overline{\text{MCLR}} = \text{VDD}$
- CPU executing while(1) statement from Flash
- RTCC and JTAG are disabled

**3:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**4:** This parameter is characterized, but not tested in manufacturing.

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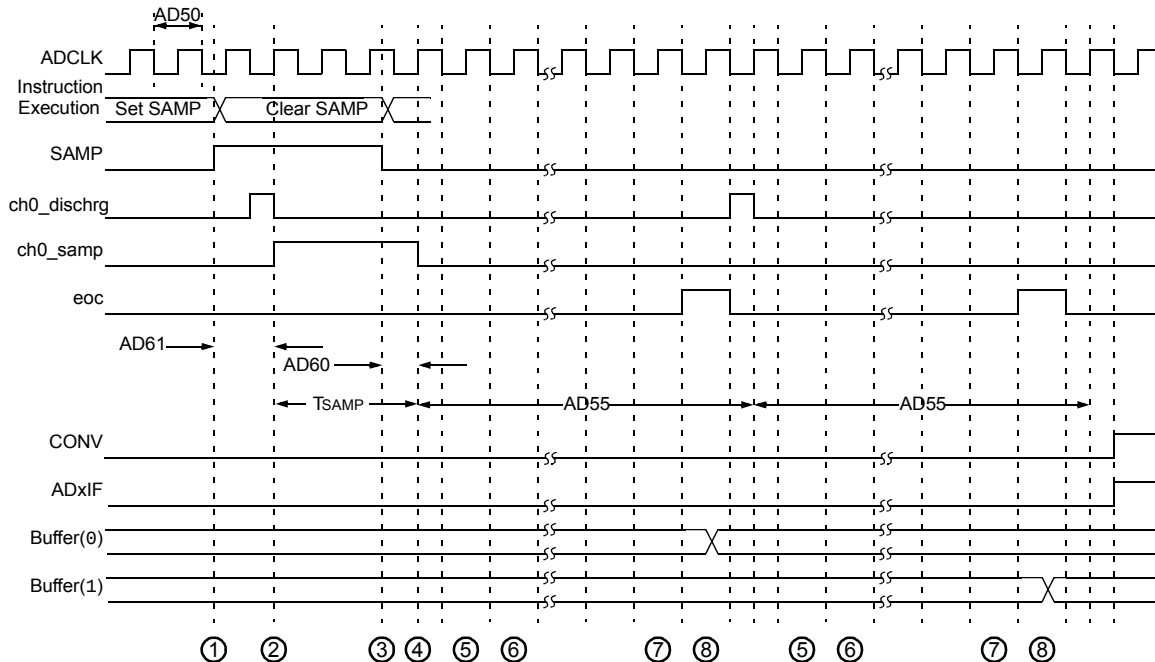
**TABLE 31-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE) (CONTINUED)**

| AC CHARACTERISTICS |         |                          |                     | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |      |       |                                                                             |
|--------------------|---------|--------------------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------|-----------------------------------------------------------------------------|
| Param. No.         | Symbol  | Characteristics          |                     | Min.                                                                                                                                                                                                     | Max. | Units | Conditions                                                                  |
| IS34               | THD:STO | Stop Condition Hold Time | 100 kHz mode        | 4000                                                                                                                                                                                                     | —    | ns    | —                                                                           |
|                    |         |                          | 400 kHz mode        | 600                                                                                                                                                                                                      | —    | ns    |                                                                             |
|                    |         |                          | 1 MHz mode (Note 1) | 250                                                                                                                                                                                                      |      | ns    |                                                                             |
| IS40               | TAA:SCL | Output Valid from Clock  | 100 kHz mode        | 0                                                                                                                                                                                                        | 3500 | ns    | —                                                                           |
|                    |         |                          | 400 kHz mode        | 0                                                                                                                                                                                                        | 1000 | ns    |                                                                             |
|                    |         |                          | 1 MHz mode (Note 1) | 0                                                                                                                                                                                                        | 350  | ns    |                                                                             |
| IS45               | TBF:SDA | Bus Free Time            | 100 kHz mode        | 4.7                                                                                                                                                                                                      | —    | μs    | The amount of time the bus must be free before a new transmission can start |
|                    |         |                          | 400 kHz mode        | 1.3                                                                                                                                                                                                      | —    | μs    |                                                                             |
|                    |         |                          | 1 MHz mode (Note 1) | 0.5                                                                                                                                                                                                      | —    | μs    |                                                                             |
| IS50               | CB      | Bus Capacitive Loading   |                     | —                                                                                                                                                                                                        | 400  | pF    | —                                                                           |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

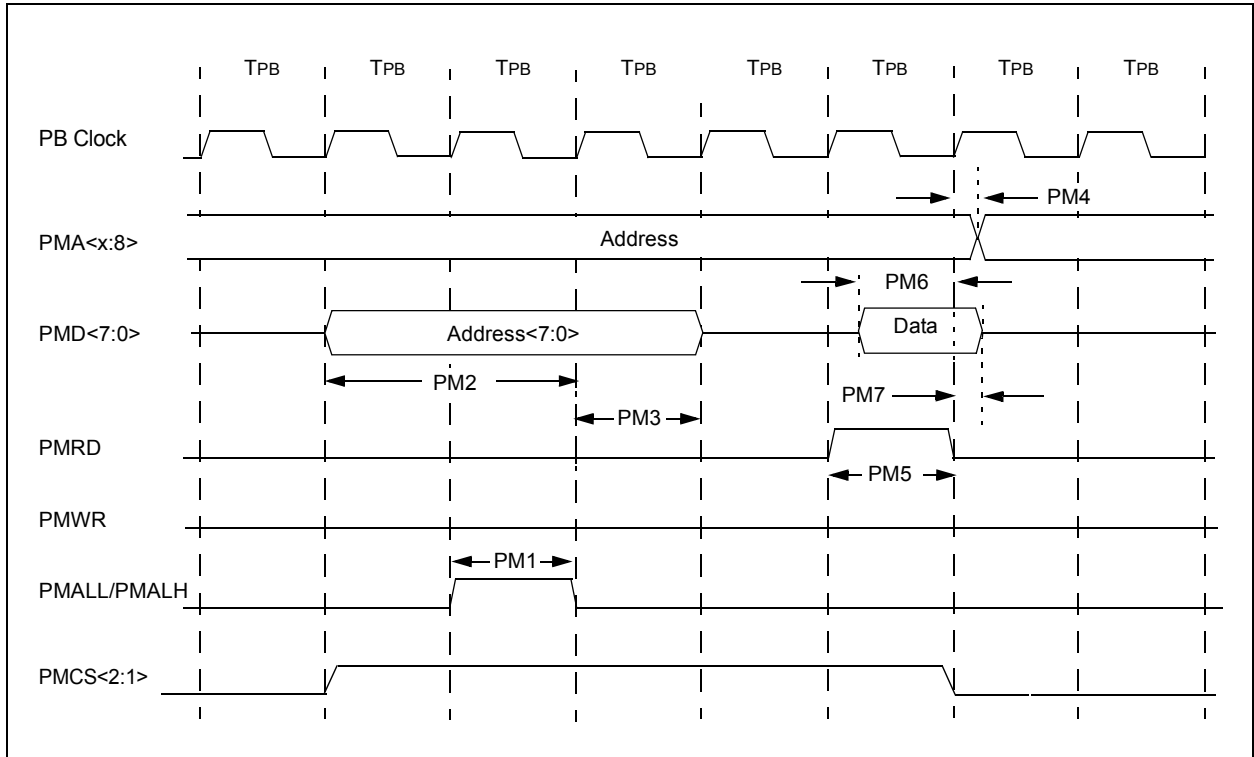
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**FIGURE 31-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)**



- ① – Software sets ADxCON. SAMP to start sampling.
- ② – Sampling starts after discharge period. Tsamp is described in **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104) in the “PIC32 Family Reference Manual”.
- ③ – Software clears ADxCON. SAMP to start conversion.
- ④ – Sampling ends, conversion sequence starts.
- ⑤ – Convert bit 9.
- ⑥ – Convert bit 8.
- ⑦ – Convert bit 0.
- ⑧ – One TAD for end of conversion.

**FIGURE 31-21: PARALLEL MASTER PORT READ TIMING DIAGRAM**



**TABLE 31-39: PARALLEL MASTER PORT READ TIMING REQUIREMENTS**

| AC CHARACTERISTICS |         |                                                                | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for Commercial<br>$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp |       |      |       |            |
|--------------------|---------|----------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|------------|
| Param. No.         | Symbol  | Characteristics <sup>(1)</sup>                                 | Min.                                                                                                                                                                                                                                                                                                                    | Typ.  | Max. | Units | Conditions |
| PM1                | TLAT    | PMALL/PMALH Pulse Width                                        | —                                                                                                                                                                                                                                                                                                                       | 1 TPB | —    | —     | —          |
| PM2                | TADSU   | Address Out Valid to PMALL/PMALH Invalid (address setup time)  | —                                                                                                                                                                                                                                                                                                                       | 2 TPB | —    | —     | —          |
| PM3                | TADHOLD | PMALL/PMALH Invalid to Address Out Invalid (address hold time) | —                                                                                                                                                                                                                                                                                                                       | 1 TPB | —    | —     | —          |
| PM4                | TAHOLD  | PMRD Inactive to Address Out Invalid (address hold time)       | 5                                                                                                                                                                                                                                                                                                                       | —     | —    | ns    | —          |
| PM5                | TRD     | PMRD Pulse Width                                               | —                                                                                                                                                                                                                                                                                                                       | 1 TPB | —    | —     | —          |
| PM6                | TDSU    | PMRD or PMENB Active to Data In Valid (data setup time)        | 15                                                                                                                                                                                                                                                                                                                      | —     | —    | ns    | —          |
| PM7                | TDHOLD  | PMRD or PMENB Inactive to Data In Invalid (data hold time)     | 1 TPB                                                                                                                                                                                                                                                                                                                   | —     | —    | —     | PMP Clock  |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

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**TABLE 31-42: CTMU CURRENT SOURCE SPECIFICATIONS**

| DC CHARACTERISTICS         |        |                                                    | Standard Operating Conditions: 2.3V to 3.6V<br>(unless otherwise stated)<br>Operating temperature 0°C ≤ TA ≤ +70°C for Commercial<br>-40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp |       |      |       |                                   |
|----------------------------|--------|----------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|-------|-----------------------------------|
| Param No.                  | Symbol | Characteristic                                     | Min.                                                                                                                                                                                                     | Typ.  | Max. | Units | Conditions                        |
| <b>CTMU CURRENT SOURCE</b> |        |                                                    |                                                                                                                                                                                                          |       |      |       |                                   |
| CTMUI1                     | IOUT1  | Base Range <sup>(1)</sup>                          | —                                                                                                                                                                                                        | 0.55  | —    | μA    | CTMUICON<9:8> = 01                |
| CTMUI2                     | IOUT2  | 10x Range <sup>(1)</sup>                           | —                                                                                                                                                                                                        | 5.5   | —    | μA    | CTMUICON<9:8> = 10                |
| CTMUI3                     | IOUT3  | 100x Range <sup>(1)</sup>                          | —                                                                                                                                                                                                        | 55    | —    | μA    | CTMUICON<9:8> = 11                |
| CTMUI4                     | IOUT4  | 1000x Range <sup>(1)</sup>                         | —                                                                                                                                                                                                        | 550   | —    | μA    | CTMUICON<9:8> = 00                |
| CTMUFV1                    | VF     | Temperature Diode Forward Voltage <sup>(1,2)</sup> | —                                                                                                                                                                                                        | 0.598 | —    | V     | TA = +25°C,<br>CTMUICON<9:8> = 01 |
|                            |        |                                                    | —                                                                                                                                                                                                        | 0.658 | —    | V     | TA = +25°C,<br>CTMUICON<9:8> = 10 |
|                            |        |                                                    | —                                                                                                                                                                                                        | 0.721 | —    | V     | TA = +25°C,<br>CTMUICON<9:8> = 11 |
| CTMUFV2                    | VFVR   | Temperature Diode Rate of Change <sup>(1,2)</sup>  | —                                                                                                                                                                                                        | -1.92 | —    | mV/°C | CTMUICON<9:8> = 01                |
|                            |        |                                                    | —                                                                                                                                                                                                        | -1.74 | —    | mV/°C | CTMUICON<9:8> = 10                |
|                            |        |                                                    | —                                                                                                                                                                                                        | -1.56 | —    | mV/°C | CTMUICON<9:8> = 11                |

**Note 1:** Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

**2:** Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC module configured for conversion speed of 500 ksps
- All PMD bits are cleared (PMDx = 0)
- Executing a while(1) statement
- Device operating from the FRC with no PLL

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