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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFTLA Dual Rows, Exposed Pad
Supplier Device Package	124-VTLA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx350f128lt-v-tl

TABLE 5: PIN NAMES FOR 100-PIN DEVICES

100-PIN TQFP (TOP VIEW)(1,2)

PIC32MX430F064L
PIC32MX450F128L
PIC32MX450F256L
PIC32MX470F512L

100

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RG15	36	VSS
2	VDD	37	VDD
3	AN22/RPE5/PMD5/RE5	38	TCK/CTED2/RA1
4	AN23/PMD6/RE6	39	RPF13/RF13
5	AN27/PMD7/RE7	40	RPF12/RF12
6	RPC1/RC1	41	AN12/PMA11/RB12
7	RPC2/RC2	42	AN13/PMA10/RB13
8	RPC3/RC3	43	AN14/RPB14/CTED5/PMA1/RB14
9	RPC4/CTED7/RC4	44	AN15/RPB15/OCFB/CTED6/PMA0/RB15
10	AN16/C1IND/RPG6/SCK2/PMA5/RG6	45	VSS
11	AN17/C1INC/RPG7/PMA4/RG7	46	VDD
12	AN18/C2IND/RPG8/PMA3/RG8	47	RPD14/RD14
13	$\overline{\text{MCLR}}$	48	RPD15/RD15
14	AN19/C2INC/RPG9/PMA2/RG9	49	RPF4/PMA9/RF4
15	VSS	50	RPF5/PMA8/RF5
16	VDD	51	USBID/RF3
17	TMS/CTED1/RA0	52	RPF2/RF2
18	RPE8/RE8	53	RPF8/RF8
19	RPE9/RE9	54	VBUS
20	AN5/C1INA/RPB5/VBUSON/RB5	55	VUSB3V3
21	AN4/C1INB/RB4	56	D-
22	PGED3/AN3/C2INA/RPB3/RB3	57	D+
23	PGEC3/AN2/C2INB/RPB2/CTED13/RB2	58	SCL2/RA2
24	PGEC1/AN1/RPB1/CTED12/RB1	59	SDA2/RA3
25	PGED1/AN0/RPB0/RB0	60	TDI/CTED9/RA4
26	PGEC2/AN6/RPB6/RB6	61	TDO/RA5
27	PGED2/AN7/RPB7/CTED3/RB7	62	VDD
28	VREF-/CVREF-/PMA7/RA9	63	OSC1/CLKI/RC12
29	VREF+/CVREF+/PMA6/RA10	64	OSC2/CLKO/RC15
30	AVDD	65	VSS
31	AVSS	66	SCL1/RPA14/RA14
32	AN8/RPB8/CTED10/RB8	67	SDA1/RPA15/RA15
33	AN9/RPB9/CTED4/RB9	68	RPD8/RTCC/RD8
34	CVREFOUT/AN10/RPB10/CTED11/PMA13/RB10	69	RPD9/RD9
35	AN11/PMA12/RB11	70	RPD10/SCK1/PMCS2/RD10

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 12.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RBx-RGx) can be used as a change notification pin (CNBx-CNGx). See **Section 12.0 "I/O Ports"** for more information.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA			
CTED4	22	33	B19	I	ST	CTMU External Edge Input 4
CTED5	29	43	B24	I	ST	CTMU External Edge Input 5
CTED6	30	44	A29	I	ST	CTMU External Edge Input 6
CTED7	—	9	B5	I	ST	CTMU External Edge Input 7
CTED8	—	92	A62	I	ST	CTMU External Edge Input 8
CTED9	—	60	A40	I	ST	CTMU External Edge Input 9
CTED10	21	32	A23	I	ST	CTMU External Edge Input 10
CTED11	23	34	A24	I	ST	CTMU External Edge Input 11
CTED12	15	24	A15	I	ST	CTMU External Edge Input 12
CTED13	14	23	B13	I	ST	CTMU External Edge Input 13
$\overline{MCLR}$	7	13	B7	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AVDD	19	30	A22	P	P	Positive supply for analog modules. This pin must be connected at all times.
AVSS	20	31	B18	P	P	Ground reference for analog modules
VDD	10, 26, 38, 57	2, 16, 37, 46, 62, 86	B1, A10, A14, B21, A30, A41, A48, A59, B53	P	—	Positive supply for peripheral logic and I/O pins
VCAP	56	85	B48	P	—	Capacitor for Internal Voltage Regulator
VSS	9, 25, 41	15, 36, 45, 65, 75	A3, B8, B12, A25, B25, A43, B41, A63	P	—	Ground reference for logic and I/O pins
VREF+	16	29	B17	I	Analog	Analog Voltage Reference (High) Input
VREF-	15	28	A21	I	Analog	Analog Voltage Reference (Low) Input

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
TTL = TTL input buffer

Note 1: This pin is only available on devices without a USB module.
2: This pin is only available on devices with a USB module.
3: This pin is not available on 64-pin devices.

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32® architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e®, is also available by accessing the CP0 registers, listed in Table 3-2.

TABLE 3-2: COPROCESSOR 0 REGISTERS

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr(1)	Reports the address for the most recent address-related exception.
9	Count(1)	Processor cycle count.
10	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
11	Compare(1)	Timer interrupt control.
12	Status(1)	Processor status and control.
12	IntCtl(1)	Interrupt system status and control.
12	SRSCtl(1)	Shadow register set status and control.
12	SRSMap(1)	Provides mapping from vectored interrupt to a shadow set.
13	Cause(1)	Cause of last general exception.
14	EPC(1)	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration register 1.
16	Config2	Configuration register 2.
16	Config3	Configuration register 3.
17-22	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
23	Debug(2)	Debug control and exception status.
24	DEPC(2)	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX330/350/370/430/450/470 family core.
30	ErrorEPC(1)	Program counter at last error.
31	DESAVE(2)	Debug handler scratchpad register.

Note 1: Registers used in exception processing.

2: Registers used during debug.

7.1 Interrupts Control Registers

TABLE 7-2: INTERRUPT REGISTER MAP

Virtual Address (BF88_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
1000	INTCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SS0	0000
		15:0	—	—	—	MVEC	—	TPC<2:0>			—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
1010	INTSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	SRIPL<2:0>			—	—	VEC<5:0>						0000
1020	IPTMR	31:16	IPTMR<31:0>																0000
		15:0																	0000
1030	IFS0	31:16	FCEIF	RTCCIF	FSCMIF	AD1IF	OC5IF	IC5IF	IC5EIF	T5IF	INT4IF	OC4IF	IC4IF	IC4EIF	T4IF	INT3IF	OC3IF	IC3IF	0000
		15:0	IC3EIF	T3IF	INT2IF	OC2IF	IC2IF	IC2EIF	T2IF	INT1IF	OC1IF	IC1IF	IC1EIF	T1IF	INT0IF	CS1IF	CS0IF	CTIF	0000
1040	IFS1	31:16	U3RXIF	U3EIF	I2C2MIF	I2C2SIF	I2C2BIF	U2TXIF	U2RXIF	U2EIF	SPI2TXIF	SPI2RXIF	SPI2EIF	PMPEIF	PMPIF	CNGIF	CNFIF	CNEIF	0000
		15:0	CNDIF	CNCIF	CNBIF	CNAIF	I2C1MIF	I2C1SIF	I2C1BIF	U1TXIF	U1RXIF	U1EIF	SPI1TXIF	SPI1RXIF	SPI1EIF	USBIF(2)	CMP2IF	CMP1IF	0000
1050	IFS2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMA3IF	DMA2IF	DMA1IF	DMA0IF	CTMUIF	U5TXIF(1)	U5RXIF(1)	U5EIF(1)	U4TXIF	U4RXIF	U4EIF	U3TXIF	0000
1060	IEC0	31:16	FCEIE	RTCCIE	FSCMIE	AD1IE	OC5IE	IC5IE	IC5EIE	T5IE	INT4IE	OC4IE	IC4IE	IC4EIE	T4IE	INT3IE	OC3IE	IC3IE	0000
		15:0	IC3EIE	T3IE	INT2IE	OC2IE	IC2IE	IC2EIE	T2IE	INT1IE	OC1IE	IC1IE	IC1EIE	T1IE	INT0IE	CS1IE	CS0IE	CTIE	0000
1070	IEC1	31:16	U3RXIE	U3EIE	I2C2MIE	I2C2SIE	I2C2BIE	U2TXIE	U2RXIE	U2EIE	SPI2TXIE	SPI2RXIE	SPI2EIE	PMPEIE	PMPIE	CNGIE	CNFIE	CNEIE	0000
		15:0	CNDIE	CNCIE	CNBIE	CNAIE	I2C1MIE	I2C1SIE	I2C1BIE	U1TXIE	U1RXIE	U1EIE	SPI1TXIE	SPI1RXIE	SPI1EIE	USBIE(2)	CMP2IE	CMP1IE	0000
1080	IEC2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	DMA3IE	DMA2IE	DMA1IE	DMA0IE	CTMUIE	U5TXIE(1)	U5RXIE(1)	U5EIE(1)	U4TXIE	U4RXIE	U4EIE	U3TXIE	0000
1090	IPC0	31:16	—	—	—	INT0IP<2:0>			INT0IS<1:0>		—	—	—	CS1IP<2:0>			CS1IS<1:0>		0000
		15:0	—	—	—	CS0IP<2:0>			CS0IS<1:0>		—	—	—	CTIP<2:0>			CTIS<1:0>		0000
10A0	IPC1	31:16	—	—	—	INT1IP<2:0>			INT1IS<1:0>		—	—	—	OC1IP<2:0>			OC1IS<1:0>		0000
		15:0	—	—	—	IC1IP<2:0>			IC1IS<1:0>		—	—	—	T1IP<2:0>			T1IS<1:0>		0000
10B0	IPC2	31:16	—	—	—	INT2IP<2:0>			INT2IS<1:0>		—	—	—	OC2IP<2:0>			OC2IS<1:0>		0000
		15:0	—	—	—	IC2IP<2:0>			IC2IS<1:0>		—	—	—	T2IP<2:0>			T2IS<1:0>		0000
10C0	IPC3	31:16	—	—	—	INT3IP<2:0>			INT3IS<1:0>		—	—	—	OC3IP<2:0>			OC3IS<1:0>		0000
		15:0	—	—	—	IC3IP<2:0>			IC3IS<1:0>		—	—	—	T3IP<2:0>			T3IS<1:0>		0000
10D0	IPC4	31:16	—	—	—	INT4IP<2:0>			INT4IS<1:0>		—	—	—	OC4IP<2:0>			OC4IS<1:0>		0000
		15:0	—	—	—	IC4IP<2:0>			IC4IS<1:0>		—	—	—	T4IP<2:0>			T4IS<1:0>		0000
10E0	IPC5	31:16	—	—	—	AD1IP<2:0>			AD1IS<1:0>		—	—	—	OC5IP<2:0>			OC5IS<1:0>		0000
		15:0	—	—	—	IC5IP<2:0>			IC5IS<1:0>		—	—	—	T5IP<2:0>			T5IS<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This bit is only available on 100-pin devices.

2: This bit is only implemented on devices with a USB module.

REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	SRIPL<2:0>(1)		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	VEC<5:0>(1)					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 **Unimplemented:** Read as '0'

bit 10-8 **SRIPL<2:0>:** Requested Priority Level bits(1)

111-000 = The priority level of the latest interrupt presented to the CPU

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **VEC<5:0>:** Interrupt Vector bits(1)

11111-00000 = The interrupt vector that is presented to the CPU

Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<31:24>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<23:16>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IPTMR<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits
Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS9	IFS8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IFS7	IFS6	IFS5	IFS4	IFS3	IFS2	IFS1	IFS0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IFS31-IFS0:** Interrupt Flag Status bits
1 = Interrupt request has occurred
0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	IEC0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **IEC31-IEC0:** Interrupt Enable bits
1 = Interrupt is enabled
0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

8.1 Oscillator Control Registers

TABLE 8-1: OSCILLATOR CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>			x1xx(2)
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK(4)	SLOCK	SLPEN	CF	UFRCEN(4)	SOSCEN	OSWEN	xxxx(2)
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
F020	REFOCON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
F030	REFOTRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on devices with a USB module.

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 3-0 **ROSEL<3:0>:** Reference Clock Source Select bits(1)

1111 = Reserved; do not use
•
•
•
1001 = Reserved; do not use
1000 = REFCLKI
0111 = System PLL output
0110 = USB PLL output
0101 = SOSC
0100 = LPRC
0011 = FRC
0010 = POSC
0001 = PBCLK
0000 = SYSCLK

Note 1: The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.

2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.

3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

TABLE 10-3: DMA CHANNEL 0 THROUGH CHANNEL 3 REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3280	DCH2CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3290	DCH2DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000
32A0	DCH3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHBUSY	—	—	—	—	—	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>		0000
32B0	DCH3ECON	31:16	—	—	—	—	—	—	—	—	CHAIRQ<7:0>								00FF
		15:0	CHSIRQ<7:0>								CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—	—	FFF8
32C0	DCH3INT	31:16	—	—	—	—	—	—	—	—	CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	—	—	—	—	—	—	—	—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
32D0	DCH3SSA	31:16	CHSSA<31:0>																0000
		15:0																	0000
32E0	DCH3DSA	31:16	CHDSA<31:0>																0000
		15:0																	0000
32F0	DCH3SSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSSIZ<15:0>																0000
3300	DCH3DSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDSIZ<15:0>																0000
3310	DCH3SPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHSPTR<15:0>																0000
3320	DCH3DPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHDPTR<15:0>																0000
3330	DCH3CSIZ	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCSIZ<15:0>																0000
3340	DCH3CPTR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	CHCPTR<15:0>																0000
3350	DCH3DAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	CHPDAT<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 11-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	FRMH<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 **Unimplemented:** Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 11-15: U1TOK: USB TOKEN REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PID<3:0>(1)				EP<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits(1)
0001 = OUT (TX) token type transaction
1001 = IN (RX) token type transaction
1101 = SETUP (TX) token type transaction
Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

13.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (SOSC) for Real-Time Clock (RTC) applications.

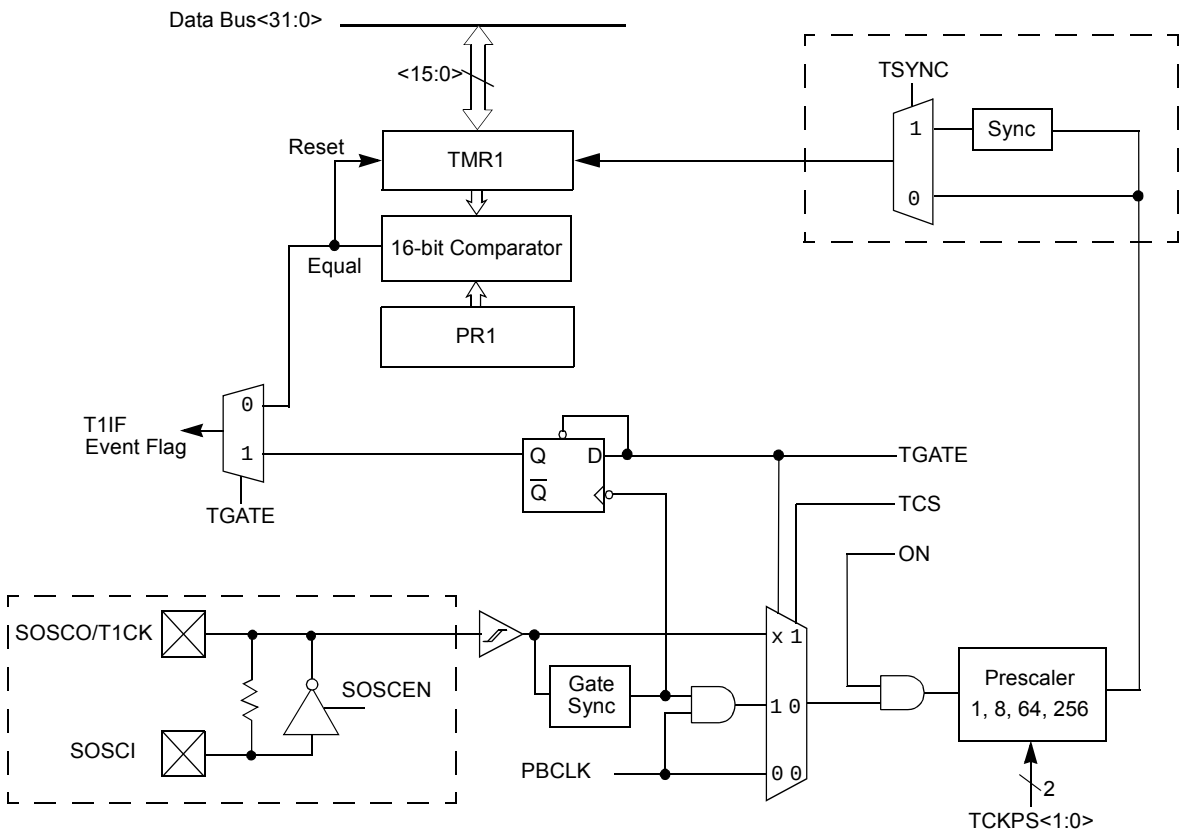
The following modes are supported:

- Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

13.1 Additional Supported Features

- Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the SOSC to function as a Real-Time Clock (RTC)

FIGURE 13-1: TIMER1 BLOCK DIAGRAM



Note: The default state of the SOSCEN (OSCCON<1>) bit during a device Reset is controlled by the FSOSCEN bit in Configuration Word, DEVCFG1.

24.1 Control Registers

TABLE 24-1: COMPARATOR REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		E1C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		E1C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	C2OUT	C1OUT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 12.2 "CLR, SET, and INV Registers"** for more information.

REGISTER 26-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 must occur before Edge 2 can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(2)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** Trigger Control bit
1 = Trigger output is enabled
0 = Trigger output is disabled

bit 7-2 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current
011110
•
•
•
000001 = Minimum positive change from nominal current
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current
•
•
•
100010
100001 = Maximum negative change from nominal current

bit 1-0 **IRNG<1:0>:** Current Range Select bits(3)
11 = 100 times base current
10 = 10 times base current
01 = Base current level
00 = 1000 times base current(4)

Note 1: When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.

2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

3: Refer to the CTMU Current Source Specifications (Table 31-42) in **Section 31.0 "Electrical Characteristics"** for current values.

4: This bit setting is not available for the CTMU temperature diode.

TABLE 31-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage**	2.3	—	3.6	V	—
DC12	VDR	**RAM Data Retention Voltage (Note 1)**	1.75	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	1.75	—	2.1	V	—
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.00005	—	0.115	V/μs	—

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 31-32: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typical(2)**	**Max.**	**Units**	**Conditions**
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input	175	—	—	ns	—
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance **(Note 4)**	5	—	25	ns	—
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	Tsck + 20	—	—	ns	—
SP60	TssL2doV	SDOx Data Output Valid after $\overline{SSx}$ Edge	—	—	25	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 40 ns.

4: Assumes 50 pF load on all SPIx pins.

TABLE 31-33: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE) (CONTINUED)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	**Symbol**	**Characteristics**		**Min.(1)**	**Max.**	**Units**	**Conditions**
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TPB * (BRG + 2)	—	ns	—
			400 kHz mode	TPB * (BRG + 2)	—	ns	
			1 MHz mode **(Note 2)**	TPB * (BRG + 2)	—	ns	
IM40	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3500	ns	—
			400 kHz mode	—	1000	ns	—
			1 MHz mode **(Note 2)**	—	350	ns	—
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	The amount of time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode **(Note 2)**	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	—
IM51	TPGD	Pulse Gobbler Delay		52	312	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

TABLE 31-35: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS[5]			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.0	—	AVDD	V	**(Note 1)**
AD05a			2.5	—	3.6	V	VREFH = AVDD **(Note 3)**
AD06	VREFL	Reference Voltage Low	AVSS	—	VREFH – 2.0	V	**(Note 1)**
AD07	VREF	Absolute Reference Voltage (VREFH – VREFL)	2.0	—	AVDD	V	**(Note 3)**
AD08	IREF	Current Drain	—	250 —	400 3	μA μA	ADC operating ADC off
Analog Input							
AD12	VINH-VINL	Full-Scale Input Span	VREFL	—	VREFH	V	—
AD13	VINL	Absolute VINL Input Voltage	AVSS – 0.3	—	AVDD/2	V	—
AD14	VIN	Absolute Input Voltage	AVSS – 0.3	—	AVDD + 0.3	V	—
AD15		Leakage Current	—	+/- 0.001	+/-0.610	μA	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V Source Impedance = 10 kΩ
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	5K	Ω	**(Note 1)**
ADC Accuracy – Measurements with External VREF+/VREF-							
AD20c	Nr	Resolution	10 data bits			bits	—
AD21c	INL	Integral Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD22c	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V **(Note 2)**
AD23c	GERR	Gain Error	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V
AD24n	EOFF	Offset Error	> -1	—	< 1	LSb	VINL = AVSS = 0V, AVDD = 3.3V
AD25c	—	Monotonicity	—	—	—	—	Guaranteed

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for VBORMIN values.

TABLE 31-37: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typical(1)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period(2)	65	—	—	ns	See Table 31-36
Conversion Rate							
AD55	TCONV	Conversion Time	—	12 TAD	—	—	—
AD56	FCNV	Throughput Rate (Sampling Speed)(4)	—	—	1000	ksps	AVDD = 3.0V to 3.6V
			—	—	400	ksps	AVDD = 2.5V to 3.6V
AD57	TSAMP	Sample Time	2 TAD	—	—	—	—
Timing Parameters							
AD60	TPCS	Conversion Start from Sample Trigger(3)	—	1.0 TAD	—	—	Auto-Convert Trigger (SSRC<2:0> = 111) not selected
AD61	TPSS	Sample Start from Setting Sample (SAMP) bit	0.5 TAD	—	1.5 TAD	—	—
AD62	TCSS	Conversion Completion to Sample Start (ASAM = 1)(3)	—	0.5 TAD	—	—	—
AD63	TDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(3)	—	—	2	μs	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures.

3: Characterized by design but not tested.

4: Refer to Table 31-36 for detailed conditions.

FIGURE 31-20: PARALLEL SLAVE PORT TIMING

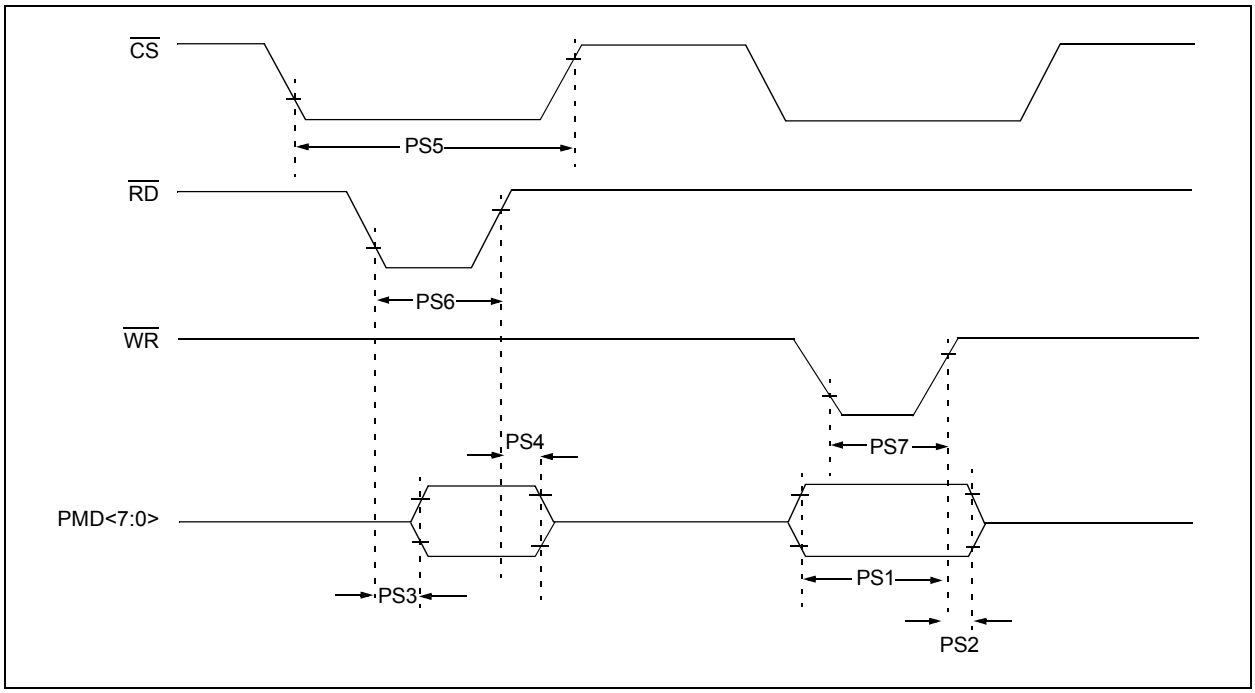


TABLE 31-38: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for Commercial -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param.No.	**Symbol**	**Characteristics(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
PS1	TdtV2wrH	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20	—	—	ns	—
PS2	TwrH2dtI	$\overline{WR}$ or $\overline{CS}$ Inactive to Data-In Invalid (hold time)	40	—	—	ns	—
PS3	TrdL2dtV	$\overline{RD}$ and $\overline{CS}$ Active to Data-Out Valid	—	—	60	ns	—
PS4	TrdH2dtI	$\overline{RD}$ Active or $\overline{CS}$ Inactive to Data-Out Invalid	0	—	10	ns	—
PS5	Tcs	$\overline{CS}$ Active Time	TPB + 40	—	—	ns	—
PS6	TWR	$\overline{WR}$ Active Time	TPB + 25	—	—	ns	—
PS7	TRD	$\overline{RD}$ Active Time	TPB + 25	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.