

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 28x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx350f256h-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note:	To access the following documents, refer								
	to the Documentation > Reference								
	Manuals section of the Microchip PIC32								
	website: http://www.microchip.com/pic32.								

- Section 1. "Introduction" (DS60001127)
- Section 2. "CPU" (DS60001113)
- Section 3. "Memory Organization" (DS60001115)
- Section 4. "Prefetch Cache" (DS60001119)
- Section 5. "Flash Program Memory" (DS60001121)
- Section 6. "Oscillator Configuration" (DS60001112)
- Section 7. "Resets" (DS60001118)
- Section 8. "Interrupt Controller" (DS60001108)
- Section 9. "Watchdog Timer and Power-up Timer" (DS60001114)
- Section 10. "Power-Saving Features" (DS60001130)
- Section 12. "I/O Ports" (DS60001120)
- Section 13. "Parallel Master Port (PMP)" (DS60001128)
- Section 14. "Timers" (DS60001105)
- Section 15. "Input Capture" (DS60001122)
- Section 16. "Output Compare" (DS60001111)
- Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104)
- Section 19. "Comparator" (DS60001110)
- Section 20. "Comparator Voltage Reference (CVREF)" (DS60001109)
- Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107)
- Section 23. "Serial Peripheral Interface (SPI)" (DS60001106)
- Section 24. "Inter-Integrated Circuit (I²C)" (DS60001116)
- Section 27. "USB On-The-Go (OTG)" (DS60001126)
- Section 29. "Real-Time Clock and Calendar (RTCC)" (DS60001125)
- Section 31. "Direct Memory Access (DMA) Controller" (DS60001117)
- Section 32. "Configuration" (DS60001124)
- Section 33. "Programming and Diagnostics" (DS60001129)
- Section 37. "Charge Time Measurement Unit (CTMU)" (DS60001167)

		Pin Numb				-,
Pin Name	64-pin QFN/ TQFP	100-pin TQFP	124-pin VTLA	Pin Type	Buffer Type	Description
RB0	16	25	B14	I/O	ST	
RB1	15	24	A15	I/O	ST	_
RB2	14	23	B13	I/O	ST	
RB3	13	22	A13	I/O	ST	
RB4	12	21	B11	I/O	ST	_
RB5	11	20	A12	I/O	ST	_
RB6	17	26	A20	I/O	ST	_
RB7	18	27	B16	I/O	ST	PORTB is a hidirectional I/O port
RB8	21	32	A23	I/O	ST	
RB9	22	33	B19	I/O	ST	
RB10	23	34	A24	I/O	ST	
RB11	24	35	B20	I/O	ST	
RB12	27	41	B23	I/O	ST	
RB13	28	42	A28	I/O	ST	
RB14	29	43	B24	I/O	ST	
RB15	30	44	A29	I/O	ST	
RC1	-	6	A5	I/O	ST	
RC2	-	7	B4	I/O	ST	
RC3	-	8	A6	I/O	ST	
RC4	-	9	B5	I/O	ST	POPTC is a hidiractional I/O part
RC12	39	63	B34	I/O	ST	
RC13	47	73	A47	I/O	ST	
RC14	48	74	B40	I/O	ST	
RC15	40	64	A42	I/O	ST	
RD0	46	72	B39	I/O	ST	
RD1	49	76	A52	I/O	ST	
RD2	50	77	B42	I/O	ST	
RD3	51	78	A53	I/O	ST	
RD4	52	81	B44	I/O	ST	_
RD5	53	82	A55	I/O	ST	_
RD6	54	83	B45	I/O	ST	_
RD7	55	84	A56	I/O	ST	PORTD is a hidirectional I/O port
RD8	42	68	B37	I/O	ST	
RD9	43	69	A45	I/O	ST	
RD10	44	70	B38	I/O	ST	_
RD11	45	71	A46	I/O	ST	
RD12		79	B43	I/O	ST	
RD13		80	A54	I/O	ST	
RD14		47	B26	I/O	ST	
RD15	_	48	A31	I/O	ST	
Legend:	CMOS = CI ST = Schmi TTL = TTL i	MOS compat itt Trigger inp input buffer	ible input or ou out with CMOS	itput levels	An O :	alog = Analog input P = Power = Output I = Input

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: This pin is only available on devices without a USB module.

2: This pin is only available on devices with a USB module.

3: This pin is not available on 64-pin devices.

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER (CONTINUED)

- bit 18-16 PLLMULT<2:0>: Phase-Locked Loop (PLL) Multiplier bits
 - 111 = Clock is multiplied by 24
 - 110 = Clock is multiplied by 21
 - 101 = Clock is multiplied by 20
 - 100 = Clock is multiplied by 19
 - 011 = Clock is multiplied by 18
 - 010 = Clock is multiplied by 17
 - 001 = Clock is multiplied by 16
 - 000 =Clock is multiplied by 15
- bit 15 Unimplemented: Read as '0'
- bit 14-12 COSC<2:0>: Current Oscillator Selection bits
 - 111 = Internal Fast RC (FRC) Oscillator divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC (FRC) Oscillator divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator (Posc) with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (Posc) (XT, HS or EC)
 - 001 = Internal Fast RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast RC (FRC) Oscillator
- bit 11 Unimplemented: Read as '0'
- bit 10-8 NOSC<2:0>: New Oscillator Selection bits
 - 111 = Internal Fast RC Oscillator (FRC) divided by OSCCON<FRCDIV> bits
 - 110 = Internal Fast RC Oscillator (FRC) divided by 16
 - 101 = Internal Low-Power RC (LPRC) Oscillator
 - 100 = Secondary Oscillator (Sosc)
 - 011 = Primary Oscillator with PLL module (XTPLL, HSPLL or ECPLL)
 - 010 = Primary Oscillator (XT, HS or EC)
 - 001 = Internal Fast Internal RC Oscillator with PLL module via Postscaler (FRCPLL)
 - 000 = Internal Fast Internal RC Oscillator (FRC)

On Reset, these bits are set to the value of the FNOSC Configuration bits (DEVCFG1<2:0>).

- bit 7 CLKLOCK: Clock Selection Lock Enable bit
 - If clock switching and monitoring is disabled (FCKSM<1:0> = 1x):
 - 1 = Clock and PLL selections are locked
 - 0 = Clock and PLL selections are not locked and may be modified

If clock switching and monitoring is enabled (FCKSM<1:0> = 0x): Clock and PLL selections are never locked and may be modified.

- bit 6 ULOCK: USB PLL Lock Status bit⁽¹⁾
 - 1 = Indicates that the USB PLL module is in lock or USB PLL module start-up timer is satisfied
 - 0 = Indicates that the USB PLL module is out of lock or USB PLL module start-up timer is in progress or USB PLL is disabled
- bit 5 SLOCK: PLL Lock Status bit
 - 1 = PLL module is in lock or PLL module start-up timer is satisfied
 - 0 = PLL module is out of lock, PLL start-up timer is running or PLL is disabled
- bit 4 **SLPEN:** Sleep Mode Enable bit
 - 1 = Device will enter Sleep mode when a WAIT instruction is executed
 - 0 = Device will enter Idle mode when a WAIT instruction is executed
- bit 3 CF: Clock Fail Detect bit
 - 1 = FSCM has detected a clock failure
 - 0 = No clock failure has been detected
- **Note 1:** This bit is available on PIC32MX4XX devices only.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

'1' = Bit is set

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.04	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
31:24				CHEPFAB	T<31:24>							
22:16	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
23:16				CHEPFAB	T<23:16>							
45.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
15:8	CHEPFABT<15:8>											
7.0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x				
7:0		CHEPFABT<7:0>										
k	1											
Legend	:											
R = Rea	dable bit		W = Writable	e bit	U = Unimple	mented bit, re	ad as '0'					

REGISTER 9-12: CHEPFABT: PREFETCH CACHE ABORT STATISTICS REGISTER

bit 31-0 CHEPFABT<31:0>: Prefab Abort Count bits

-n = Value at POR

Incremented each time an automatic prefetch cache is aborted due to a non-sequential instruction fetch, load or store.

'0' = Bit is cleared

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0			PKTDIS ⁽⁴⁾	HEBDET			DDDDOT	USBEN ⁽⁴⁾
	JUNE	320	TOKBUSY ^(1,5)	USBROI	HOSTEN,	RESUMEN	FFDROI	SOFEN ⁽⁵⁾

REGISTER 11-11: U1CON: USB CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-8 Unimplemented: Read as '0'

- bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit 1 = JSTATE detected on the USB
 - 0 = No JSTATE detected
- bit 6 SE0: Live Single-Ended Zero flag bit
 1 = Single Ended Zero detected on the USB
 0 = No Single Ended Zero detected
- bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾
 - 1 = Token and packet processing disabled (set upon SETUP token received)
 - 0 = Token and packet processing enabled
 - TOKBUSY: Token Busy Indicator bit^(1,5)
 - 1 = Token being executed by the USB module
 - 0 = No token being executed

bit 4 USBRST: Module Reset bit⁽⁵⁾

- 1 = USB reset is generated
- 0 = USB reset is terminated

bit 3 HOSTEN: Host Mode Enable bit⁽²⁾

- 1 = USB host capability is enabled
- 0 = USB host capability is disabled

bit 2 RESUME: RESUME Signaling Enable bit⁽³⁾

- 1 = RESUME signaling is activated
- 0 = RESUME signaling is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 11-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - **3:** Software must set the RESUME bit for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a low-speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

PIC32MX330/350/370/430/450/470

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
31:24	—	—	—	—	—	—	—	—				
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0				
23:10	—	—	—	—	—	—	—	—				
15:0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0				
15:8	ON ^(1,3)	—	SIDL ⁽⁴⁾	—	—	—	—	—				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0				
7:0	TGATE ⁽³⁾	Т	CKPS<2:0>(3)	T32 ⁽²⁾	—	TCS ⁽³⁾	—				

REGISTER 14-1: TxCON: TYPE B TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

- bit 15 **ON:** Timer On bit^(1,3)
 - 1 = Module is enabled
 - 0 = Module is disabled
- bit 14 Unimplemented: Read as '0'
- bit 13 SIDL: Stop in Idle Mode bit⁽⁴⁾
 - 1 = Discontinue operation when device enters Idle mode 0 = Continue operation even in Idle mode

bit 12-8 Unimplemented: Read as '0'

- bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit⁽³⁾
 - When TCS = 1:

This bit is ignored and is read as '0'.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6-4 TCKPS<2:0>: Timer Input Clock Prescale Select bits⁽³⁾

- 111 = 1:256 prescale value
- 110 = 1:64 prescale value
- 101 = 1:32 prescale value
- 100 = 1:16 prescale value
- 011 = 1:8 prescale value
- 010 = 1:4 prescale value
- 001 = 1:2 prescale value
- 000 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
 - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3 and Timer5). All timer functions are set through the even numbered timers.
 - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

NOTES:

NOTES:

NOTES:

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX330/350/370/430/450/470 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The UART module is one of the serial I/O modules available in the PIC32MX330/350/370/430/450/470 family of devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN and IrDA[®]. The module also supports the hardware flow control option, with UxCTS and UxRTS pins, and also includes an IrDA encoder and decoder.

The primary features of the UART module are:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- · One or two Stop bits
- Hardware auto-baud feature
- · Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 76 bps to 30 Mbps at 120 MHz
- 8-level deep First-In-First-Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- · Separate transmit and receive interrupts
- · Loopback mode for diagnostic support
- · LIN Protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 20-1 illustrates a simplified block diagram of the UART.



FIGURE 20-1: UART SIMPLIFIED BLOCK DIAGRAM

21.1 Control Registers

TABLE 21-1: PARALLEL MASTER PORT REGISTER MAP

ess										Bi	its								
Virtual Add (BF80_#	Registel Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
7000	7000 PMCON 3	31:16	_	_	—	—	—	—	—	_	_	—	—	_	—	—	_	—	0000
1000	FINCOIN	15:0	ON	_	SIDL	ADRM	JX<1:0>	PMPTTL	PTWREN	PTRDEN	CSF	<1:0>	ALP	CS2P	CS1P	—	WRSP	RDSP	0000
7010		31:16	_	_	_	_	—	_	_		_	—	_	_	_	_	_	_	0000
		15:0	BUSY	IRQN	1<1:0>	INCM	1<1:0>	MODE16	MODE	<1:0>	WAITI	B<1:0>		WAITI	M<3:0>		WAITE	E<1:0>	0000
7020		31:16	_	_	_	_	—	_	_		_	—	_	_	_	_	_	_	0000
7020	PINADUR	15:0	CS2	CS1							ADDR	<13:0>							0000
7020		31:16									17-221-05								0000
7030	PINDOUT	15:0								DATAOU	11<31.0>								0000
7040		31:16									1~31.0>								0000
7040	FINDIN	15:0								DAIAIN	1-31.0-								0000
7050		31:16	—	—	—	—	—	—	—	—	_	—	—	—	—	—	—	—	0000
7050	FIVIALIN	15:0								PTEN•	<15:0>								0000
7060	DMOTAT	31:16	_	_	_	—	-	—	—	—	—	—	—	_	—	—	_	—	0000
1000	FINISTAL	15:0	IBF	IBOV	_	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E	BFBF
Logon	du	unknow		Depart: -	- unimanlama	antad road	an for Den	at values ar	a about in l	a a v a d a a i m a									

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 12.2 "CLR, SET, and INV Registers" for more information.

REGISTER 23-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)

- 1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.
- 0 = Normal operation, buffer contents will be overwritten by the next conversion sequence
- bit 3 Unimplemented: Read as '0'
- bit 2 ASAM: ADC Sample Auto-Start bit
 - 1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.
 0 = Sampling begins when SAMP bit is set
- bit 1 **SAMP:** ADC Sample Enable bit⁽²⁾
 - 1 = The ADC sample and hold amplifier is sampling
 - 0 = The ADC sample/hold amplifier is holding
 - When ASAM = 0, writing '1' to this bit starts sampling.
 - When SSRC = 000, writing '0' to this bit will end sampling and start conversion.
- bit 0 **DONE:** Analog-to-Digital Conversion Status bit⁽³⁾
 - 1 = Analog-to-digital conversion is done
 - 0 = Analog-to-digital conversion is not done or has not started

Clearing this bit will not affect any operation in progress.

- **Note 1:** When using the 1:1 PBCLK divisor, the user software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ 0, this bit is automatically cleared by hardware to end sampling and start conversion.
 - **3:** This bit is automatically set by hardware when ADC is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	—	CSSL30	CSSL29	CSSL28	CSSL27	CSSL26	CSSL25	CSSL24
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23:16	CSSL23	CSSL21	CSSL21	CSSL20	CSSL19	CSSL18	CSSL17	CSSL16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0

REGISTER 23-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15-0 CSSL<30:0>: ADC Input Pin Scan Selection bits^(1,2)
 - 1 = Select ANx for input scan
 - 0 = Skip ANx for input scan
- **Note 1:** CSSL = ANx, where x = 0-27; CSSL30 selects Vss for scan; CSSL29 selects CTMU input for scan; CSSL28 selects IVREF for scan.
 - 2: On devices with less than 28 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
21.24	R/P	R/P	R/P	R/P	U-0	U-0	U-0	U-0				
31:24	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	_				
22.16	U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P				
23.10	—	—	—	—	—	FSRSSEL<2:0>						
15.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P				
15:8	USERID<15:8>											
7.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P				
7.0				USERID<	7:0>							

REGISTER 28-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **FVBUSONIO:** USB VBUS_ON Selection bit 1 = VBUSON pin is controlled by the USB module

- 0 = VBUSON pin is controlled by the OSB module0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit 1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function
- bit 29 IOL1WAY: Peripheral Pin Select Configuration bit
 - 1 = Allow only one reconfiguration
 - 0 = Allow multiple reconfigurations
- bit 28 PMDL1WAY: Peripheral Module Disable Configuration bit
 - 1 = Allow only one reconfiguration
 - 0 = Allow multiple reconfigurations
- bit 27-19 Unimplemented: Read as '0'

bit 18-16 FSRSSEL<2:0>: Shadow Register Set Priority Select bit

These bits assign an interrupt priority to a shadow register.

- 111 = Shadow register set used with interrupt priority 7
- 110 = Shadow register set used with interrupt priority 6
- 101 = Shadow register set used with interrupt priority 5
- 100 = Shadow register set used with interrupt priority 4
- O11 = Shadow register set used with interrupt priority 3
- 010 = Shadow register set used with interrupt priority 2
- 001 = Shadow register set used with interrupt priority 1
- 000 = Shadow register set used with interrupt priority 0
- bit 15-0 USERID<15:0>: This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG

TABLE 31-34: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: } 2.3V \ to \ 3.6V \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ for \ Commercial \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ for \ Industrial \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \ for \ V-temp \end{array}$			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
IS10 TLO:SCL Clock Low Time		100 kHz mode	4.7	—	μS	PBCLK must operate at a minimum of 800 kHz	
			400 kHz mode	1.3	—	μS	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	—	μS	_
IS11 THI:SCL		Clock High Time	100 kHz mode	4.0	—	μS	PBCLK must operate at a minimum of 800 kHz
			400 kHz mode	0.6	—	μS	PBCLK must operate at a minimum of 3.2 MHz
			1 MHz mode (Note 1)	0.5	_	μS	—
IS20	TF:SCL	SDAx and SCLx	100 kHz mode		300	ns	CB is specified to be from
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode (Note 1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx	100 kHz mode		1000	ns	CB is specified to be from
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	10 to 400 pF
			1 MHz mode (Note 1)	_	300	ns	
IS25 T	TSU:DAT	Data Input	100 kHz mode	250	_	ns	—
		Setup Time	400 kHz mode	100	—	ns	_
			1 MHz mode (Note 1)	100	—	ns	
IS26 THD:DAT	THD:DAT	Data Input	100 kHz mode	0	—	ns	_
		Hold Time	400 kHz mode	0	0.9	μs	_
			1 MHz mode (Note 1)	0	0.3	μS	
IS30	Tsu:sta	Start Condition	100 kHz mode	4700	—	ns	Only relevant for Repeated
		Setup Time	400 kHz mode	600	—	ns	Start condition
			1 MHz mode (Note 1)	250	_	ns	
IS31	THD:STA	Start Condition	100 kHz mode	4000	_	ns	After this period, the first
		Hold Time	400 kHz mode	600	—	ns	clock pulse is generated
			1 MHz mode (Note 1)	250	—	ns	
IS33	Tsu:sto	Stop Condition Setup Time	100 kHz mode	4000		ns	_
			400 kHz mode	600		ns	
			1 MHz mode (Note 1)	600	_	ns	

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

AC CHA Param. No.	ARACTERIS	STICS ⁽⁵⁾ Characteristics	Standard Op (unless othe Operating ter Min.	oerating Co erwise stat mperature Typical	onditions: 2 ed) 0°C ≤ TA ≤ -40°C ≤ TA ≤ -40°C ≤ TA ≤ Max.	2.3V to +70°C ≤ +85°C ≤ +105° Units	3.6V for Commercial for Industrial C for V-temp Conditions	
ADC Accuracy – Measurements with Internal VREF+/VREF-								
AD20d	Nr	Resolution	1	0 data bits		bits	(Note 3)	
AD21d	INL	Integral Nonlinearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)	
AD22d	DNL	Differential Nonlinearity	> -1	_	< 1	LSb	VINL = AVss = 0V, AVDD = 2.5V to 3.6V (Notes 2,3)	
AD23d	Gerr	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)	
AD24d	Eoff	Offset Error	> -2	_	< 2	LSb	VINL = AVss = 0V, AVDD = 2.5V to 3.6V (Note 3)	
AD25d	—	Monotonicity	_	—	_	_	Guaranteed	
Dynamic Performance								
AD31b	SINAD	Signal to Noise and Distortion	55	58	—	dB	(Notes 3,4)	
AD34b	ENOB	Effective Number of Bits	9 9.5 —				(Notes 3,4)	

TABLE 31-35: ADC MODULE SPECIFICATIONS (CONTINUED)

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

3: These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

5: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 31-10 for VBORMIN values.

AC CHARACTERISTICS ⁽²⁾				Standa (unles Operat	ard Operating s otherwise s ing temperatu	tated) re $0^{\circ}C \le TA \le +70^{\circ}C$ for Commercial $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp
ADC Input	ADC Speed	TAD Min.	Sampling Time Min.	Rs Max.	Vdd	ADC Channels Configuration
AN0-AN14	1 Msps to 400 ksps ⁽¹⁾	65 ns	132 ns	500Ω	3.0V to 3.6V	ANX CHX ADC
	Up to 400 ksps	200 ns	200 ns	5.0 kΩ	2.5V to 3.6V	ANX CHX ANX OF VREF- ANX OF VREF- ANX OF VREF-
AN15-AN27	400 ksps ⁽¹⁾	154 ns	1000 ns	500Ω	3.0V to 3.6V	ANX CHX ADC

TABLE 31-36: 10-BIT CONVERSION RATE PARAMETERS ſ

Note 1: External VREF- and VREF+ pins must be used for correct operation.

2: These parameters are characterized, but not tested in manufacturing.



PIC32MX330/350/370/430/450/470

100

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-193A Sheet 1 of 2

APPENDIX A: REVISION HISTORY

Revision A (July 2012)

This is the initial released version of the document.

Revision B (April 2013)

Note:	The status of this data sheet was updated				
	to Preliminary; however, any electrical				
	specifications listed for PIC32MX370/470				
	devices is to be considered Advance				
	Information and is marked accordingly.				

This revision includes the following updates, as shown in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section	Update Description			
"32-bit Microcontrollers (up to 512 KB Flash and 128 KB SRAM) with Audio/Graphics/Touch (HMI), USB,	SRAM was changed from 32 KB to 64 KB. Data Memory (KB) was changed from 32 to 64 for the following devices (see			
and Advanced Analog"	 PIC32MX350F256H PIC32MX350F256L PIC32MX450F256H PIC32MX450F256L The following devices were added: PIC32MX370F512H PIC32MX370F512L PIC32MX470F512H 			
	 PIC32MX470F512H PIC32MX470F512L 			
4.0 "Memory Organization"	The Memory Map for Devices with 256 KB of Program Memory was updated (see Figure 4-3).			
	The Memory Map for Devices with 512 KB of Program Memory was added (see Figure 4-4).			
7.0 "Interrupt Controller"	Updated the Interrupt IRQ, Vector and Bit Locations (see Table 7-1).			
20.0 "Parallel Master Port (PMP)"	Added the CS2 bit and updated the ADDR bits in the Parallel Port Address register (see Register 20-3).			
27.0 "Special Features"	Updated the PWP bit in the Device Configuration Word 3 register (see Register 27-4).			
30.0 "Electrical Characteristics"	Note 2 in the DC Characteristics: Operating Current (IDD) were updated (see Table 30-5).			
	Note 1 in the DC Characteristics: Idle Current (IIDLE) were updated (see Table 30-6).			
	Note 1 in the DC Characteristics: Power-down Current (IPD) were updated (see Table 30-7).			
	Updated Program Memory values for parameters D135 (Tww), D136 (Trw), and D137 (TPE and TCE) (see Table 30-12).			
31.0 "DC and AC Device Characteristics Graphs"	New IDD, IIDLE, and IPD current graphs were added for PIC32MX330/430 devices and PIC32MX350/450 devices.			